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Varactor Based Capacitive Shunt Switch Using BaSrTiO₃ (BST) Thin-Films for Microwave Applications

Dissertation

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UNIVERSITY OF DAYTON

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By

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UNIVERSITY OF DAYTON

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VARACTOR BASED CAPACITIVE SHUNT SWITCH USING BaSrTiO₃ (BST)
THIN-FILMS FOR MICROWAVE APPLICATIONS

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ABSTRACT

VARACTOR BASED CAPACITIVE SHUNT SWITCH USING BaSrTiO₃ (BST) THIN-FILMS FOR MICROWAVE APPLICATIONS

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Recently there has been growing interest in the field of tunable microwave/millimeterwave applications. This dissertation describes a Barium Strontium Titanate (BST) thin-film based capacitive shunt switch for applications in RF/Microwave industry. The performance of the switch is based on the dielectric tunability of BST thin-films. This dissertation demonstrates the design, theory of operation, theoretical analysis, modeling, optimization, electromagnetic simulation, fabrication, experimental results, applications, and possible future research of the capacitive shunt switch.

Specifically this dissertation addresses the capacitive shunt switch which is designed on a multilayer substrate with a coplanar waveguide (CPW) transmission line configuration. High resistivity Si ($> 6 \text{ K}\Omega\text{-cm}$) is used as a

substrate. The novelty of the capacitive shunt switch is in the utilization of dielectric tunability and elimination of moving parts as compared to the RF MEMS switches. The dielectric permittivity of the BST thin-films reduces with an applied dc voltage.

SonnetTM electromagnetic simulation tools have been utilized for the design and theoretical analysis of the switches verified with the experimental data. The dissertation also addresses the potential applications and future research using this device (capacitive shunt switch) in microwave/millimeterwave applications.

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LIST OF ABBREVIATIONS

BaSrTiO₃= BST

BST= Barium Strontium Titanate

SrTiO₃= STO

STO= Strontium Titanate

CPW= Coplanar Waveguide

PLD= Pulsed Laser Deposition

MEMS= Microelectromechanical Systems

SEM= Scanning Electron Microscope

LAO= Lanthanum Aluminate

ESL= Equivalent Series Inductance

ESR= Equivalent Series Resistance

IDC= Interdigital Capacitor

VCOs= Voltage Control Oscillators

MMICs= Monolithic Microwave Integrated Circuits

CHAPTER I

INTRODUCTION

1.1 Motivation

Since the early 1960s, ferroelectrics have been regarded as attractive materials for applications in electrical tunable microwave devices and a number of practical devices have been demonstrated [1]-[4]. In general, ferroelectric materials should be in paraelectric phase for the application of the electrically tunable microwave devices. Ferroelectric thin films are very attractive because of their electrical tunability of the relative dielectric constant with an applied dc bias [5]. The change in permittivity can be utilized in microwave devices for frequency and phase agility [6]. The applications of the ferroelectric materials in the field of microwave engineering include field-dependent tunable capacitors (varactors), tunable resonators, phase shifters, tunable filters, variable power dividers, variable frequency oscillators, harmonic generation, pulse shaping, mixing, and parametric amplification [6]. Recently, there is a great deal of interest in using ferroelectric materials for nonvolatile memory applications and micro-electromechanical systems [7]. Ferroelectric thin-film based devices are fast, small, lightweight and have low power consumption. Ferroelectric components

are simple in nature and allow cost effective integration in complex microwave systems [8]-[10].

With the increased use of tunable ferroelectric thin-films in microwave applications, Strontium Titanate (SrTiO_3) STO and Barium Strontium Titanate ($\text{Ba}_x\text{Sr}_{1-x}\text{TiO}_3$), henceforth known as BST are two of the most attractive ferroelectric thin-films being studied [5]. BST is attractive for room temperature applications, whereas STO is attractive for low temperature applications. Ferroelectric thin-films of BST are used in high frequency applications including tunable filters, phase shifters, voltage controlled oscillators, RF MEMS switches, reconfigurable antennas, due to the large electric field dependent permittivity, low loss tangent, high dielectric constant, high power handling capability [11], negligible dc power consumption, potential low cost, high integration capability, requiring low tuning voltage and high speed. The dielectric constant of BST thin-films can be tuned by applying a dc voltage [12]-[13] and by varying the film-thickness, a wide range of operating voltages can be obtained. BST thin-films can withstand high operating voltages as it has a high breakdown field ($>2\text{MV/cm}$). The electrical properties of BST thin-films greatly depend on the BST composition (Ba/Sr ratio and Ti composition), the bottom and top electrode materials, film thickness, processing temperature [14], and pressure.

With the advent of microelectromechanical systems (MEMS) technology, more and more attention has been focused on the development of MEMS

devices for RF applications [15]. MEMS switches are one of the most prominent micromachined products that have attracted numerous research efforts in recent years and have many potential applications such as impedance matching networks, filters, voltage controlled oscillator, phase shifters, signal routing in RF system front-end, and other high frequency reconfigurable circuit applications. MEMS switches provide many advantages over the conventional electromechanical or solid-state counterparts because of low insertion loss, high isolation, low power consumption, high breakdown voltage, high linearity, low fabrication cost and high integration capability [15]-[21]. The majority of MEMS switches reported to date employ electrostatic actuation [22]-[25] and require a high actuation voltage which is one of the major drawbacks of the MEMS switches. The performance of RF MEMS switches can be improved by using tunable BST thin-films [26]-[28]. It has been shown that isolation can be improved by more than 10 dB by using ferroelectric materials of BST thin-films instead of other dielectric materials (e.g., Si_3N_4) [26], [28]. However, RF MEMS switches do have several limitations such as relatively low speed, low power handling capability, required high actuation voltage, low reliability, low switching lifetime, fabrication complexity, and packaging cost. Before RF MEMS switches are widely accepted by the market, these problems need to be overcome. For this reason, a new switch has been demanded for high frequency applications.

This dissertation addresses a new concept (a ferroelectric varactor-based capacitive shunt switch) for high frequency RF applications which will overcome

most of the existing limitations in RF MEMS switches. To our knowledge, it is the first time that this type of a switch is being reported for high frequency RF applications. A ferroelectric varactor-based capacitive shunt switch [8],[12],[13],[29]-[31] has been developed that is designed on high resistivity Si/SiO₂ substrates with coplanar waveguide (CPW) transmission line configuration using ferroelectric materials of BST thin-films as a dielectric layer. This dissertation addresses the design, modeling (physical and electrical), optimization, electromagnetic simulations, theoretical analysis and experimental results for the varactor-based capacitive shunt switch. The experimental results have been verified with the simulations and the theoretical analysis. This dissertation also addresses possible potential applications using the capacitive shunt switches.

Possible uses for the varactor-based capacitive shunt switch include microwave switching circuits, analog/continuous phase shifters, tunable filters, voltage control oscillator, matching networks, sensor for RF applications, etc.

1.2 Research objectives

The primary objective of this dissertation is to develop a Si monolithic microwave integrated circuit (MMICs) compatible ferroelectric varactor-based capacitive shunt switch using ferroelectric material of BST thin-films on high resistivity Silicon (Si) substrate. The switch is designed on multilayer substrates with a coplanar waveguide (CPW) transmission line configuration. The switch

operations are based on the dielectric tunability of the BST thin-films. The main research objectives of this dissertation are as follows:

1. Design, modeling, optimization, simulation, and theoretical analysis of the ferroelectric varactor-based capacitive shunt switch using BST thin-films. The switch is designed for a wide range of frequencies. The objective is to minimize the insertion loss and improve the isolation in the ON and OFF states respectively. Also, an electrical model of this switch has been developed for the potential applications in microwave integrated circuits such as integrated filters, voltage control oscillator (VCO's), phase shifters, reconfigurable antennas, and wireless sensing device.
2. Experimental verification of the ferroelectric varactor shunt switches. The experimental work included switching speed measurements, frequency response of the switches, etc.

The following research questions have been addressed in this dissertation:

- I. What is the optimum varactor area and dielectric constant of the ferroelectric thin-films, necessary to get high isolation and low insertion loss?
- II. What is the minimum voltage required to tune the dielectric constant of the BST thin-films to obtain maximum tunability?

- III. What is the maximum voltage the BST thin-films can withstand before destructive breakdown of switches?
- IV. Can the designed switch overcome the limitations of the existing RF MEMS switches in terms of isolation, insertion loss, speed, switching lifetime, reliability, packaging, power handling, etc.?

1.3 Significance of our study

Currently RF MEMS technology offers the potential for low insertion loss, high isolation capacitive shunt switches over a broad frequency range. The ferroelectric varactor-based capacitive shunt switch is normally in the "OFF" state compared to capacitive shunt RF MEMS switches which are in the normally "ON" state. The switching speed of the varactor-based capacitive shunt switch is about ~43ns, whereas the RF MEMS switch is about ~10 μ s. A lower bias voltage (~10V) can be used for varactor shunt switches compared to 40-60V needed for RF MEMS switches. In combination with a rectifying antenna which can convert an RF signal into a dc bias voltage, one can use this switch for remote activation and integration.

The integration of ferroelectric thin-films with Si MMICs should allow designers to use larger capacitor values with reasonable high Q values (~100@10GHz). The size of capacitors will be reduced due to the large dielectric constant of the ferroelectric thin-films (500 at zero bias to 120 at high bias). The higher power handling capability of the ferroelectric thin-film varactor (~ 10W or

higher @ 10 GHz) gives improved power handling performance of MMICs over that of the semiconductor varactor-based tunable MMICs. Since the varactor-based capacitive shunt switch does not have any moving part, it has a higher switching lifetime compared to RF MEMS switches and it has lower packaging cost. The fabrication cost and complexity of this switch are lower than the RF MEMS counterparts. This switch is free from the stiction problem compared to the RF MEMS switches.

The switching performance depends on the tunability of the BST thin-films and therefore extra care needs to be taken during the fabrication process. Precise control of the composition ratio, grain size, temperature and pressure of the BST thin-films during the fabrication process are the key issues to achieve higher tunability of the films. The higher the tunability, the better the performance of this switch. Greater than 5:1 tunability has been obtained in the BST thin-films [60/40 (Ba/Sr) composition ratio] with an average grain size of 60nm, grown at 750°C and 75mT oxygen partial pressure. The switch is implemented on Si/SiO₂ multilayer substrates with a coplanar waveguide (CPW) transmission line configuration. We have used high resistivity Si (>6KΩ-cm) as a substrate to reduce the loss in high frequency applications. Without applying a dc voltage, the shunt capacitance of the switch is high, resulting in most of the signal shunted to the ground from the signal line of the CPW transmission line. In this case, the switch is in the OFF state. By applying a biasing voltage (~10V) between the signal and ground lines of the CPW transmission line, the dielectric constant of

BST thin-films and the capacitance of the switch are reduced, allowing for most of the signal to pass through from the input to the output port. As a result the switch is in the ON state.

The higher isolation in the OFF state and the lower insertion loss in the ON state depend on the overlap area of the varactor and dielectric constant of the BST thin-films. The varactor area can be used as a design parameter for obtaining high isolation at a specific frequency. The maximum isolation is obtained at a frequency determined by the series resonance of the varactor and parasitic inductance. It is also possible to obtain the higher isolation and lower insertion loss at lower frequency (<5 GHz) by cascading two switches with the same dimension and a variable length of the shunt line between the two grounds.

CHAPTER II

LITERATURE REVIEW

2 Literature review on ferroelectric tunable microwave circuits and devices

Ferroelectric materials have been studied since the early 1960s for applications in microwave devices. Several references [6][32][33] provide a comprehensive review of the work on ferroelectric materials using Strontium Titanate (STO) and Barium Strontium Titanate (BST); this includes models of the ferroelectric permittivity and loss tangent, as well as methods of measurement of these properties. Recently, a large number of groups are involved in research on the ferroelectric materials in microwave applications due to various advantageous such as high switching speed, small size, lightweight, low actuation voltage, low power consumption, and high integration capability. Strontium Titanate (SrTiO_3) and Barium Strontium Titanate ($\text{Ba}_x\text{Sr}_{1-x}\text{TiO}_3$) are two of the most popular ferroelectric thin-film materials currently being studied [5]. The relative dielectric constant of ferroelectric thin-films can be tuned by applying an external dc voltage. This dielectric tunability is attractive for fabrication of tunable RF and microwave devices. Such devices include varactors, phase shifters, voltage control oscillators (VCOs), tunable filters, reconfigurable antennas, and RF MEMS switches [14],[26]-[27],[34]-[38].

Ferroelectric materials have a characteristic temperature called Curie temperature (T_C) at which the material changes from a polar (ferroelectric) to a non-polar (paraelectric) phase. Ferroelectrics in polar phase have not been considered for applications in tunable microwave devices as they introduce large losses at relatively low microwave frequencies (typically <10 GHz). Additional losses at low frequencies are associated with the domain wall movements [4]. The ferroelectric non-polar phase (paraelectric) possesses zero spontaneous polarization that can be oriented by an applied electric field (i.e., no hysteresis loop), but the relative dielectric constant remains large and can be changed with the applied electric field. This enables the fabrication of electrically tunable capacitors with large tunabilities ($>50\%$) at a dc-bias voltage [34],[35]. The tunable capacitors can be used in tunable microwave circuits and devices.

Tunability and loss tangent are the most important basic parameters characterizing ferroelectrics for applications in tunable microwave devices. The losses are among the most critical issues in ferroelectric device applications and most of the efforts in recent years have been devoted to the optimization of film fabrication processes in terms of microwave loss reduction [4]. STO thin-films exhibit lower tunability ($<20\%$) and are not suitable for integration in systems operating at room temperature. BST thin-films can overcome these difficulties [34]. BST is a very attractive for RF tunable ferroelectric material due to its large field dependent permittivity, high dielectric constant, high electrical breakdown field, charge storage capacity, and low loss tangent. Precise control of

composition and microstructure is critical for the production of BST thin-films with large field dependence permittivity, low losses, and high electrical breakdown fields that are required for successful integration of BST into tunable high frequency microwave devices. Other prominent features of BST thin-films are integration capability with active devices like MMICs, low cost, simultaneous fabrication of multiple sections, low losses and high power handling capability [11],[34]. A wide range of operating voltages can be obtained by changing the film thickness.

BST thin-film based varactors offer the advantages of integration capability, low cost, low voltage tunability and high speed. BST varactors do not produce junction noise in comparison with the reverse biased junction in semiconductor varactor diodes and in general, the semiconductor varactor diodes tend to be lossy at RF and microwave frequencies [14]. The temperature dependence of the dielectric permittivity of ferroelectric materials is a major problem in practical implementations of tunable ferroelectric devices. One can overcome this problem by using appropriate thickness and permittivity of the layers, ratio between the total thickness of the films, and the width of the gap between electrodes [4]. The temperature and pressure need to be precisely controlled during the thin-film growth as the performance of the ferroelectric based device depends on the film qualities.

Currently, our group is actively involved in research on tunable microwave components and circuits using ferroelectric materials [39]. Our group is currently investigating the nano-structured $\text{Ba}_{0.6}\text{Sr}_{0.4}\text{TiO}_3$ (BST) thin-films [39]. The average grain size of the thin-films is controllable from ~20nm to ~150nm with the oxygen ambient pressure from 38mT to 150mT. We have found that the films with smaller average grain size to be tunable and low loss up to 50 GHz. A low loss tunable high K dielectric for variety of applications can be implemented by controlling the grain size.

Tunable electromagnetic band gap structures (EBGs) [37],[39] have been designed using thin-films of ferroelectric materials such as STO and BST. The tunable CPW EBG structure has been realized on multilayer substrates (high resistivity Si) with thin-films (BST or STO) varactors fabricated by the laser ablation method. The performance of the EBG depends on the tunability of the capacitance of the ferroelectric varactors. BST thin-film reduces the size of the EBG structures due to the higher dielectric constant, since the wavelength of these structures is inversely proportional to the square root of the dielectric permittivity. A one-dimensional tunable EBG structure has been designed and experimentally verified using CPW transmission line, periodically loaded by a ferroelectric varactor. The first bandgap has been observed between 20-35GHz, and the second one between 45-70GHz with changing the capacitance values (150fF, 200fF, and 250fF) have been achieved in the EBG structure described in

[37],[39]. The tunability up to 10% has been achieved, under the biasing voltage of 20V in the EBG structures.

A tunable K-band frequency agile band pass filter [5] has been implemented using ferroelectric material of STO on LaAlO_3 substrates with a microstrip transmission line. This circuit could be used in K-band satellite communication subsystems such as a receiver front-end. The dielectric constant of STO thin-films is taken 300, 1650, and 3000 and the loss tangent has been assumed to be 0.01. The two pole filter has a center frequency of 19 GHz and 4% bandwidth. A large tunability of greater than 10% has been obtained in the bandpass filters operating below 77K. A center frequency shift of 2.3 GHz has been achieved at a 400V bipolar dc bias, and 30K with a minimal degradation in the insertion loss of the filter. The lowest passband insertion loss measured has been obtained approximately 1.5dB at 24K. The unbiased filter's passband at 77K has been centered at 17.4 GHz with return losses better than 10 dB in the passband, and the minimum insertion loss is approximately 3.3 dB. The center frequency of this filter shifted from 17.4 GHz at no bias to 19.1 GHz at $\pm 500\text{V}$ bias with a tunability of 9% at 77K. Tunable low pass and band pass filters [34] have been designed using BST thin films in RF applications. The lowpass filter has an insertion loss of 2 dB and a tunability of 40% (120-170 MHz) with a bias voltage of 0-9V dc. The bandpass filter has an insertion loss of 3 dB and a tunability of 57% (176-276 MHz) with the application of 0-6 V dc. The third-order intercept point of the band

pass filter has been measured to be 19 dBm by applying of two tones around 170 MHz.

Several groups [8],[36],[40]-[50] are engaged in research on phase shifters using ferroelectric materials of BST thin-films for RF applications. In these applications, BST forms either the entire substrate [8],[36],[40],[49] on which the conductors are deposited or a small part of the substrate (selective area deposition) with BST thin-films between the substrate and the conductors [45]-[48]. Other circuits have been implemented [42]-[43],[49]-[50] by periodic loading of transmission lines with tunable BST capacitors. Biasing the BST varactor, changes the phase velocity of the transmission line, achieving the required phase shift. A relative phase shift per dB insertion loss has been obtained approximately 75 degrees per dB at 5 GHz, and drop down to 10 degrees/dB at 20 GHz with a bias voltage between 0V and 9.5V [8]. An X-band distributed phase shifter fabricated using the new process provided 240 degrees phase shift with an insertion loss of 3 dB at 10 GHz at room temperature [50]. The phase shifter is demonstrated a figure of merit of 93 degrees per dB at 6.3 GHz and 87 degrees per dB at 8.5 GHz at room temperature. A planar microstrip phase shifter has been reported in reference [40] that provided 20 degrees per dB at 2.65 GHz. A phase shift of 165 degrees at 2.4 GHz with only 3 dB loss and a bias of 250V have been obtained from a microstrip on a BST thin-film [41]. A phase capable of continuous 0-160 degrees phase shift at 30 GHz with the insertion loss of 5.8 dB and the return loss less than 12 dB over all phase states

has been demonstrated in reference [49]. A figure of merit of 120 degrees per dB at 40K has been reported using coupled microstriplines as dc electrodes ($\text{YBa}_2\text{Cu}_3\text{O}_{7-\delta}$) with thick SrTiO_3 thin-films [51]. Using Au electrodes with 400nm thick $\text{Ba}_{1-x}\text{Sr}_x\text{TiO}_3$ films, some devices have been demonstrated approximately 70 degrees per dB at room temperature [52]. A strip-line circuit with a BST capacitor is provided a differential phase shift of 11 degrees at X-band with a biasing field of 70 kV/cm [53]. Another phase shifter with a figure of merit of 45 degrees per dB has been demonstrated with a 500V bias [36].

Recently, ferroelectric thin-films of BST and STO have initiated a renewed interest toward the electrically tunable devices based on interdigital capacitors [54]-[56]. An interdigital capacitor using $\text{YBa}_2\text{Cu}_3\text{O}_{7-\delta}$ (YBCO) and $\text{Ba}_x\text{Sr}_{1-x}\text{TiO}_3$ has been reported [54] with variations in capacitance of more than 6 to 1 at 86K with a peak electric field strength of 25 kV/cm. Also an interdigital capacitor on LaAlO_3 substrate using BST thin-films has been deposited by the metal organic deposition (MOD) process has been reported with an approximate tuning range of 10% for peak field of 66 kV/cm at the temperature range from 50K to 120K [54]. The tunability of STO films of Au/STO/YBCO parallel plate configuration of 47, 32, and 30% with an electric field of 0.1MV/cm are demonstrated in reference [56]. At 77 K, a tunability of 70% has been observed, and $\tan\delta$ ranged from 0.015 to 0.001, depending on bias. The loss behavior of the STO film with the interdigital structure has been attributed to defects intrinsic to the STO film, whereas the

loss behavior of the STO/YBCO film has been dominated by electrical shorting of the YBCO through the STO layers [56].

Ferroelectric thin-films have been used to improve the performance of the RF MEMS switches [26]-[27]. A prototype MEMS switches for K/Ka band applications are designed using BST thin-film with $\epsilon_r > 200$ [26]. The high dielectric constant of BST thin-film resulted in both higher isolation and smaller device size for MEMS switches. More than 30 dB isolation has been obtained in a wide frequency range from 16 GHz to 36 GHz with an actuation voltage as low as 10-20V. A shunt MEMS switch with a high temperature superconductor (HTS) by using a BaTiO₃ thin-film has been reported for RF applications [27]. This switch is demonstrated a high isolation of more than 30 dB up to 1.8 GHz and very low insertion loss of 0.06 dB at 2 GHz. A capacitive shunt RF MEMS switch [28] has been designed on multilayer substrates with a CPW configuration using BST thin-films. Isolation could be improved by more than 10 dB using BST thin-films as the dielectric layer instead of other dielectric materials such as Si₃N₄.

The main idea behind the use of ferroelectric materials in tunable microwave circuits is the large dielectric tunability with low additional microwave dielectric losses due to the insertion of the ferroelectric thin films. Dielectric tunability is defined as the $(\epsilon_r(0) - \epsilon_r(V)) / \epsilon_r(0)$. High – temperature superconductors (HTS) could be used with a combination of the ferroelectric thin-films to reduce the losses at microwave frequencies [57].

CHAPTER III

FERROELECTRIC MATERIALS

3 Introduction to ferroelectric materials

Ferroelectricity is one of the most fascinating properties of dielectric solids. Materials exhibiting ferroelectric properties must be either single crystals or polycrystalline solids composed of the crystallinities; they must also possess reversible spontaneous polarization [58]. The term ferroelectric is analogous with ferromagnetics because of similar characteristics. Ferromagnetic materials contain iron atoms but in ferroelectrics there are no iron atoms [57]. Like ferromagnetics, ferroelectrics show a spontaneous polarization below the Curie temperature, a hysteresis loop, and an associated mechanical strain. Ferroelectric materials differ from ferromagnetic materials for their fundamental mechanisms and their applications.

Crystals are classified into seven systems according to their geometry and the systems can be subdivided into point groups (crystal classes) according to their symmetry with respect to a point. There are 32 such crystal classes and 11 of them possess a centre of symmetry (nonpolar) and remaining 21 are non-centrosymmetric, the polar piezoelectrics. Of the 21 noncentrosymmetric crystal classes, only one doesn't exhibit piezoelectric effect [58]. In 10 of these 20

classes, polarization can be induced by a mechanical stress, while the other 10 classes exhibit spontaneous polarization, so they are permanently polar and thus can have piezoelectric as well as pyroelectric effects. There is a subgroup within these 10 classes that possess spontaneous polarization and reversible polarization; this subgroup can show all three effects-ferroelectric, piezoelectric, and pyroelectric. In fact, the ferroelectric effect is distinct from piezoelectric and pyroelectric effects in that it exists with a reversible polarization. A crystal is said to be ferroelectric when it has two or more orientational states in the absence of an electric field and can be shifted from one to the other states by an electric field [59]. If ferroelectrics are to be considered as a subgroup of the pyroelectric class which includes only those crystals capable of being switched in some manner, then whether or not a material is ferroelectric depends on experimental limitations. Crystal structure, perfection, electrical conductivity, pressure, and temperature are all factors which affect the reversibility of polarization.

A very important group of ferroelectrics is known as the perovskites with the general formula of ABO_3 , where A is a monovalent or divalent metal and B is a tetra- or pentavalent one (Fig. 3.1). It is cubic, with A atoms at the cube corners, B atoms at the body centers, and the oxygen atoms at the face centers. Fig. 3.1 describes the unit cell of the ferroelectric materials of STO and BST thin-films. The structure of the unit cell is temperature dependent [58]. At a certain transition temperature (T_c), the particular structure of the unit cell becomes unstable and must transform to a more stable one. Therefore, the unit cells become

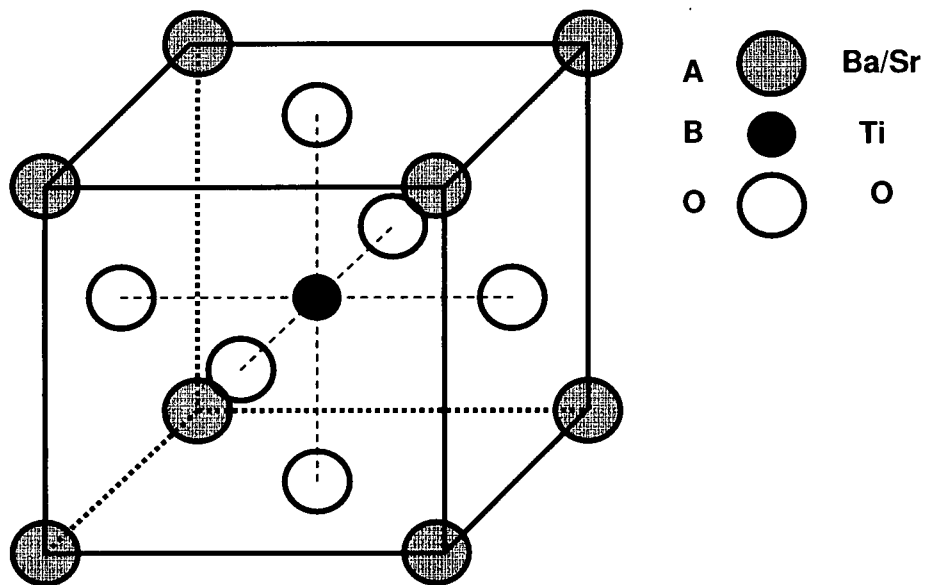


Fig. 3.1 : Unit cell of a perovskite structure.

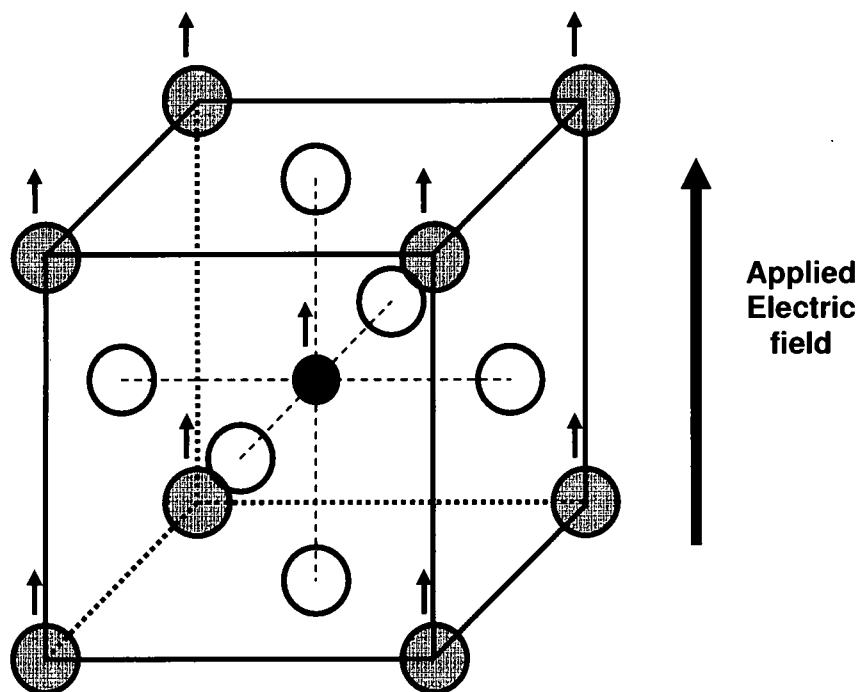


Fig. 3.2 : Electric field on the unit cell of the ferroelectric material.

permanently polarized and behave as permanent dipoles, leading to spontaneous polarization. The direction of the dipole moment can be reversed by applying a large electric field with opposite polarity. Fig. 3.2 shows the direction of the applied electric field on the unit cell of the ferroelectric materials. The reversal of the dipole moment distinguishes ferroelectric materials from nonferroelectric ones. The direction of spontaneous polarization is always along the direction of the unit cell's elongation, that is, the stretching direction (c-axis). This is also referred to as the ferroelectric polar axis.

Ferroelectric material exhibits spontaneous polarization. A crystal of such a material consists of positive and negative ions, which become displaced at a certain temperature. The displacement results in a net dipole moment. The orientation of the dipole moment in ferroelectric materials can be shifted by applying an electric field. The appearance of the spontaneous polarization is highly temperature dependent, and in general, ferroelectric crystals undergo phase transitions which involve structural changes. As the temperature decreases from above the Curie temperature, a structural phase change occurs and the crystal goes from paraelectric to ferroelectric region [6], [60]. From Fig. 3.3, we see that above the Curie temperature, the ferroelectric material is no longer in ferroelectric phase, it is in paraelectric phase. One can also see from Fig. 3.3 that in the paraelectric phase, ferroelectric material does not show any spontaneous polarization, however it shows a high dielectric constant slightly above the transition temperature (T_c).

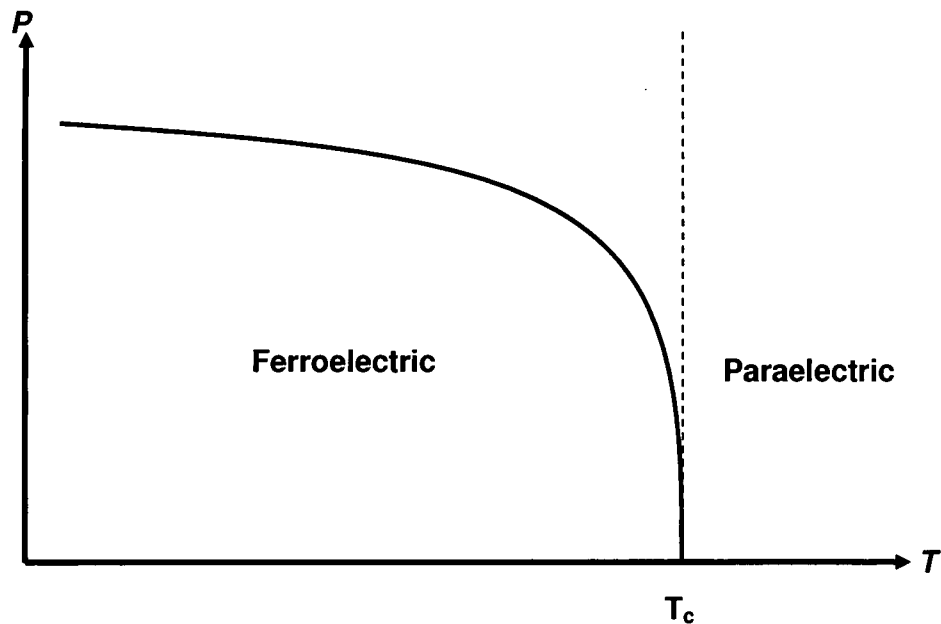


Fig. 3.3 : Spontaneous polarization versus temperature showing the two distinct phases of a ferroelectric material.

Fig. 3.4 describes the spontaneous polarization versus applied electric field of the ferroelectric materials showing the hysteresis behavior. One can see a couple of important observations from figure (Fig. 3.4). By applying a field, the polarization value increases and at a certain field, polarization value doesn't change any more due to saturation effects, and this polarization is called the saturation polarization (P_{Sat}). Now, if one removes the applied electric field, the polarization value does not return to the initial condition (zero). It holds some dipole moment in the direction it was polarized, and it is called the remanent polarization (P_r). To reduce the polarization to zero, an electric field needs to be applied in the opposite direction. The amount of electric field which reduces the net polarization to zero is called the coercive field (E_c).

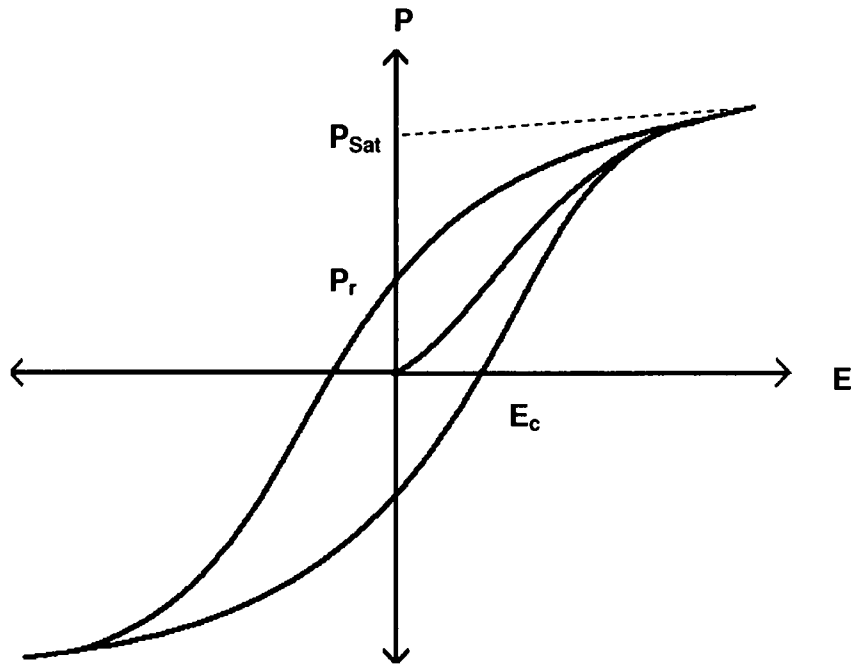


Fig. 3.4 : Variation of the polarization with electric field of the ferroelectric material.

The net polarization in the ferroelectric material is due to (1) spontaneous polarization, (2) electronic polarization, and (3) ionic polarization [57],[61].

The dielectric constant is the most important property of the ferroelectric materials. Above the Curie temperature, ferroelectric materials have neither polarization nor exhibits hysteresis behavior. They exhibit a high relative dielectric constant which is the slope of the polarization versus the electric field. The dielectric constant of ferroelectric materials depends on several factors such as temperature, grain size, composition ratio, pressure, and applied field.

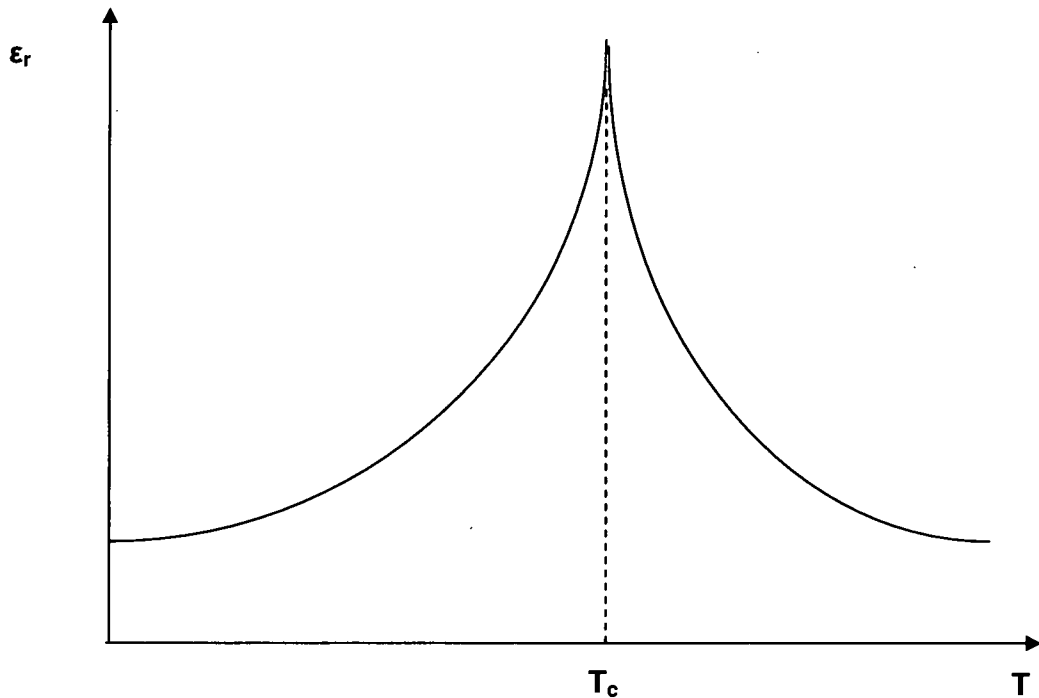


Fig. 3.5 : Variation of the relative dielectric constant with temperature for a ferroelectric material.

Fig. 3.5 shows the temperature dependence dielectric constant of the ferroelectric materials. Dielectric constant increases to a large value close to the Curie temperature. Above the Curie temperature, the Curie-Weiss law describes the temperature dependence of the dielectric constant for the ferroelectric materials which is proportional to $1/(T-T_c)$. When one plots ϵ_r versus T , ϵ_r rises anomalously near the T_c , as shown in Fig. 3.5. The effective dielectric coefficient shows pronounced dependencies on the applied electric field strength and stress intensity, due to variations in the ferroelectric domain wall contribution [62]. It is recognized in the earliest studies on ferroelectrics that the movement of

ferroelectric domain walls should make a significant contribution to the dielectric properties [63]. At the lower values of electric field, the reversible vibration of domain walls about an equilibrium position is expected to provide a significant contribution to the dielectric properties. Lewis has referred to the domain switching and domain wall vibration mechanisms as macrohysteresis and microhysteresis respectively [64]. Both extrinsic and intrinsic mechanisms contribute to the real 'in-phase' components of field induced strain and dielectric displacement, whereas the imaginary, lossy components are due to extrinsic mechanisms only. One can write the dielectric coefficient as [65], $\epsilon^* = \epsilon' - j\epsilon''$, where $\epsilon' = \epsilon'_{in} + \epsilon'_{ex}$ and $\epsilon'' = \epsilon''_{ex}$. Also "*" denotes a complex quantity and 'ex', "in" refer to extrinsic and intrinsic respectively.

Our group's research involves using ferroelectric materials made of STO and BST thin-films. Both these ferroelectric materials work slightly above the Curie temperature in paraelectric region. There is no spontaneous polarization and no hysteresis behavior in these ferroelectric materials. However, both these materials show high dielectric constant which depends on electric field and temperature. Fig. 3.6 describes the variation of the relative dielectric constant with temperature. From Fig. 3.6, one can see that at the Curie temperature, both ferroelectric materials show high dielectric constant. Fig. 3.7 shows the dielectric constant versus the applied electric field characteristics of ferroelectric STO.

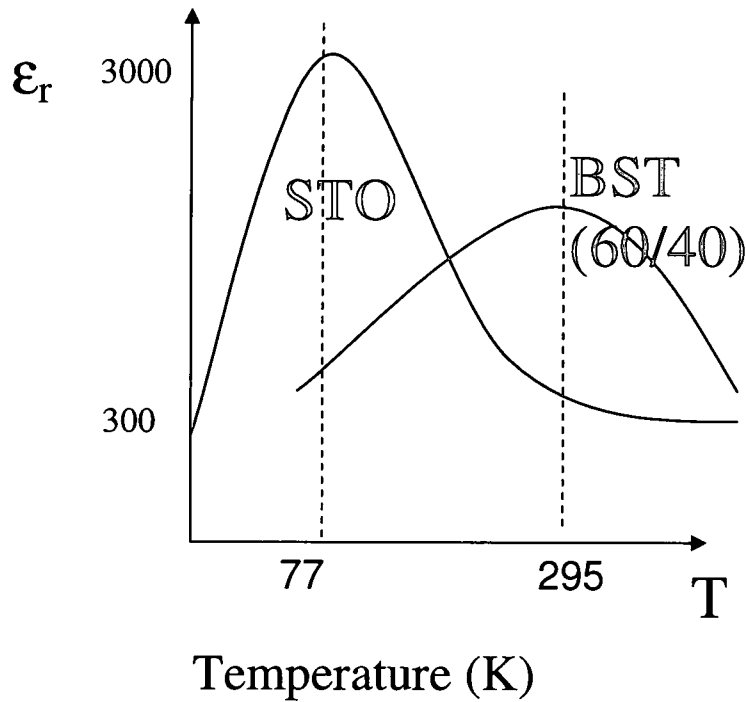


Fig. 3.6 : Relative dielectric constant versus temperature for the ferroelectric materials of STO and BST.

The value of the dielectric constant reduces with electric field due to the reorientation of the dipole moment of the ferroelectric materials. The higher the electric field, the lower is the dielectric constant (Fig. 3.7). The dielectric constant of ferroelectric materials depends on several factors such as composition ratio, processing temperature, pressure, and grain size. Recently, our group has investigated a nano-structured ferroelectric material made of BST thin-films [60/40 (Ba/Sr)] composition ratio. More than 4:1 dielectric tunability [30] has

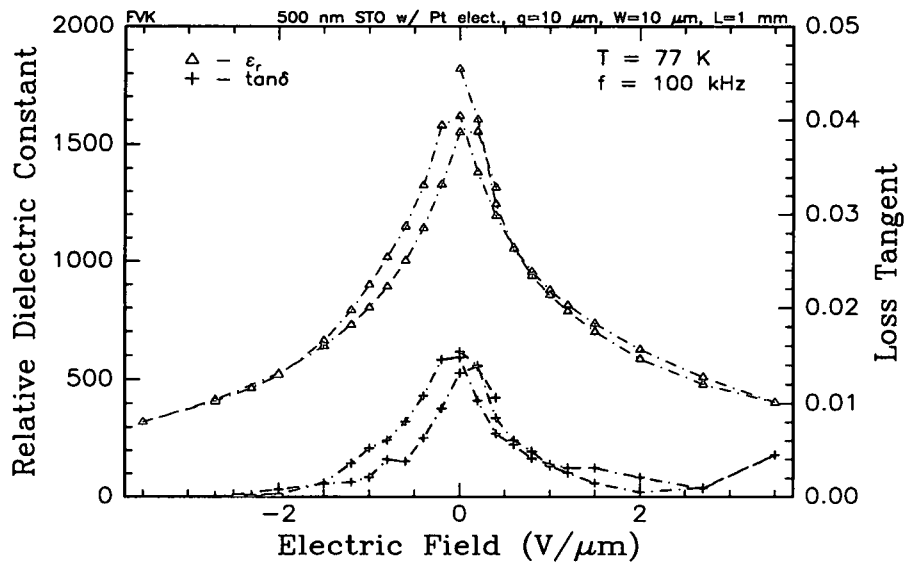


Fig. 3.7 : Relative dielectric constant versus electric field of the STO material.

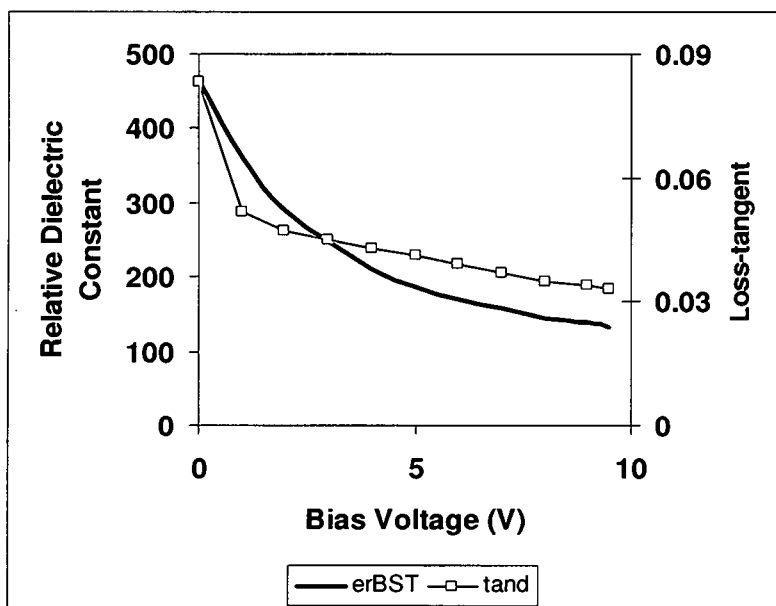


Fig. 3.8 : Variation of the relative dielectric constant, and loss tangent with the bias voltage for a nanostructured BST thin-films used in our study.

[30]been obtained in BST thin-films processed at 75 milli-Torr (mT) oxygen partial pressure and substrate temperature of approximately 700°C. Such films have an average grain size of 60nm [8]. Fig. 3.8 shows the variation of the dielectric constant and loss tangent of the nano-structured BST thin-films with biasing voltage. We see from Fig. 3.8 that a BST thin-film shows higher dielectric constant and loss tangent at zero bias, but the dielectric constant and the loss tangent reduce with higher bias voltage (~10V). Fig. 3.9 and Fig. 3.10 describe the Scanning Electron Microscope (SEM) picture of the BST thin-films on Si and LAO substrates respectively. From Fig. 3.9 and Fig. 3.10, one can see that grain size of the BST thin-films is small. But the larger the grain size, the higher is the dielectric constant [66].

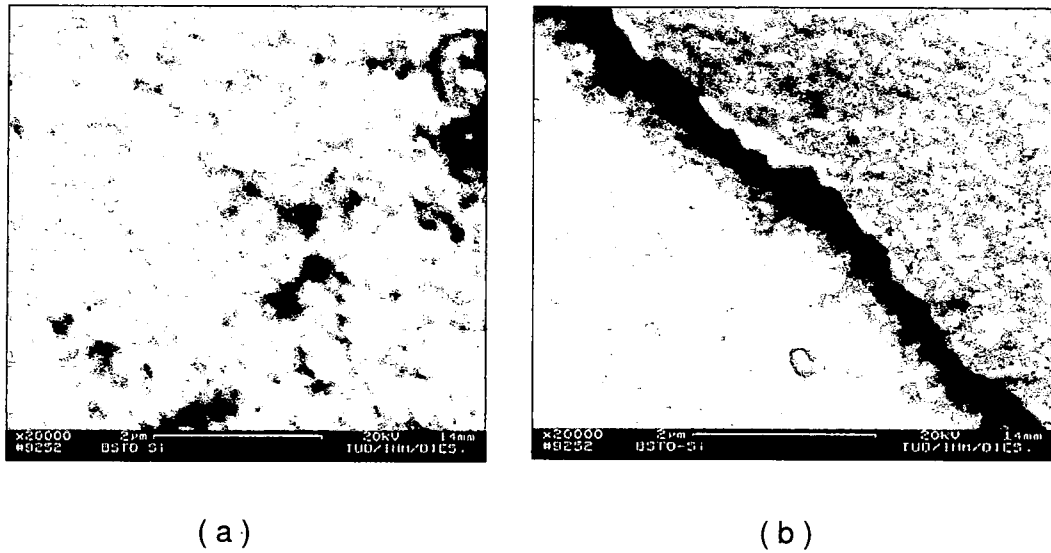
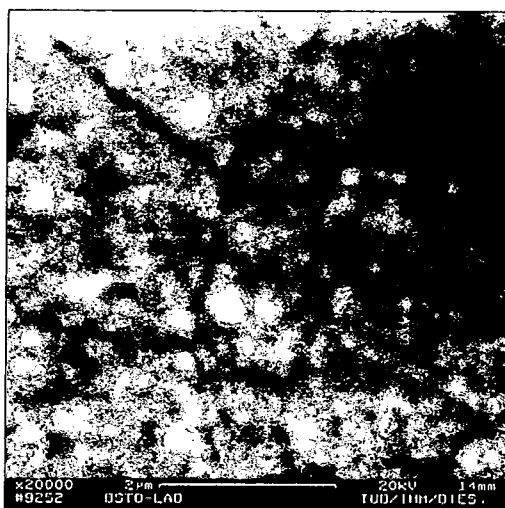
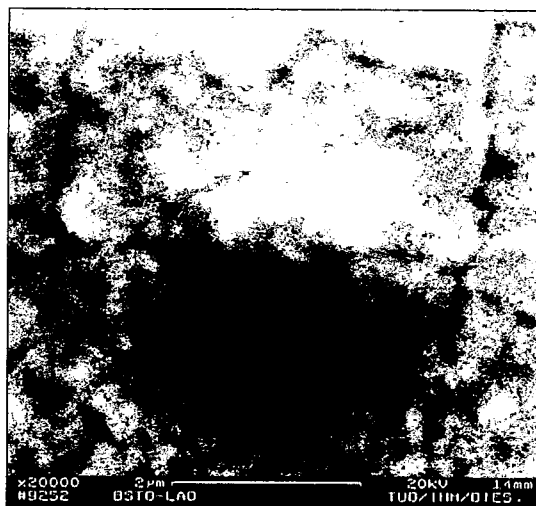


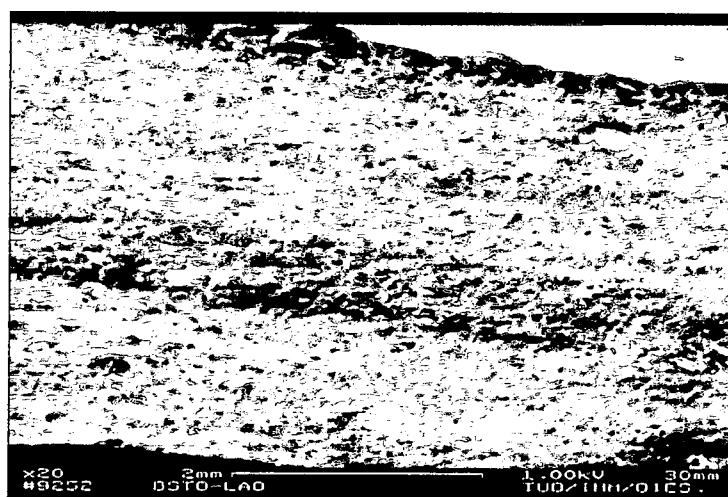
Fig. 3.9 : (a) Grain size, and (b) interface SEM micrograph for the BST thin-films on Si substrate.



(a)



(b)



(c)

Fig. 3.10 : (a) Grain size (b) surface and (c) cross-sectional SEM micrograph of the BST thin-films on LAO substrates.

CHAPTER IV

CAPACITIVE SHUNT RF MEMS SWITCH

4 Introduction

Microelectromechanical systems (MEMS) technology is expected to have a tremendous impact on the design of communication systems. MEMS is the integration of mechanical elements, sensors, actuators and electronics on a common silicon substrate through microfabrication technology. MEMS is an enabling technology allowing the development of smart products, augmenting the computational ability of microelectronics with the perception and control capabilities of microsensors and microactuators and expanding the space of possible designs and applications. With the recent progress of this technology, more and more attention has been focused on the development of MEMS devices for RF applications.

MEMS electrostatically actuated reflective switches have been recently demonstrated for low loss RF/Microwave and millimeterwave applications [67]-[70]. MEMS switches are composed of thin-metal bridge called membrane which can be electrostatically actuated to the RF signal line by applying a DC bias voltage.

Recently, MEMS technology has begun to be used in wireless communication systems to improve performance of existing devices based on structures or operational principles. RF MEMS systems and components can reduce the size and cost of the initial third-generation devices by increasing the level of integration and by creating possibilities for tuning and directing the components [16],[71]-[72].

MEMS is a new manufacturing technology, a way of making complex electromechanical systems using batch fabrication techniques similar to those used for integrated circuits, and uniting these electromechanical elements together with electronics. MEMS switches provide a solution that combines the performance of electromechanical relays with a dimension scale and cost structure of microelectronic devices. They offer great potential benefits over the conventional semiconductor switches such as PIN diode, and FETs. These switches provide low insertion loss ($<1\text{dB}$), high isolation ($>30\text{dB}$), extremely low power consumption, excellent linearity ($\text{IP}_3 >66\text{dBm}$), lack of intermodulation distortion, high breakdown voltage, compactness and high levels of integration capability [15]-[21],[26]-[27],[67],[73]-[77]. However, RF MEMS switches also have several limitations such as low speed, low power handling capability, low mechanical lifetime, high actuation voltage, low reliability, high packaging cost, and fabrication complexity. The potential applications of the RF MEMS switches include varactors, phase shifters, voltage control oscillators (VCOs), tunable

filters, and reconfigurable antennas, RF MEMS switches could also be used as a matching network [78].

4.1 Device structure and description of the switch

Shunt capacitive RF MEMS switch is designed on multilayer substrates with a coplanar waveguide (CPW) transmission line configuration. Fig. 4.1 describes the top view and cross sectional view of the capacitive shunt RF MEMS switches. The switch consists of a thin metal membrane “bridge” suspended over the center conductor at both ends to the ground conductors of the CPW line (Fig. 4.2 and Fig. 4.3). Aluminum (Al) is used as a metal membrane because of low resistivity, good stability, and efficiency in RF signal propagation. In this design, a tunable ferroelectric materials of BST thin-film with a high dielectric constant ($\epsilon_r \geq 200$) is used as a dielectric layer (500nm thickness) on top of the center conductor of the CPW line to isolate the switch from the suspended metal membrane. By using conformal mapping technique [79]-[97], a characteristic impedance (Z_0) of the CPW line has been taken approximately 50Ω to reduce the line loss with dimensions of Ground-Signal-Ground (150/50/150 μm) for DC-20 GHz measurements. The RF MEMS switch is designed on a high resistivity silicon substrate ($>6\text{K}\Omega\text{-cm}$). The spacing (S) between the center and ground conductors is taken 50 μm with a geometric ratio ($k=W/(W+2S)$) is equal to 0.333 of the CPW line. The thickness of the substrate (Si) and SiO_2 layer is taken 500 μm and 0.3 μm respectively.

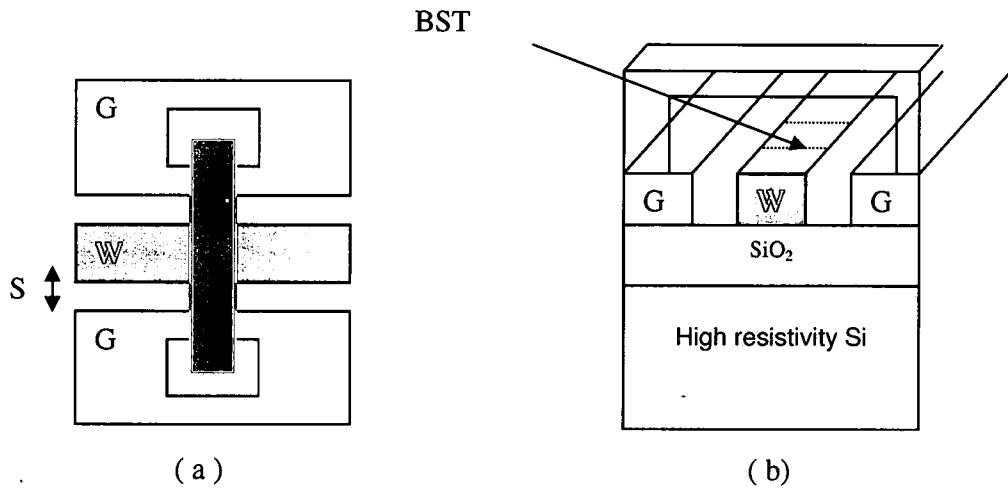


Fig. 4.1 : (a) Top view and (b) Cross sectional view of the capacitive shunt RF MEMS switch.

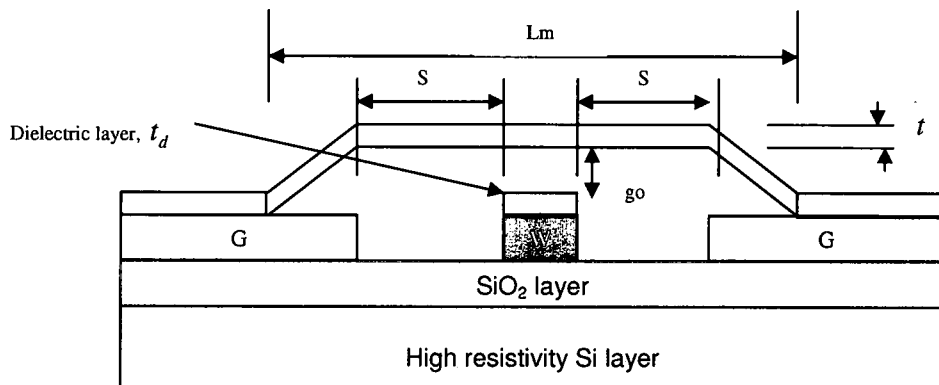


Fig. 4.2 : Physical modeling (ON state) of the RF MEMS shunt capacitive switch, where L_m =switch length, t_d =dielectric thickness, t =bridge conductor's thickness, S =spacing between the center and ground conductor, W =width of the center conductor, G =width of the ground conductor, and g_0 =air gap.

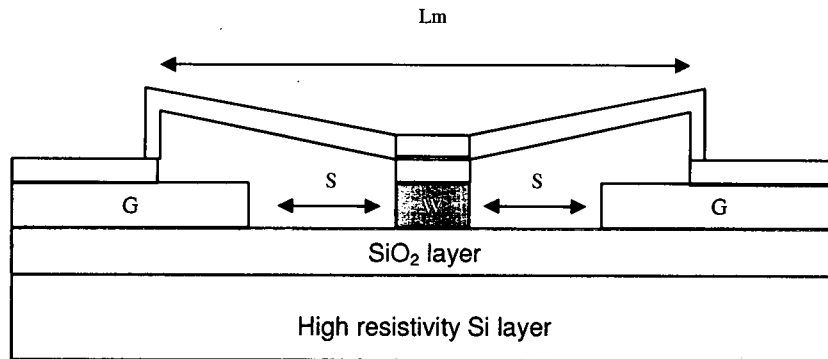


Fig. 4.3 : Physical modeling (OFF state) of the RF MEMS capacitive shunt switch.

4.2 Theory of operation

Fig. 4.2 and Fig. 4.3 describe the shunt capacitive RF MEMS switches in the ON (up) and OFF (down) states respectively. The dielectric constant of the BST thin-films is assumed to be 300 at zero-bias. Without applying a bias voltage between the suspended metal membrane and center conductor of the CPW line, a very small capacitance exists and due to the residual tensile stress keeps the suspended membrane above the RF signal path called the “up” state position of the switch (reference to Fig. 4.2). The capacitance between two electrodes in the “up” state position is named the up state capacitance (C_u) and it is very small. In that case, most of the RF signal passes through from input to the output ports of the CPW signal line. By applying a dc voltage between the membrane and the center conductor of the CPW line, an electrostatic force is created to pull the membrane down onto the dielectric film on top of the bottom electrode, forming the low impedance RF path to ground and reducing the dielectric constant of

ferroelectric materials of the BST thin-films [12]-[13],[98] from 300 to 200 , the position of the switch is called “down” state (Fig. 4.3) and the capacitance is named the “down” state capacitance (C_d) which is very high. The increased capacitance in the down state or the blocking state of the switch couples the signal to ground and thus blocks the RF signal from passing through to the output side of the signal line. The stress level within the membrane film can also affect the performance of the switch. A low-tensile material can increase the pull – down voltage, while compressive-stressed material may cause the membrane to buckle [18]. The ratio of C_d/C_u is the most important parameter to obtain the better performance (high isolation and low insertion loss) of shunt capacitive RF MEMS switches. The higher the ratio, the better is the performance. Switch performance also depends on the surface roughness of the dielectric layer and it should be $<5\text{nm}$ [16]. This current design demonstrates how to obtain the higher C_d/C_u ratio by using the high dielectric constant of the ferroelectric materials of BST thin-films to achieve the higher performance of the shunt capacitive RF MEMS switches.

4.3 Optimization of the switch parameters

The switch parameters are optimized by the numerical analysis. The characteristic impedance of the CPW line is determined by using the conformal mapping technique. Since the characteristic impedance of the CPW line is taken as 50Ω to reduce the losses, so, therefore, an optimization is required for the width of the center conductor and the spacing between the center and the ground

conductors of the CPW line. The ratio between the width of the center conductor and the spacing between the ground conductors is denoted by k , mathematically we can write,

$$k = \frac{W}{W + 2S} \quad (4.1)$$

where W is the width of the center conductor and S is the spacing between the center and the ground conductors. By using the conformal mapping technique, a characteristic impedance of the multilayer CPW line is determined. From Fig. 4.4, one can see that Z_0 of the CPW line varies with the geometric ratio of k which is directly dependent on the geometric dimensions of the CPW line. The higher the value of k , the lower the characteristic impedance of the CPW line. One can easily get any value of the characteristic impedance by changing these two parameters. In this design, both W and S are taken $50\mu\text{m}$ to get the Z_0 approximately 50Ω . So, the ratio of k is 0.333 and from Fig. 4.4, one can also see that the value of k is approximately 0.333 for 50Ω of the multilayer CPW transmission line.

In the switch perspective, the important design parameter is the air gap (g_0) between the suspended metal membrane and top of the center conductor. In order to keep the actuation voltage minimum, a small air gap is required. The actuation voltage of the switch is described by [19]

$$V_p = \sqrt{\frac{8K_s}{27\epsilon_0 A}} g_0^3 \quad (4.2)$$

where K_s is the spring constant of the membrane, A is the contact area of the switch, ϵ_0 is the permittivity of the free space, and g_0 is the height of the air gap.

Notice that the pull down voltage is independent of the switch width.

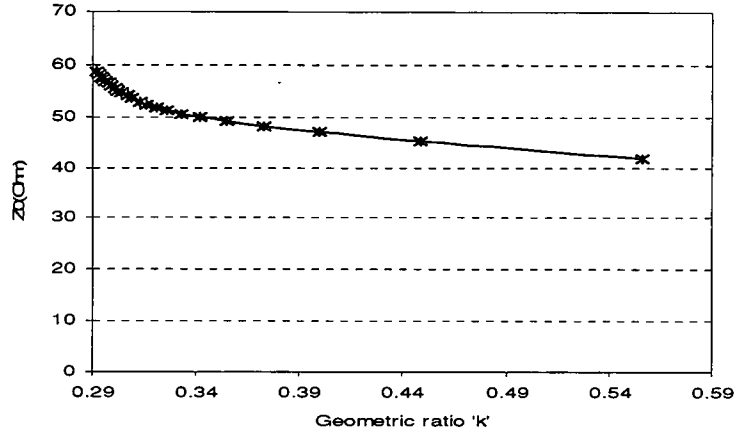


Fig. 4.4 : Variation of the characteristics impedance (Z_0) with k of the CPW transmission line on multilayer substrates.

The spring constant, K_s of the metal membrane can be approximated by [17]

$$K_s = \frac{32Et^3w}{L_m^3} + \frac{8\sigma(1-\nu)tw}{L_m} \quad (4.3)$$

where E is Young's modulus of the membrane metal, L_m is the switch length, t is the thickness of the Al metal membrane, w is the width of the membrane, σ is the residual tensile stress in the membrane, and ν is the Poisson's ratio for the membrane material. In this design, the actuation voltage has been obtained 13-37V with $E=70\text{GPa}$, $g_0=2.5\mu\text{m}$, $W=50\mu\text{m}$, $w=50\mu\text{m}$, $L_m=300\mu\text{m}$, $\sigma=0$ and 11MPa , $\nu = 0.31$, and $t=0.815\mu\text{m}$. From Eq. (4.2), one can see that the actuation voltage is directly proportional to the air gap and minimum air gap gives a minimum

voltage but we can't take it as small as possible because g_0 is also related to the characteristic impedance of the CPW line. An optimized air gap of $2.5\mu\text{m}$ is taken for this design to obtain the minimum actuation voltage and also the required characteristic impedance.

The ratio between C_d and C_u is a key parameter of the capacitive shunt RF MEMS switches for determining both insertion loss and isolation. A small C_u is required for maintaining low insertion loss in the ON state of the switch. Large air gap between the membrane and bottom electrode creates smaller capacitance with the disadvantage of high pull down voltage. An optimization is required of the air gap to get the optimum capacitance and minimum pull down voltage. A large C_d is required to maintain high isolation that requires an intimate contact between the membrane and the dielectric thin films over the bottom electrode in the OFF or down state of the switch.

The up state and down state switch capacitances are expressed as follows;

$$C_u = \frac{\epsilon_0 A}{g_0 + \frac{t_d}{\epsilon_r} + C_f} \quad (4.4)$$

$$C_d = \frac{\epsilon_0 \epsilon_r A}{t_d} \quad (4.5)$$

where ϵ_0 is the permittivity of the free space, ϵ_r is the relative dielectric constant of the BST thin-films, A is the contact area of the switch, g_0 is the air gap between the metal membrane and the top of the center conductor, t_d is the

thickness of the dielectric layer, and C_f is the fringing capacitance. From equations (4.4) and (4.5), we see that the value of C_d and C_u depends on the value of dielectric constant and its thickness. To get the higher value of C_d , a higher value of ϵ_r is required or lower value of t_d . A minimum t_d is required for the dielectric thin-films to withstand large bias voltage. So, therefore, an optimization is required between ϵ_r and t_d to get the higher C_d/C_u , resulting in lower insertion loss and higher isolation of the capacitive shunt RF MEMS switches. The value of C_d also depends on the surface roughness of the dielectric layer and it should be very low, e.g. $\leq 5\text{nm}$ [20]. Fig. 4.5 shows how the ratio of C_d/C_u changes with ϵ_r and t_d of BST material for the fixed value of k and g_0 of the switch.

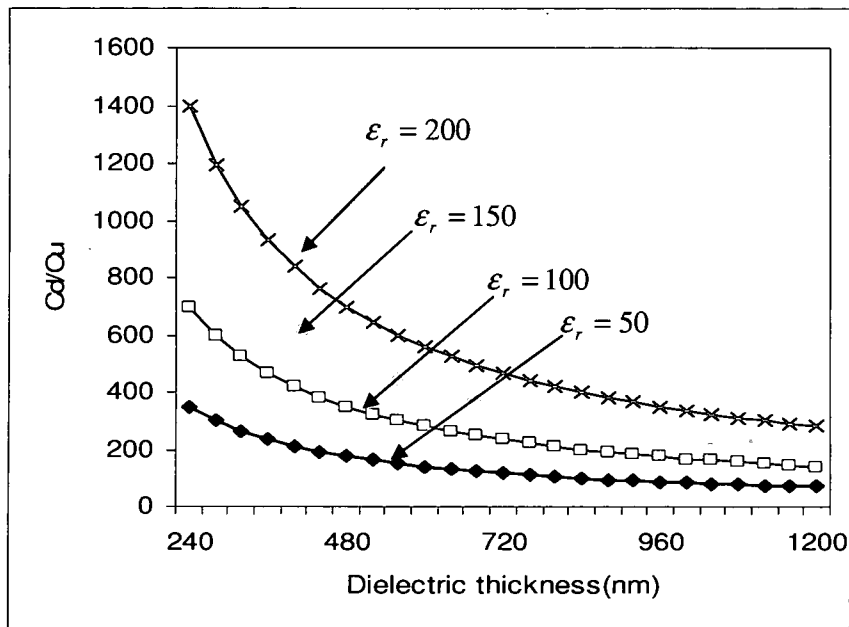


Fig. 4.5 : Variation of the C_d/C_u with t_d and ϵ_r of the ferroelectric material of BST thin-films for the fixed value of g_0 , and k .

4.4 Electrical model of the capacitive shunt RF MEMS switch

Capacitive shunt RF MEMS switch is modeled by two short sections of the transmission line and a lumped RLC model of the suspended metal bridge with the capacitance (C_d or C_u) depending on the position of the switch. The electrical modeling both in the ON and OFF states of the capacitive shunt RF MEMS switch is shown in Fig. 4.6 describing in Fig. 4.2 and Fig. 4.3 respectively.

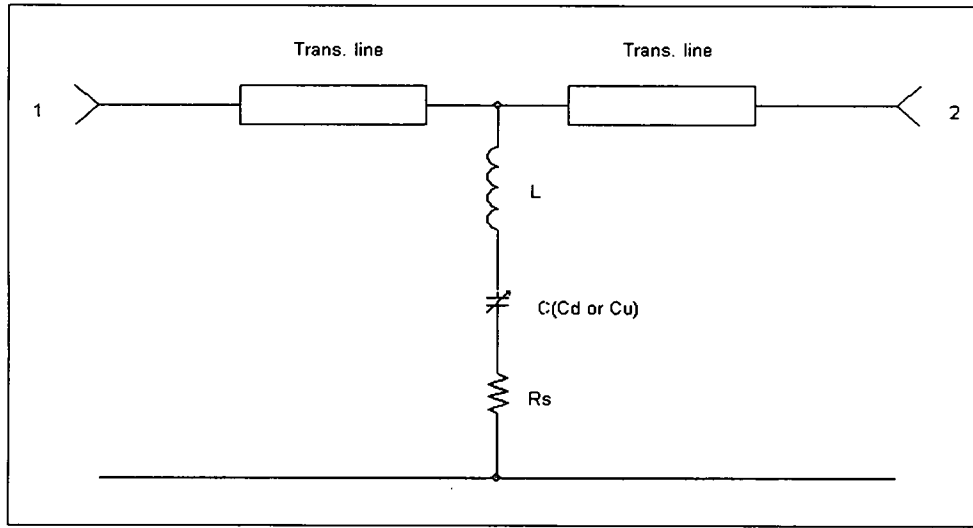


Fig. 4.6 : Equivalent electrical model of the capacitive shunt RF MEMS switch both in the ON and OFF states of the switches described in Fig. 4.2 and Fig. 4.3 respectively.

The per unit resistance, inductance and capacitance of the transmission line have been calculated by [97],

$$R = \frac{1}{W\sigma_m\delta_s\left\{1 - \exp\left(-\frac{t}{\delta_s}\right)\right\}} \quad (4.6)$$

where R is the per unit resistance, δ_s is the skin depth, W is the width of the center conductor, σ_m is the conductivity of the conductor material (Gold), and t is the thickness of the conductor.

And

$$L = \mu_0 \frac{K(k_L)}{K(k'_L)} \quad (4.7)$$

where $\frac{K(k_L)}{K(k'_L)}$ is the elliptical function, L is the per unit inductance, μ_0 is the permeability of the air, k_L is the modulus of the complete elliptic integrals, and is defined;

$$k_L = \frac{S/2 + \delta_s}{W + S/2 - \delta_s} \quad (4.8)$$

where S is the spacing between the center and the ground conductors, and δ_s is the skin depth of the transmission line. By using Eqs. (4.6) and (4.7), per unit inductance and resistance of the transmission line have been calculated and found 0.801nH/mm, 1.016Ω/mm at 20 GHz.

And also

$$C = \epsilon_0 \epsilon_f \frac{K(k'_0)}{K(k_0)} \quad (4.9)$$

Where C is the per unit capacitance, ϵ_0 is the air permittivity, ϵ_f is the effective permittivity of the device, and k_0 is the modulus of the complete elliptic integrals.

The up state (C_u) and the down state (C_d) capacitances have been calculated by numerically using Eqs. (4.4) and (4.5) and found 0.01332pF and 13.281pF with the dielectric thickness 500nm and dielectric constant 300 (up state) and 200 (down state). The series resistance of the metal bridge is expressed by [99]

$$R_s = \frac{1}{\sigma_{Al} w T} \quad (4.10)$$

where R_s is per unit resistance of the metal bridge, w is the width of the bridge, σ_{Al} is the conductivity of aluminum metal, and T is thickness of the metal bridge. The value of R_s has been found 0.606Ω/mm at 20GHz for $w = 75\mu m$, and $T = 0.576\mu m$. The per unit bridge inductance can be expressed as;

$$L = \frac{\mu_0 h}{w} \quad (4.11)$$

where μ_0 is the permeability of vacuum, h is the distance between the metal bridge and ground conductor of the CPW line and w is the width of the bridge. The inductance of 0.041nH/mm has been found for $h = 2.5\mu m$ and $w = 75\mu m$ of the metal bridge.

4.5 Discussion of the simulation results

The dielectric constant (ϵ_r) of BST thin-films is reduced [12]-[13],[98] by applying a bias. In this design, ϵ_r is taken 300 at zero bias voltage (ON state) and reduced to 200 by applying a bias (13–37V) between the metal bridge and the center conductor of the CPW line, resulting the switch is in the down (OFF) state position. Small up state capacitance (C_u) is expected to pass the signal and high

down state capacitance (C_d) is required to block the signal as much as possible. The value of C_u and C_d depends on the overlap area (A) between the bridge and center conductor of the transmission line, height of the air gap (g_0), dielectric thickness (t_d), and ϵ_r of the BST thin-films. Since A , t_d and g_0 are fixed for a particular design. So, therefore, only ϵ_r of the ferroelectric material is the most important parameter for obtaining the capacitance in both positions of the switch. Fig. 4.7 shows how Z_0 and C_d change with ϵ_r for the fixed overlap area, t_d , and g_0 . For the fixed geometric ratio (k) of the transmission line, characteristic impedance (Z_0) of the CPW line reduces with increasing ϵ_r because of increasing the effective dielectric constant of the device. Since air gap (g_0) is a constant in this design, so, therefore, the actuation voltage (V_p) and up state capacitance (C_u) are also constant.

Simulation results (see Fig. 4.8) describe both physical and electrical modeling of the RF capacitive shunt MEMS switches. Simulated isolations both in physical and electrical modeling have been obtained -35dB at 20 GHz. From the simulation results (reference to Fig. 4.8), one can see that both the cases (physical and electrical modeling) the resonance occurs at 40 GHz. Fig. 4.8 also indicates that a small variation exists in the isolations between the physical and electrical modeling due to fringing effect on the physical design. Simulated insertion losses (S_{21}) both in physical and electrical modeling in the ON state of the switches have been found -0.027dB and -0.21dB (ref. to Fig. 4.8) respectively

at 20 GHz. The performance of the RF MEMS switch can be improved by using BST thin-films as a dielectric layer instead of using Si_3N_4 [26][28]. By using BST

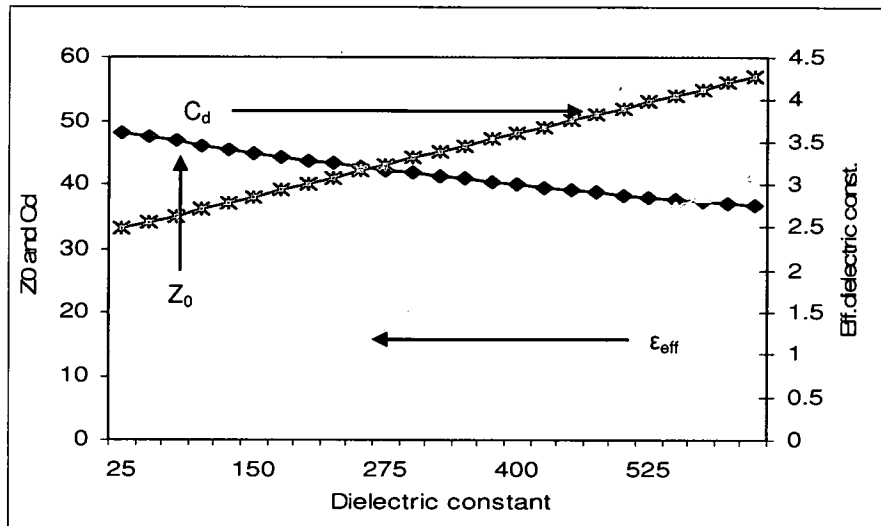


Fig. 4.7 : Variation of the switch parameters with the dielectric constant of the BST thin-films.

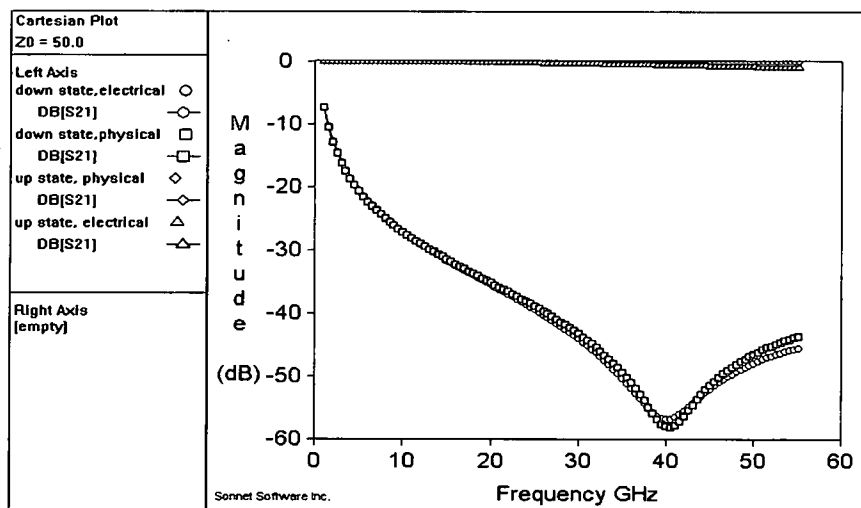


Fig. 4.8 : Simulated S-parameters both physical (see Fig. 4.2 and Fig. 4.3) and electrical modeling (see Fig. 4.6) for OFF and ON state of the capacitive shunt RF MEMS switches.

Si_3N_4 [26][28]. By using BST thin-films, isolation can be improved at least more than 10 dB in the OFF state of the switches. From simulation results in Fig. 4.9, we see that BST thin-films gives the higher isolation than Si_3N_4 as a dielectric layer in the OFF state of the shunt RF MEMS switches but the insertion loss doesn't change that much in the ON state of the switches.

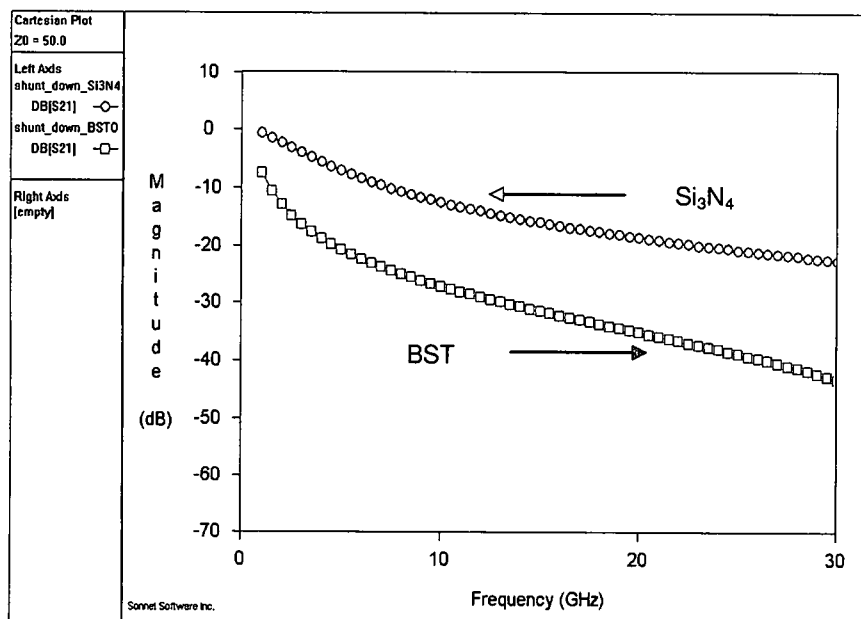


Fig. 4.9 : Compared simulated isolation using the BST thin-films and Si_3N_4 as a dielectric layer in the OFF state of the RF MEMS switches.

CHAPTER V

FERROELECTRIC BASED CAPACITIVE SHUNT SWITCH

5 Introduction

A ferroelectric thin-film based capacitive shunt switch will be used as a potential replacement for RF MEMS switches in RF/microwave applications. The novelty in the implementation comes from the elimination of any moving parts (as in RF MEMS switches) for switching [12]. The implementation of a capacitive shunt switch is based on a coplanar waveguide (CPW) transmission line shunted by a ferroelectric varactor. High-K tunable microwave dielectrics such as BST are gaining acceptance in microwave integrated circuits due to the large need for tunable/reconfigurable circuits [9],[31],[34],[49]. Semiconductor varactors are good competitors to ferroelectric varactors in the frequency band below 10 GHz [8]. The quality factor of semiconductor varactors drastically degrades above 10GHz but varactors-based on ferroelectrics have high quality factor throughout the millimeterwave frequency band [8],[99]. The characteristics of ferroelectric varactors based devices include fast switching speed, ease of integration with Si MMICs, and have reasonable Qs at microwave and millimeterwave frequencies [8],[99].

Recently, our group demonstrated a new varactor capacitive shunt switch based on the dielectric tunability of BST thin-films [8],[12],[13],[29]-[31],[39]. The concept of switching ON and OFF is based on the field-dependent dielectric permittivity of the ferroelectric material of BST thin-films [12]. Without applying a bias voltage between the ground and signal conductors of the CPW line, the dielectric constant of the BST thin-film is shown high (~ 500), resulting in a high varactor capacitance. As a result, most of the rf signal is bypassed from the signal line to the ground conductors and the switch is in the OFF state [13]. By applying a DC voltage (~ 10 V) between the ground and signal conductors of the CPW line, the dielectric constant of the BST thin-films reduces from 500 to 120, resulting in a low varactor capacitance. In this case, most of the rf signal is allowed to pass through from the input to the output port of the transmission line, resulting in the switch ON state [13]. The performance in the ON and OFF states of the device depends not only on the dielectric tunability of the BST thin-films but also on the varactor overlap area. The higher the overlap area, the better is the performance in the OFF state of the device at the expense of high loss in the ON state.

This section describes the details of the varactor-based capacitive shunt switch. The theory of operation, design, simulation, modeling, theoretical analysis, optimization, fabrication, and experimental results of the capacitive shunt switch are presented and discussed. This section also contains possible applications and future research using this device in RF/Microwave applications.

5.1 Device structure

The ferroelectric varactor-based capacitive shunt switch is designed on the multilayer substrates with a CPW transmission line configuration. High resistivity Si ($>6\text{k}\Omega\text{-cm}$) is used as the substrate to reduce the losses for high frequency applications. A thin layer of SiO_2 is used as an isolation layer between the bottom conductor and substrate. The thickness of the substrate and SiO_2 layer is taken to be $500\mu\text{m}$ and $0.3\mu\text{m}$ respectively. Fig. 5.1 shows the cross sectional view of

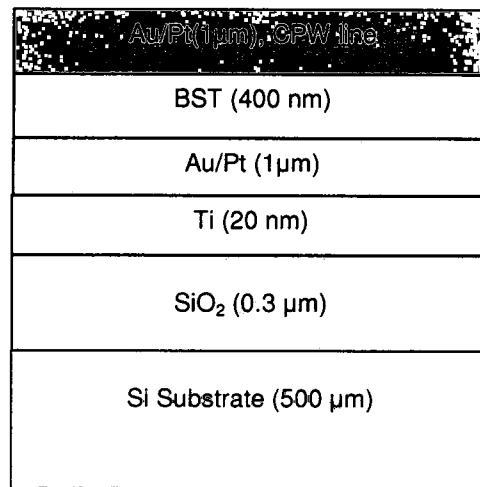


Fig. 5.1 : Cross sectional view of different layers of the capacitive shunt switch.

the ferroelectric varactor-based capacitive shunt switch. A very thin layer of Ti (20 nm) is used as an adhesion layer to increase the adhesion of the bottom metal (Gold). This switch consists of two metal layers. The top metal layer (metal 2) is used as a regular CPW transmission line (Ground/Signal/Ground) configuration but the bottom metal layer (metal 1) uses only the ground lines and

a shunt line between the the grounds of the bottom metal layer. Fig. 5.2 and Fig. 5.3 show the top and bottom metal structure of the capacitive shunt switch. From

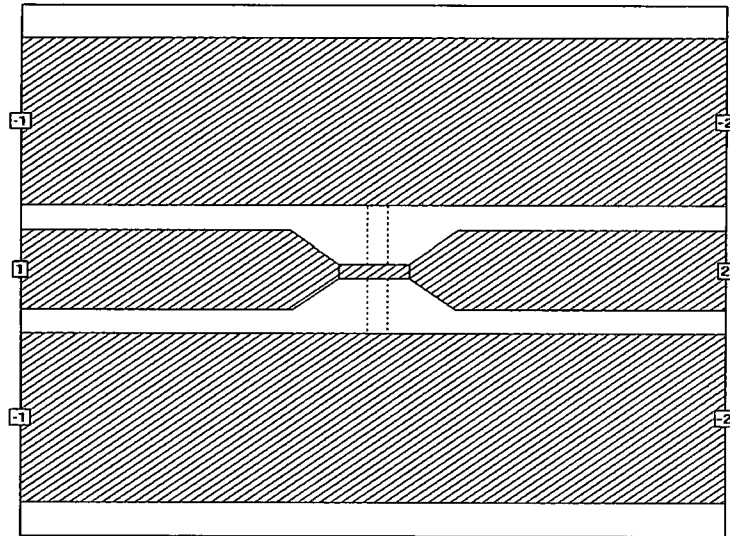


Fig. 5.2 : Top metal pattern (metal 2) of the capacitive shunt switch showing the ground/signal/ground for the regular CPW line configuration.

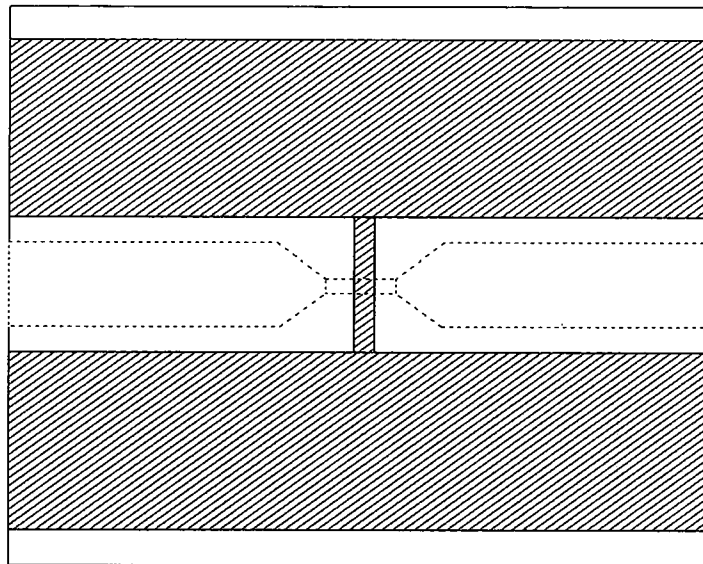


Fig. 5.3 : Bottom metal pattern (metal 1) of the capacitive shunt switch showing the two ground lines and a shunt line between the ground lines.

Fig. 5.2, we can see that the top metal layer consists of ground/signal/ground pattern of the CPW line but in Fig. 5.3, we see that the bottom metal layer consists of two ground lines with exactly the same dimension as the CPW ground lines of top layer and a shunt line between two grounds. The ferroelectric material of BST thin-film is deposited on the entire surface of the bottom metals. The thickness of the BST thin films is taken as 400 nm for all of the devices. A thin Pt metal layer (~100nm thickness) is used with Au to improve the interface between the BST thin-film and metal layers.

5.2 Fabrication Process

The ferroelectric varactor-based capacitive shunt switch requires two metal layer processes. The bottom and top metal layers are known as metal1 and metal2 layers respectively. Standard positive photoresist lift-off photolithography is used for the metal1 layer with a Ti adhesion layer (20 nm) deposited first, followed by the gold (~800 nm) and Pt (100 nm) in an electron-beam evaporation system [31]. After the bottom metal layer is defined, the $\text{Ba}_{0.6}\text{Sr}_{0.4}\text{TiO}_3$ (BST) thin-film is deposited on the entire surface using pulse-laser deposition (PLD) process. After the BST thin-film deposition, metal2 layer (10 nm Ti + ~1 μm Au) [8] is defined and processed using the positive photoresist lift-off process to complete the device fabrication. Fig. 5.4 shows the fabrication process for the capacitive shunt switch to deposit the metal layer pattern and BST thin film [8]. Fig. 5.5

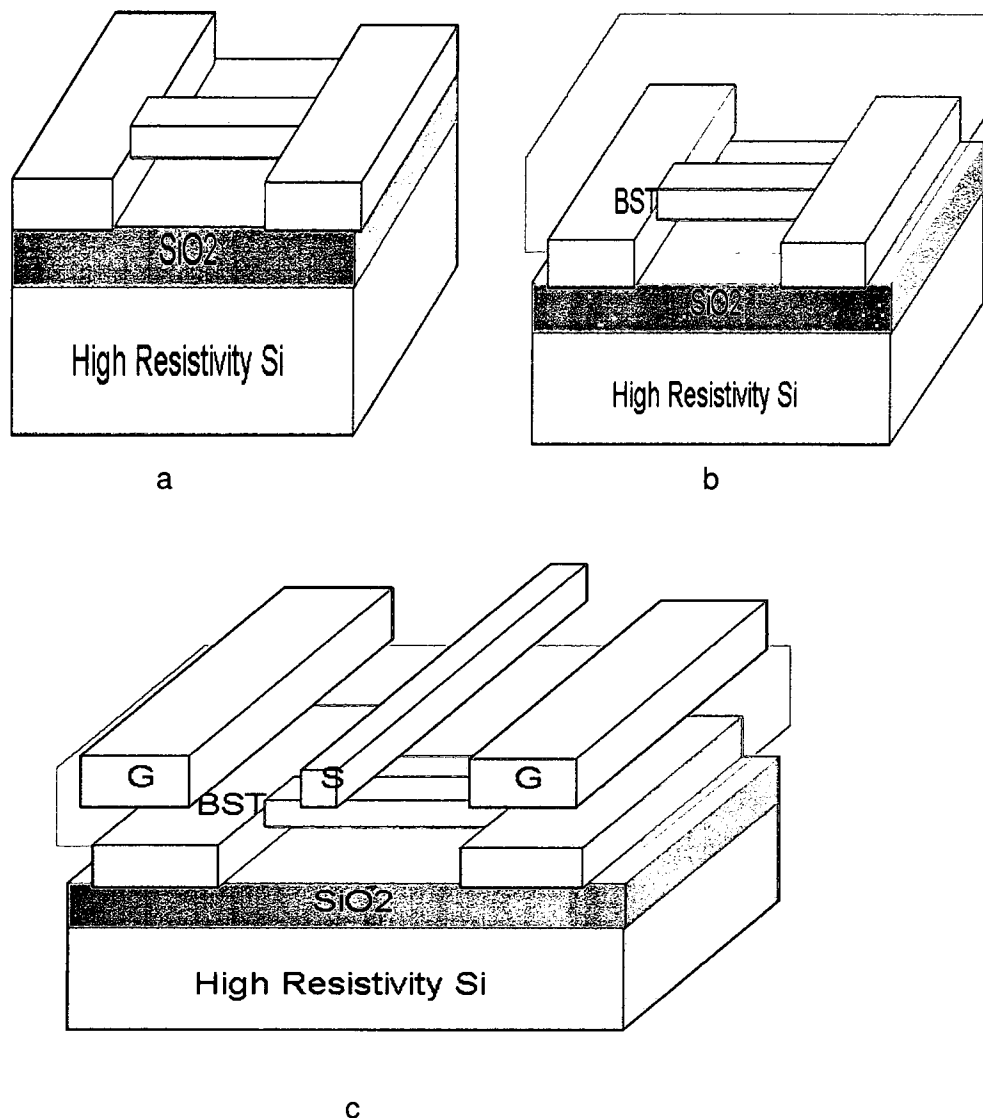


Fig. 5.4 : Fabrication process for the capacitive shunt switch outlined in process steps a through c. Step a shows metal1 pattern. Step b shows the entire sample coated with BST thin-film, and step c final device structure.

Table 1 : Process steps of the positive photoresist lift-off photolithography process Au or Au+PT. Starting from high resistivity Si/SiO₂ substrates

No.	Process Step	Time	Status
1	1:10 BOE:DI H ₂ O solution	30 secs	
2	DI rinse wafers (3 or 4 rinses)		
3	Prebake wafers @ 110 C on the hotplate	1 min	
4	Degreasing in Acetone and IPA (spin+spray)	30 Secs	
5	PMGI SF-11 spin coat @4000 rpm, ramp at 200 (~1 µm thick) Remove edge-bead with nanoEBR	30 secs	
6	Bake at 270 C on the hot-plate	2 mins	
7	Spin-coat S1813 photoresist @4000 rpm, ramp at 200 (~2 µm) Remove edge-bead with acetone	30 secs	
8	Bake at 110 C on the hot-plate	1 min	
9	Align and expose in MJB3	12 secs	
10	Develop in AZ351 developer solution followed by DI spray And blow dry in N2 (examine pattern)	30 secs	
11	Deep UV exposure	200 secs	
12	Develop in SAL101 solution followed by DI rinse and N2 blow Dry (examine pattern)	2 mins	
13	Plasma ash in O2 plasma	4-8 mins	
14	Pre-metal etch (BOE solution, 1:10 with DI H2O)	30 secs	N/A
15	Metallization (e-beam), Ti: 20 nm, Pt: 200 nm, Au: 800 nm		
16	Lift-off step 1: Soak in acetone for ~ 5 mins. Spin+spray acetone, followed by IPA to remove residue (examine pattern)		
17	Lift-off step 2: Soak in 1165 solution @90C	2 mins	
18	DI rinse in the rinse station, blow dry in N2 (examine pattern)	4 cycles	
19	Plasma Ash in oxygen plasma	2-4 mins	
20	Examine pattern under the microscope		

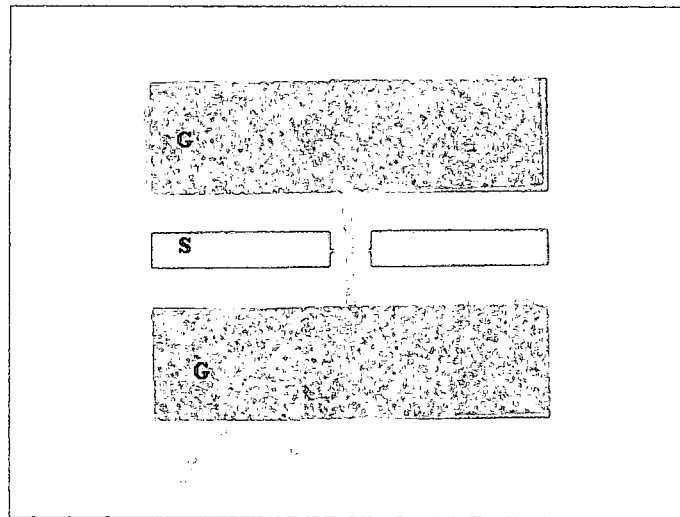


Fig. 5.5 : Photograph of a fabricated varactor shunt switch on a high resistivity Si substrate. The photograph clearly shows the two metal layers.

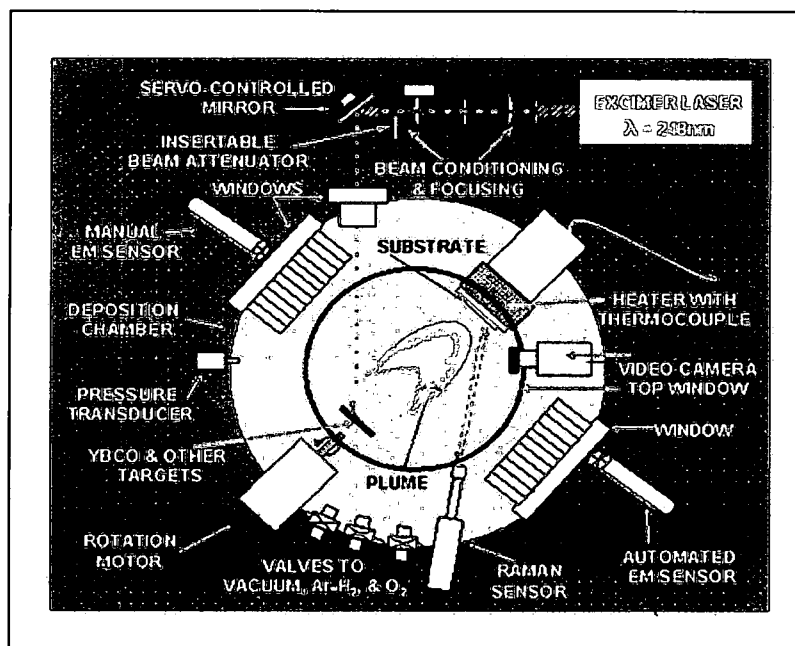


Fig. 5.6 : Automated in- situ, real-time, process-control pulse laser deposition system. Real-time control based on feedback from emission spectra (ES).

shows the photograph of a fabricated shunt switch on a high resistivity Si substrate. In Fig. 5.5, G, S, and G stand for Ground-Signal-Ground of the CPW in metal2. The fabricated switch (Fig. 5.5) clearly shows the two metal layers, with the bright one the top metal layer (metal2) and the slightly darker one of the bottom metal layer (metal1). Table 1 shows the processing steps of the standard positive photoresist lift-off process to deposit the metal layers pattern of the varactor-based capacitive shunt switch.

Pulsed Laser Deposition (PLD), a synthesis technique, is utilized to engineer the size of nanoparticles/grains and nanocluster formation in thin ferroelectric films [102]-[105]. The BST thin-film is deposited using a process controlled PLD system, for obtaining nano-structured BST thin-films with low microwave loss and large dielectric tunability [101]. Fig. 5.6 shows the BST deposition process. In PLD process, one can control precisely the film growth by controlling the energy density of the laser pulses, wavelength, oxygen partial pressure, the substrate temperature, grain size, and distance between the target and the substrate. Fig. 5.7 shows the schematic diagram of the PLD chamber. Fig. 5.8 shows the hierarchical process model using a pulse laser deposition system. The average grain size of the film is controllable from ~20nm to ~150nm without any clustering by increasing the oxygen ambient pressure from 38mT to 150mT [39]. The BST thin-film used in this study has been deposited at 75 mT oxygen partial pressure resulting an average grain size of 60 nm [8] and the processing temperature is approximately 750⁰C. Detailed deposition process of the nano-structured BST

thin-films using a PLD system is described elsewhere [101]. The sample size is typically limited to 1"×1", which is a major drawback using the PLD system.

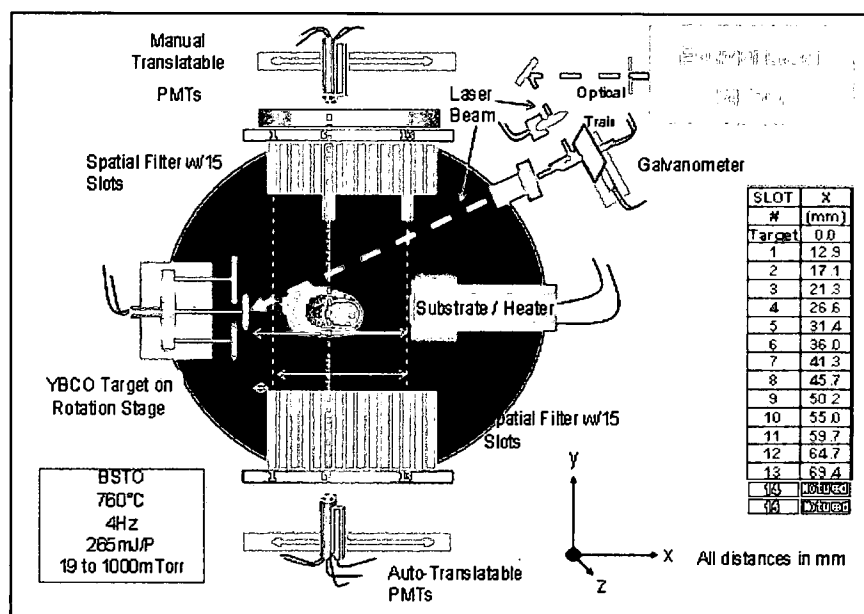


Fig. 5.7 : The schematic diagram of the PLD chamber.

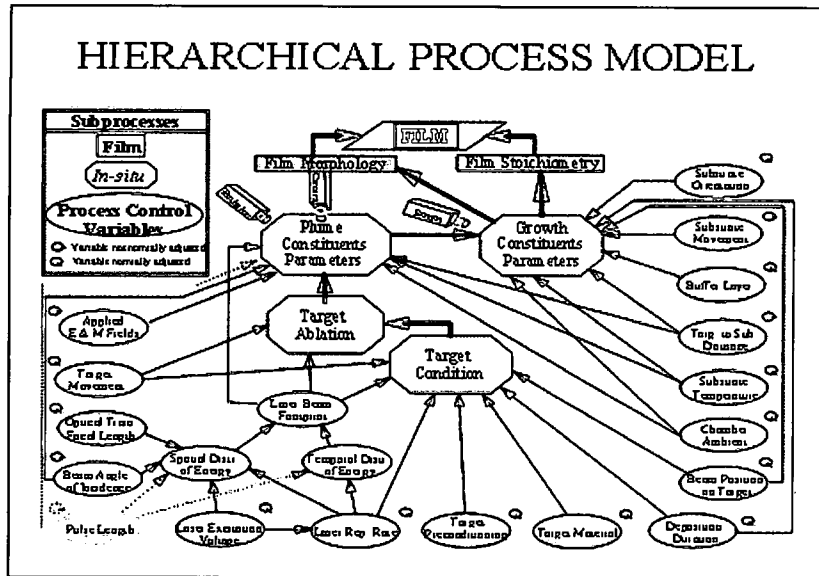


Fig. 5.8 : Hierarchical process model showing the process control variables and their complex interactions with a PLD system [101].

5.3 Design

The dimension of the ground-signal-ground conductors of the CPW line is taken as $150\mu\text{m}/50\mu\text{m}/150\mu\text{m}$ to obtain a characteristic impedance of approximately 50Ω over the range of the dielectric tunability. The spacing between the center and ground conductors of the CPW line is taken as $50\mu\text{m}$. The geometric ratio ($k=W/(W+2S)$) of the CPW line is equal to 0.333, where W and S are the width of the center conductor and spacing between the center and ground conductors respectively. The characteristic impedance of the CPW line is determined by using the conformal mapping technique [79]-[97] of the multilayer substrates.

The overlap area of the narrow region of the center conductor in metal2 and the connecting line between the ground conductors in metal1 defines the varactor area. Fig. 5.9 shows the different metal layer structures and the final

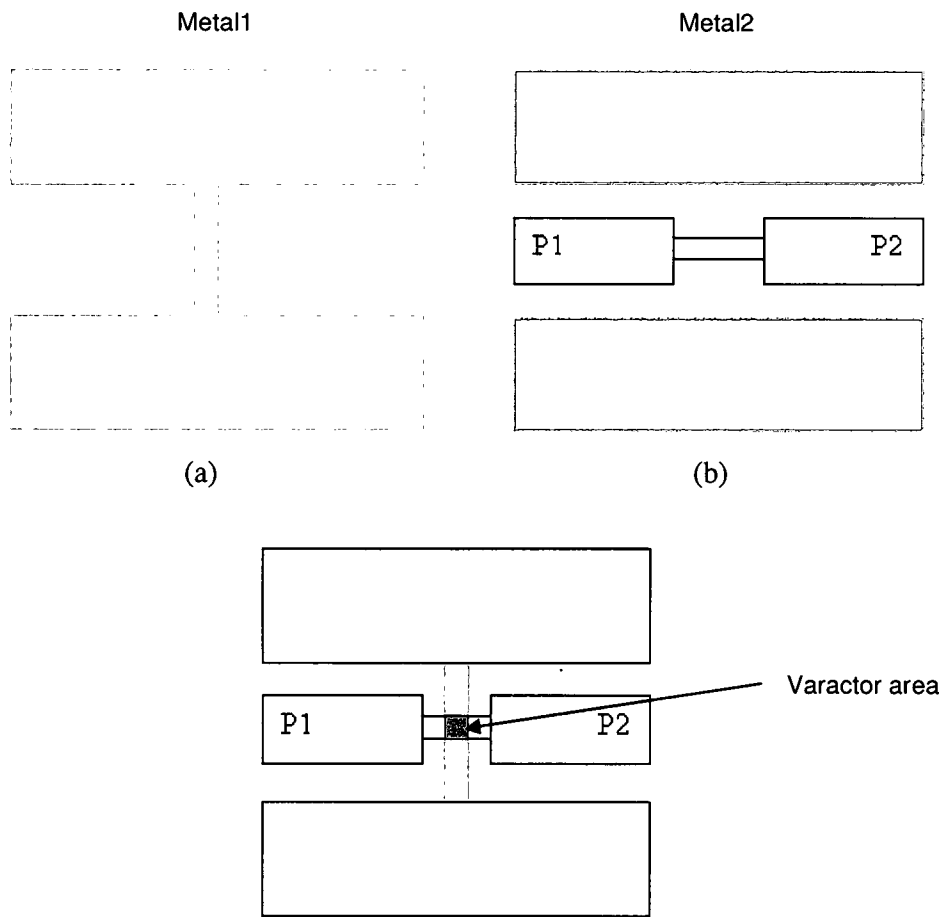


Fig. 5.9 : Different metal layer structure; (a) metal1 layer (b) metal2 layer, and (c) final device with varactor area.

device model with a varactor area. In Fig. 5.9, P1 and P2 stand for port1 (input) and port2 (output) respectively. The capacitive shunt switch with different varactor areas ranging from $5 \times 5 \mu\text{m}^2$ to $17.5 \times 17.5 \mu\text{m}^2$ have been designed,

fabricated, and tested. The overall dimension of the device is $500\mu\text{m} \times 450\mu\text{m}$. The ground planes in the top and bottom electrodes are effectively shorted due to the large capacitance between the two metal layers.

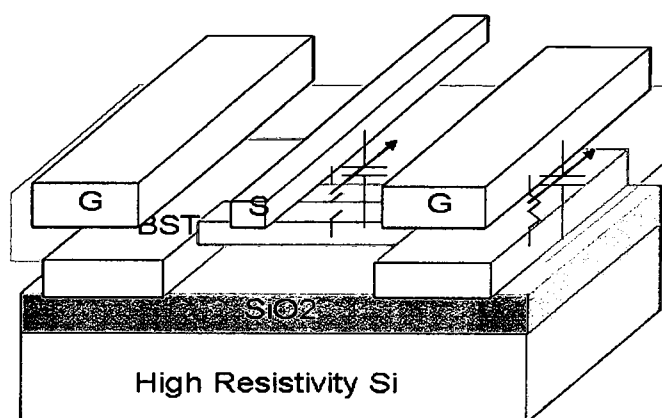


Fig. 5.10 : Three-dimensional view of the varactor shunt switch, showing the varactor and large ground-pad capacitance.

From Fig. 5.10, we see that the varactor capacitance is in series with the large ground pad capacitance introduced between the ground conductors of the two metal layers. One can show mathematically, the effective capacitance to be the smaller capacitance which is the varactor capacitance (**Appendix A**). The device does not require any via hole to the ground pads in metal1, because a dc voltage applied to the signal conductors will pass through the shunt leakage conductances of the varactor and the large ground pad capacitor to the ground line of the top conductor. Hence, this device results in a simpler process to fabricate.

5.4 Critical design parameters

The performance of the capacitive shunt switch depends on several design parameters. The following are the important parameters:

- 1) High dielectric tunability of BST thin-films.
- 2) Thickness of the BST thin-films.
- 3) The varactor area (overlap area of the metal1 and metal2 layers).
- 4) CPW transmission line parameters, such as the width of the center conductor, spacing between the center and ground conductors, and length of the CPW line sections.
- 5) Parasitic inductance and resistance of the thin-line shunting to the grounds in metal1.

5.5 Modeling of the capacitive shunt switch

Fig. 5.11 shows electrical modeling of the capacitive shunt switch. From the electrical modeling, we see that a very large ground capacitance (C_1) is in series with the varactor capacitance (C). One can readily show that the effective capacitance is the varactor capacitance if $C_1 \gg C$ (**Appendix A**). Therefore, Fig. 5.11 reduces to Fig. 5.12. The per unit resistance, inductance and capacitance of the transmission line have been calculated using Eqs. (4.6), (4.7), and (4.9) respectively. Since, the parasitic capacitance of the transmission line is very small, so, we have ignored it in this design. The per unit series resistance of the shunt line between the two ground conductors (metal1) has been calculated

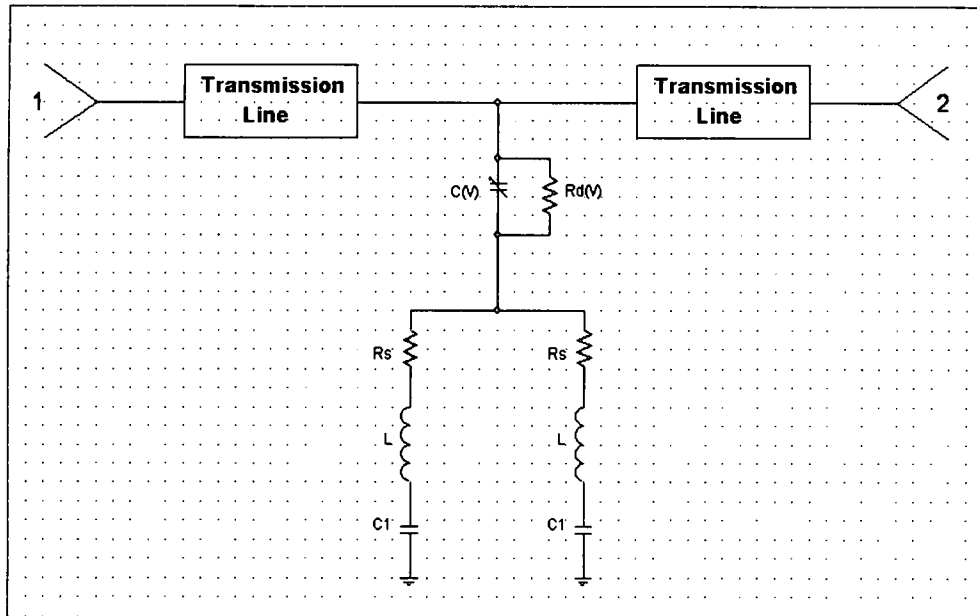


Fig. 5.11 : Equivalent electrical model of the capacitive shunt switch shows in Fig. 5.5.

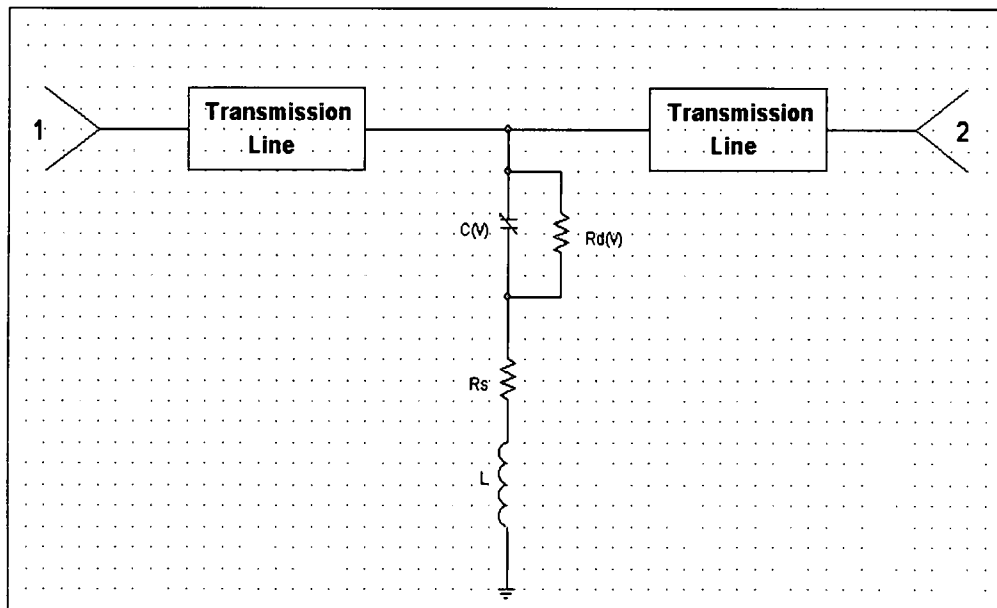


Fig. 5.12 : Modified electrical model of the capacitive shunt switch.

using Eq. (4.10). The per unit inductance is expressed by [106];

$$L = \frac{Z_0}{2\pi f} \sin\left(\frac{2\pi f}{\lambda_g}\right) \quad (5.1),$$

where Z_0 is the characteristic impedance of the CPW transmission line, f is the operating frequency, and λ_g is the guide wave length of the transmission line.

The capacitance of the varactor can be expressed as:

$$C(V) = \frac{\varepsilon_0 \varepsilon_r(V) A}{t_d} \quad (5.2),$$

where ε_0 is the permittivity of the free-space, $\varepsilon_r(V)$ is the voltage dependent dielectric constant of the BST thin-films, A is the overlap area of the varactor, and t_d is the thickness of the BST thin-films. One can express the shunt resistance of the varactor as follows:

$$R_d = \frac{1}{\omega C(V) \tan \delta} \quad (5.3),$$

where ω is the operating angular frequency, $C(V)$ is the capacitance of the overlap area of the varactor, and $\tan \delta$ is the loss tangent of the BST thin-films.

The loss tangent can be defined as,

$$\tan \delta = \frac{\varepsilon''}{\varepsilon'} \quad (5.4),$$

where dielectric permittivity of the BST thin-films is a complex quantity, given by:

$$\varepsilon = \varepsilon' - j\varepsilon'' \quad (5.5),$$

The real part of the expression is the relative dielectric constant of ϵ_r and the imaginary part contains the information about the shunt conductance of the ferroelectric materials of the BST thin-films [108].

5.6 Optimization of the device

To reduce losses, the characteristic impedance (Z_0) of the CPW line is taken as 50Ω for all the devices. The width of the center conductor and spacing between the center and ground conductors is optimized to get the characteristic impedance. Since the device is designed on a multilayer substrate, a conformal mapping technique is used to determine the characteristic impedance of the CPW line. The ratio of the width of the center conductor to the spacing between the ground and center conductors is denoted by k (geometric ratio), mathematically,

$$k = \frac{W}{W + 2S} \quad (5.6)$$

where W is the width of the center conductor and S is the spacing between the center and ground conductors. From Fig. 4.4, we see that Z_0 of the CPW line varies with the geometric ratio of k which depends on the geometric dimensions of the CPW line. In this design, both W and S are taken to be $50\mu m$ to get a Z_0 approximately 50 Ohms. So the geometric ratio of k is 0.333. From Fig. 5.5, we see that the width of the center conductor of the CPW line is not uniform. The overlap section of the center conductor needs to be smaller than the other according to the cross section area in the overlap region. It is required to change

the width of the center conductor smoothly to reduce the radiation and mismatch losses [107]. But from Fig. 5.5, we see that the center conductor of the CPW transmission line is suddenly tapered (90°) which increased the losses. To reduce the losses, the transmission line is tapered with a 45° section. Fig. 5.13 shows a photograph of an optimized fabricated varactor shunt switch [31].

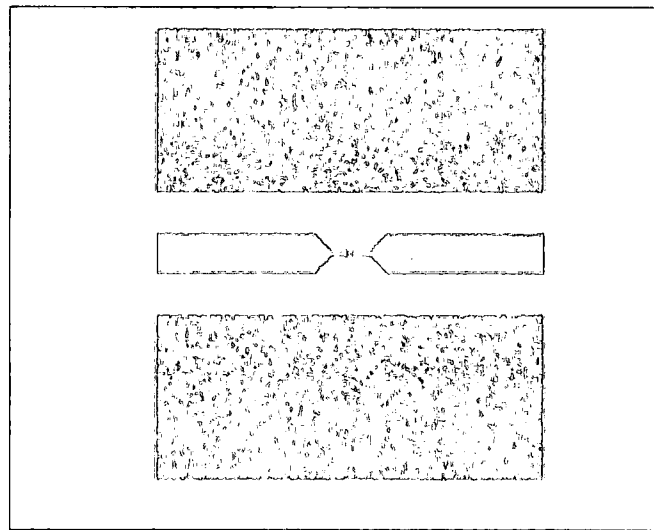


Fig. 5.13 : Photograph of an optimized fabricated capacitive shunt switch.

From Fig. 5.13, one can see clearly the metal2 (bright) and shunt line (dark) of metal1 between the two grounds of the device. From the optimized fabricated switch, we can also see that the signal conductor of the CPW line bends at 45° . Fig. 5.14 shows the fabricated several capacitive shunt switches on a single wafer for testing. The spacing between the center and ground conductors increased due to decreasing the width of the center conductor in the overlap region of the device. To obtain a characteristic impedance 50Ω of all the sections of the device, this portion of the device needs to be optimized for the same

spacing ($50\mu\text{m}$). Fig. 5.15 shows an equal spacing between the center and ground conductors of the device. The switching performance (e.g. insertion loss) can be improved by using the selective area deposition process. Fig. 5.16 shows the capacitive shunt switch using selective area deposition method. In selective area deposition method, BST thin-films are deposited only in the varactor areas instead of the entire surface.

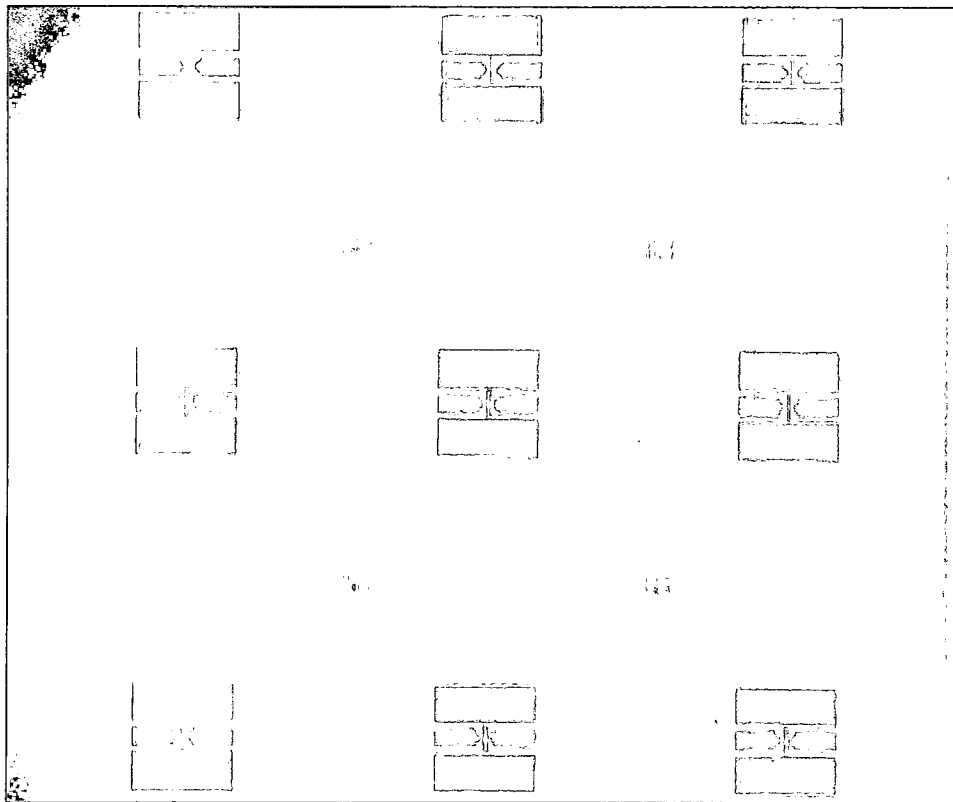


Fig. 5.14 : Fabricated devices with different overlap area on a single wafer.

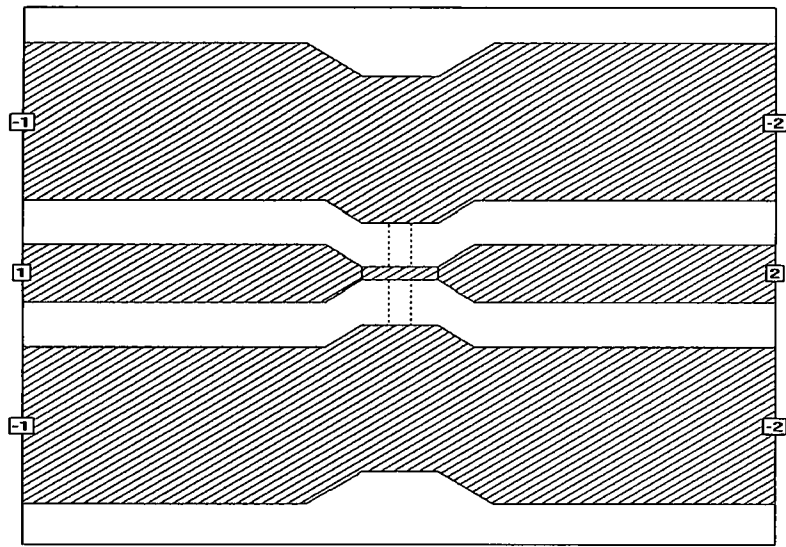


Fig. 5.15 : An optimized shunt switch (not fabricated yet), showing an equal spacing between the center and ground conductors of all the sections of the device.

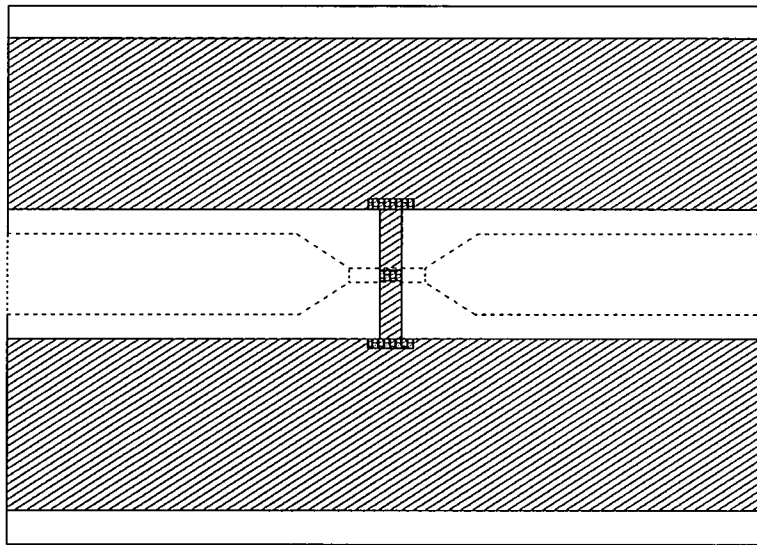


Fig. 5.16 : Capacitive shunt switch showing the selective area deposition of the BST thin-films (dark region).

5.7 Theoretical Analysis

Fig. 4.4 shows the variation of the characteristic impedance with the geometric ratio (k) of the CPW line designed on the multilayered substrates. The effective dielectric permittivity needs to be determined to obtain the characteristic impedance of the CPW transmission line due to the non-homogeneous media. The conventional formulas [79]-[97] are no longer valid to determine the filling factor (denoted by q) for a particular layer of the multilayer substrates if the thickness of the layer is too small. An assumption [81] is made to obtain the filling factor for the thin layer and it can be expressed as [81]:

$$q = \frac{h}{S} \quad (5.7)$$

where h is the height of a particular layer and S is the gap between the center and ground conductors of the CPW line. Less than 5% error has been obtained based on the above assumption (5.7) to calculate the overall filling factors.

The isolation in the OFF state and the insertion loss in the ON state are the most important performance parameters for any switching device. If we denote the transmission line parameters, varactor capacitance with the shunt conductance, series resistance, and inductance and characteristic impedance of the source and load as Z_1 , Z_2 and Z_0 respectively, then one can redraw the electrical model as shown in Fig. 5.17. In Fig. 5.17, 1, 2, Z_s , Z_L , (+), and (-)

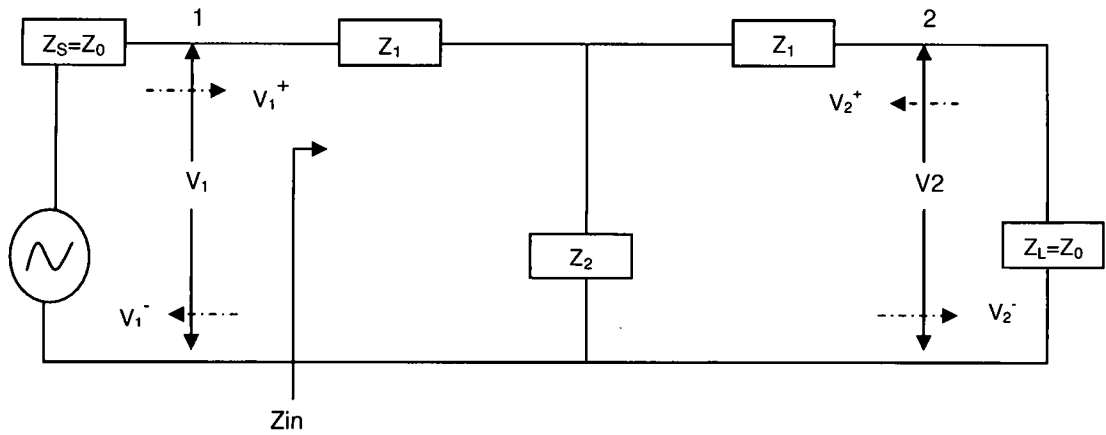


Fig. 5.17 : Model to determine the S-parameters of the capacitive shunt switch, showing forward and backward traveling waves and also source and load impedances.

stand for port1, port2, source impedance, load impedance, forward traveling wave and backward traveling wave respectively. The source and load impedances are assumed to be 50Ω in this analysis. Since parasitic capacitance of the transmission line is very small, for analysis purpose, it can be ignored this parameter in this design as well as in Fig. 5.17. Z_{in} stands for the input impedance at the port 1 looking towards the port 2. By using S-parameters analysis (**Appendix B**), the reflection coefficient at port 1 can be written as:

$$S_{11} = \frac{(Z_0 + Z_1 + Z_2)(Z_1 - Z_0) + Z_2(Z_0 + Z_1)}{(Z_0 + Z_1)(Z_0 + Z_1 + 2Z_2)} \quad (5.8)$$

The output signal at port 2 can be expressed, when applying the signal at port 1, as

$$S_{21} = \frac{2Z_0Z_2}{(Z_0 + Z_1)(Z_0 + Z_1 + 2Z_2)} \quad (5.9)$$

where Z_0 is the characteristic impedance of the CPW line and assuming 50Ω , Z_1 is the summation of resistance and inductance of the transmission line and Z_2 is the summation of the varactor capacitance with parallel shunt conductance and the parasitic series resistance and inductance of the shunt line. Detailed description for the expressions of S_{11} and S_{21} are presented in Appendix B. The resistance and inductance of the transmission line have been obtained approximately 0.2537Ω and 0.203nH respectively by using Eqs. (4.6) and (4.7). The inductance and resistance of the shunt line are calculated by using Eqs. (5.1), (4.6) and obtained approximately 0.02nH and 0.1645Ω respectively. The varactor capacitance has been calculated using Eq. (5.2) with the thickness 400nm of the BST thin-films for the different varactor areas ranging from $2.5 \times 2.5\mu\text{m}^2$ to $17.5 \times 17.5\mu\text{m}^2$. The isolation in the OFF state and insertion loss in the ON state can be found using Eq. (5.9) at a particular frequency. Table2 shows the theoretical capacitance and the resonance frequency in the OFF state by using Eq. (5.9). Table2 also shows the isolation in the OFF state and insertion loss in the ON state at the resonance frequency. One can easily calculate the resonance frequency in the OFF state of the switch using the general formula can be shown as an equation $\left(\frac{1}{2\pi\sqrt{L_s C_v}} \right)$, where C_v is the varactor capacitance, and L_s the parasitic series inductance. The resonance frequency using the general formula and Eq. (5.9) is shown in Table2.

Table 2 : Theoretical performance summary of the switches designed, based on the assumption $\epsilon_{\text{BST}}=500$, $\tan\delta=0.045$ at zero-bias and $\epsilon_{\text{BST}}=150$, $\tan\delta=0.03$ at 10 V bias.

Varactor overlap area (μm^2)	OFF state capacitance (pf)	ON state capacitance (pf)	OFF state resonance frequency (GHz)	OFF state Isolation @resonance Frequency (-dB)	ON state Insertion loss @resonance Frequency (-dB)
2.5×2.5	0.069	0.021	133	52	13
5×5	0.277	0.083	68	46	11
7.5×7.5	0.623	0.187	45	43	11
10×10	1.107	0.332	34	43	11.7
12.5×12.5	1.729	0.519	27	42	13
15×15	2.49	0.747	23	42	13.8
17.5×17.5	3.389	1.017	19	42	16

The higher isolation in the OFF state and the lower insertion loss in the ON state are always desirable for any switch operation. Higher the capacitance in the OFF state gives better isolation, and higher insertion loss in the ON state of the device. Capacitance can be increased with increasing the overlap area and using the higher dielectric constant BST thin-films, and also using thinner BST thin-films. In the current design, the dielectric constant and the thickness of the dielectric layer are constants; hence we can only change the varactor overlap area to operate the switch at a particular frequency. Devices with overlap areas ranging from $2.5 \times 2.5 \mu\text{m}^2$ to $17.5 \times 17.5 \mu\text{m}^2$ are designed. From Fig. 5.18 using Eq.(5.9), we see that isolation can be improved at a particular frequency using higher overlap area with higher insertion loss (see Fig. 5.19). Fig. 5.18 also shows that the resonance frequency is reduced due to increasing the capacitance of the varactor.

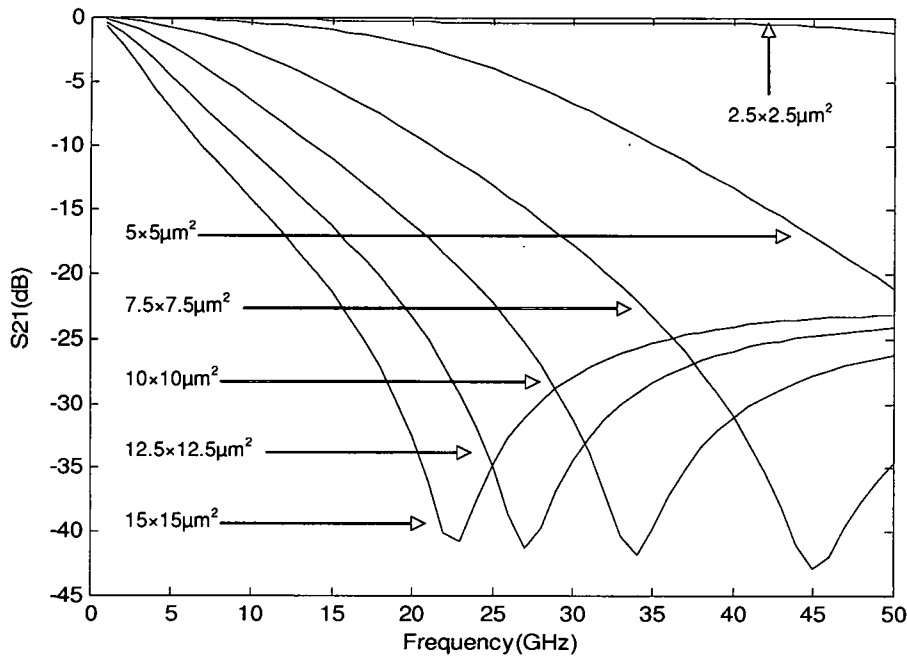


Fig. 5.18 : Theoretical isolation with different overlap area in the OFF state of the capacitive shunt switch.

Theoretical isolations (Fig. 5.18) in the OFF state of the switch with the varactor area of $15 \times 15 \mu\text{m}^2$, $12.5 \times 12.5 \mu\text{m}^2$, $10 \times 10 \mu\text{m}^2$, $7.5 \times 7.5 \mu\text{m}^2$, and $5 \times 5 \mu\text{m}^2$ are obtained approximately 30dB, 24dB, 16dB, 9dB, and 4dB respectively at 20 GHz and the insertion loss in the ON state of the switch (at the same frequency) with the same varactor area as shown in Fig. 5.19 have been obtained approximately 12dB, 7.5dB, 4.5dB, 0.7dB, and 0.3dB respectively.

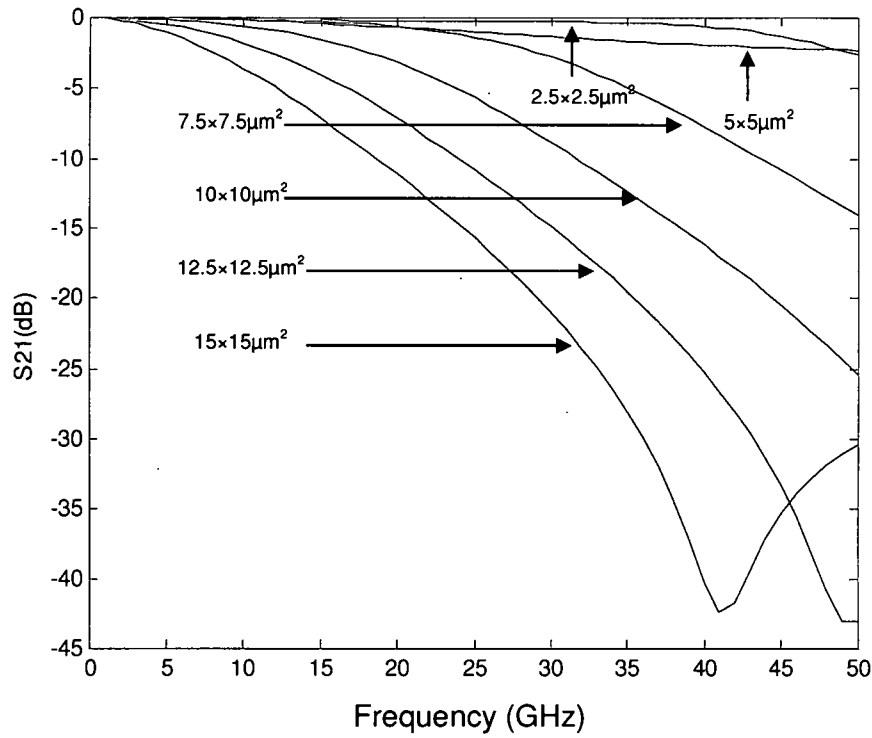


Fig. 5.19 : Theoretical insertion loss with different overlap area of the capacitive shunt switch.

We have already assumed that both the load and source impedances are 50 Ohms and are perfectly matched to the characteristic impedance of the CPW transmission line. The input power can be written is as follows;

$$P_{in} = \frac{|V_1|^2}{2Z_0}$$

By using **Appendix B**, we get,

$$P_{in} = \frac{|V_1^+|^2 * |1 + S_{11}|^2}{2Z_0} \quad (5.10).$$

The output power can be written,

$$P_{out} = \frac{|V_2|^2}{2Z_0}$$

By using APPENDIX B, we get,

$$P_{out} = \frac{|V_1^+|^2 * |S_{21}|^2}{2Z_0} \quad (5.11)$$

By using Eqs. (5.10) and (5.11), we can write the output power,

$$P_{out} = \frac{|S_{21}|^2}{|1 + S_{11}|^2} * P_{in} \quad (5.12)$$

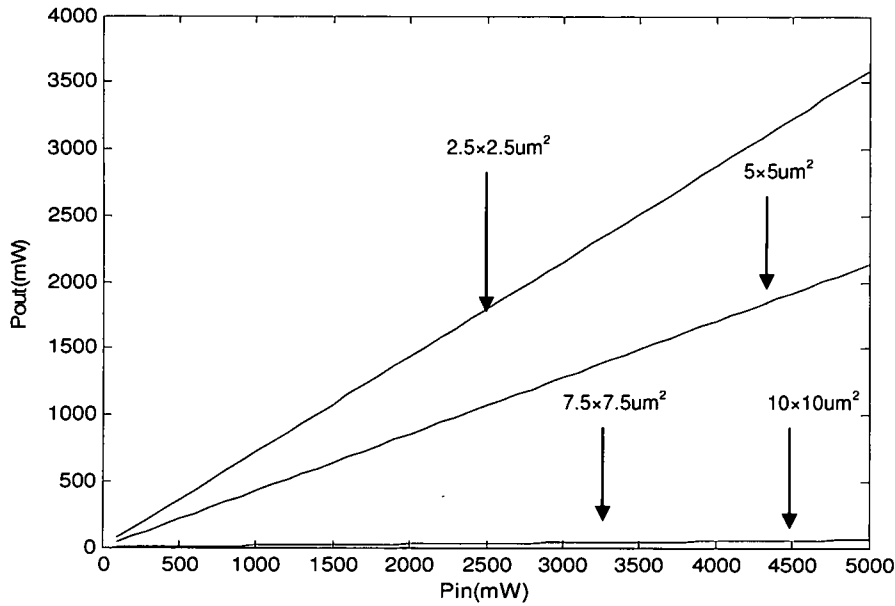


Fig. 5.20 : Output power versus input power at 20 GHz in the OFF state of the capacitive shunt switch.

By knowing S_{11} and S_{21} parameters using Eqs. (5.8) and (5.9), one can easily determine the output power using the above expression at any frequency. The capacitive shunt switch blocks the power based on the capacitance in the OFF

state. The higher the capacitance value, the lower the output power. From Fig. 5.20, we see that output power reduces with increasing the overlap area due to increasing the capacitance in the OFF state of the switch.

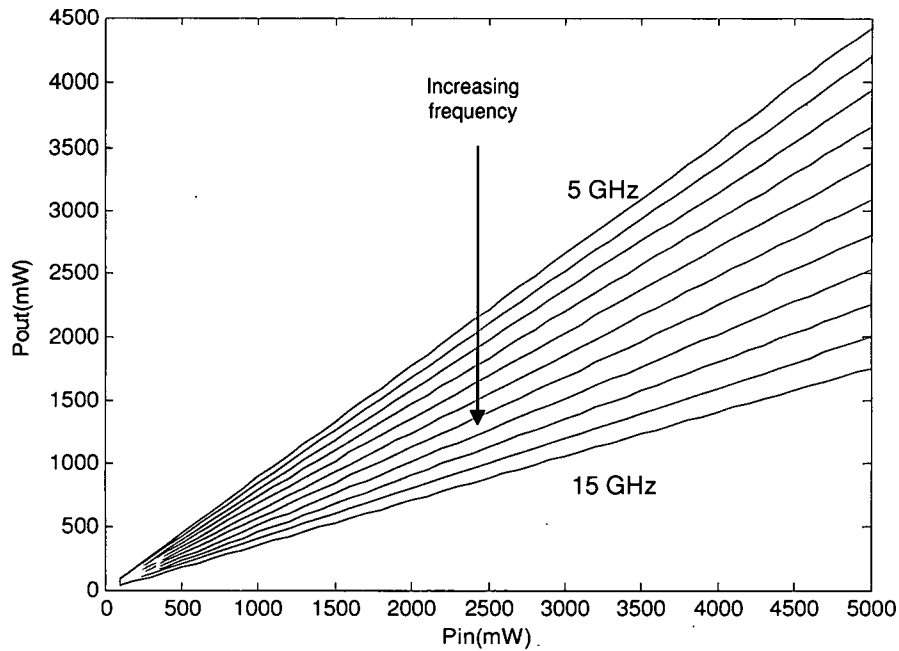


Fig. 5.21 : Output power versus input power in the ON state of the switch with an overlap area of $10 \times 10 \mu\text{m}^2$ with frequency ranges from 5 to 15 GHz.

The output power decreases with increasing the frequency in the ON state of the switch due to decreasing the capacitance. From Fig. 5.21, one can see that output power reduces with increasing the frequency for the overlap area of $10 \times 10 \mu\text{m}^2$.

5.8 Discussions on simulation results

The performance (e.g. high isolation, low insertion loss and etc.) of the capacitive shunt switch depends on the dielectric tunability of the ferroelectric materials of BST thin-films. The higher the capacitance, the better the isolation in the OFF state but it also increases the insertion loss in the ON state. The capacitance value can be increased by using high dielectric constant of the ferroelectric thin-films or large varactor area or reducing the thickness of the dielectric layer. Since dielectric constant of the BST thin-films is constant for a particular composition ratio (here Ba/Sr is 60/40) and thickness is also constant ($\sim 400\text{nm}$), only the overlap area of the capacitive shunt switch needs to be changed to operate the device at different frequencies. Table 3 shows the simulated performance of the capacitive shunt switch with different overlap area. From Table 2 and Table 3, we see that simulated resonance frequency is lower than the theoretical resonance frequency due to the parasitic effect.

The isolation can be improved in the OFF state by using the larger overlap area but it also increases the insertion loss in the ON state of the device. One can operate the device at any frequency by designing the overlap area. Fig. 5.22 shows the simulated isolation in the OFF state of the device for a fixed dielectric constant of 500 and thickness of 400nm with varactor area of $15 \times 15 \mu\text{m}^2$, $12.5 \times 12.5 \mu\text{m}^2$, $10 \times 10 \mu\text{m}^2$, $7.5 \times 7.5 \mu\text{m}^2$, and $5 \times 5 \mu\text{m}^2$ (left to right). From Fig. 5.22, we see that isolation increases and resonance frequency decreases due to the capacitance for the larger varactor area.

Table 3 : Simulated performance summary of the switches designed, based on the assumption $\epsilon_{\text{BST}}=500$, $\tan\delta=0.045$ at zero-bias and $\epsilon_{\text{BST}}=150$, $\tan\delta=0.03$ at 10 V bias.

Varactor overlap area (μm^2)	OFF state capacitance (pf)	ON state capacitance (pf)	OFF state resonance frequency (GHz)	OFF state Isolation @resonance Frequency (-dB)	ON state Insertion loss @resonance Frequency (-dB)
2.5×2.5	0.069	0.021	112	26	1.1
5×5	0.277	0.083	67	33	4.9
7.5×7.5	0.623	0.187	49	37	8
10×10	1.107	0.332	39	40	11
12.5×12.5	1.729	0.519	32	41	12
15×15	2.49	0.747	28	43	14

But larger varactor area also increases the insertion loss in the ON state of the switch (Fig. 5.23). The simulated isolation (Fig. 5.22) at 20 GHz in the OFF state of the switch with varactor area of $15\times 15\mu\text{m}^2$, $12\times 12\mu\text{m}^2$, $10\times 10\mu\text{m}^2$, $7.5\times 7.5\mu\text{m}^2$, and $5\times 5\mu\text{m}^2$ have been obtained as 24.36dB, 19.35dB, 14.28dB, 8.96dB, and 3.66dB respectively. The simulated insertion losses (Fig. 5.23) in the ON state of the switch at the same frequency with same varactor area shown in Fig. 5.22 have been obtained as 9.89dB, 6.92dB, 4.09dB, 1.75dB, and 0.12dB respectively. From Fig. 5.22 and Fig. 5.23, we see that higher the varactor area, better the isolation, and higher insertion loss. Fig. 5.24 shows the simulated isolation and insertion loss of the optimized device shown in Fig. 5.15. The isolation of the device is better than 20 dB at 40 GHz and the insertion loss is below 5 dB at this frequency. Fig. 5.25 shows a comparison between the simulated results based on the electromagnetic simulation of the physical device (Fig. 5.15), and the electrical model (Fig. 5.12). The insertion loss of the two simulations compare well. The isolation is better for the electrical model as it

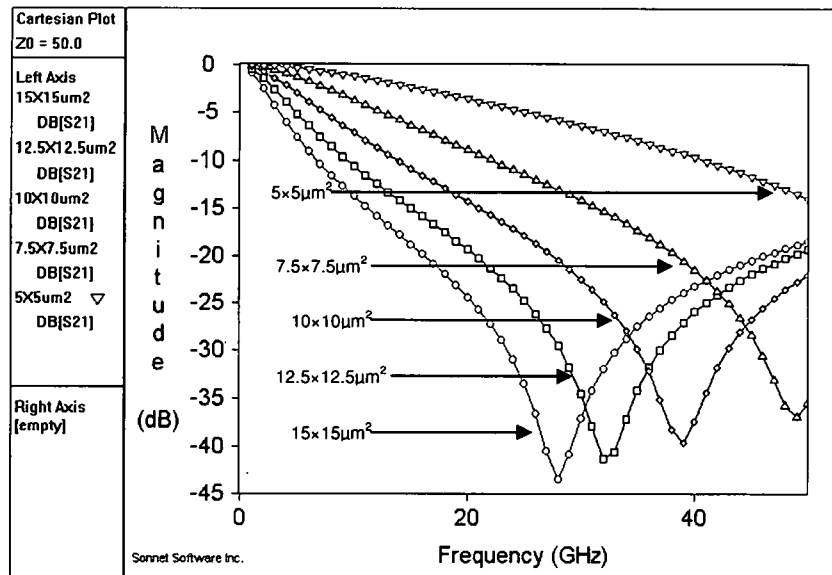


Fig. 5.22 : Simulated isolation for the different varactor area using the same dielectric constant (500) and thickness (400nm) of the BST thin-films.

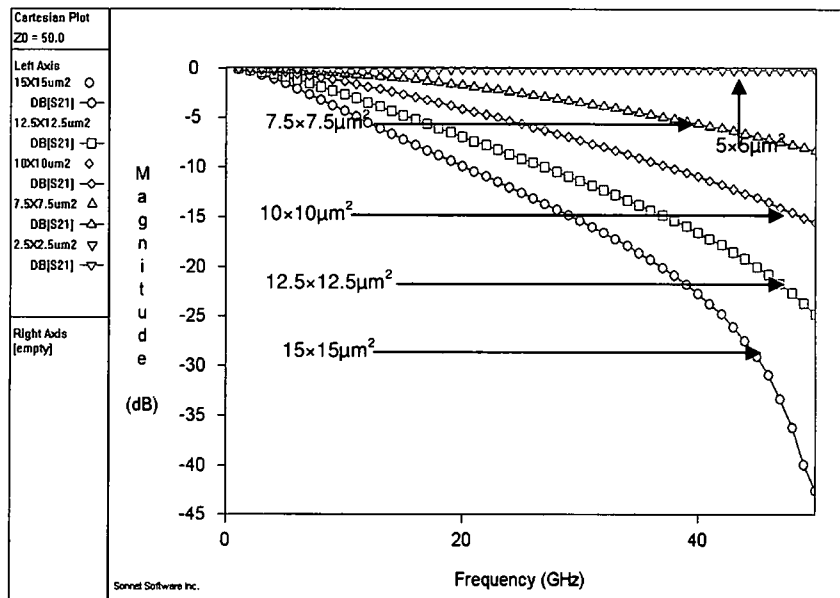


Fig. 5.23 : Simulated insertion losses using different varactor area (from $15 \times 15 \mu\text{m}^2$ to $5 \times 5 \mu\text{m}^2$, left to right) with relative dielectric constant of 120 and thickness (400 nm) of the BST thin-films.

ignores the parasitic the parasitic effects [12]. The simulation results (Fig. 5.25) show a good agreement between the electrical and physical models over the frequency 5-18 GHz .One can improve the insertion loss (ON state) by using the selective area (see Fig. 5.16) deposition process of the BST thin-films. From simulation results in Fig. 5.26, we see that the insertion loss improves at least 1dB (green curve) using selective area deposition process but the isolation doesn't change that much.

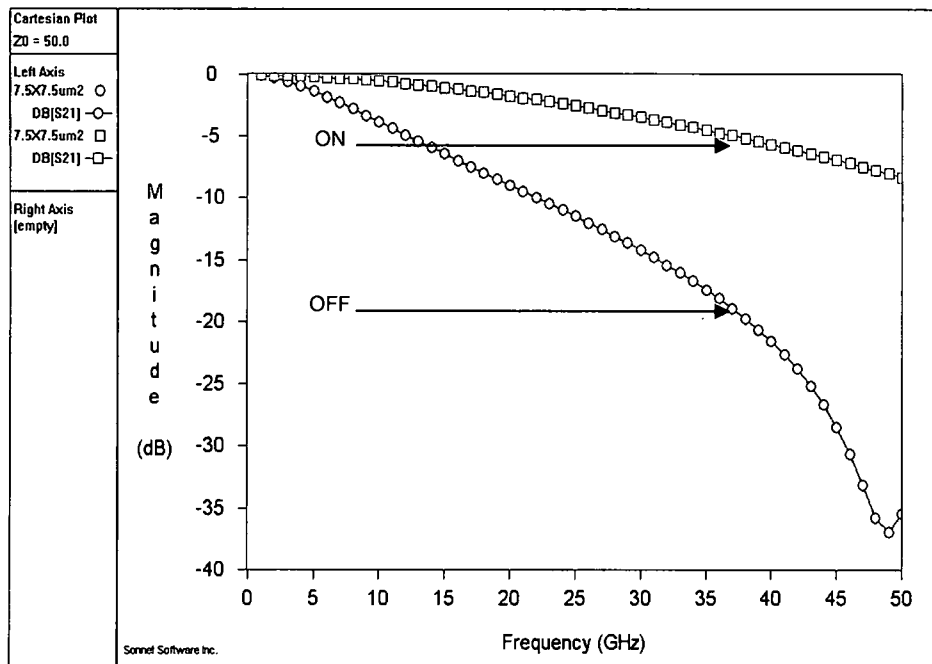


Fig. 5.24 : Simulated isolation and insertion loss of the physical device with dielectric constant 500 (OFF) and 150 (ON) for the varactor area of $7.5 \times 7.5 \mu\text{m}^2$.

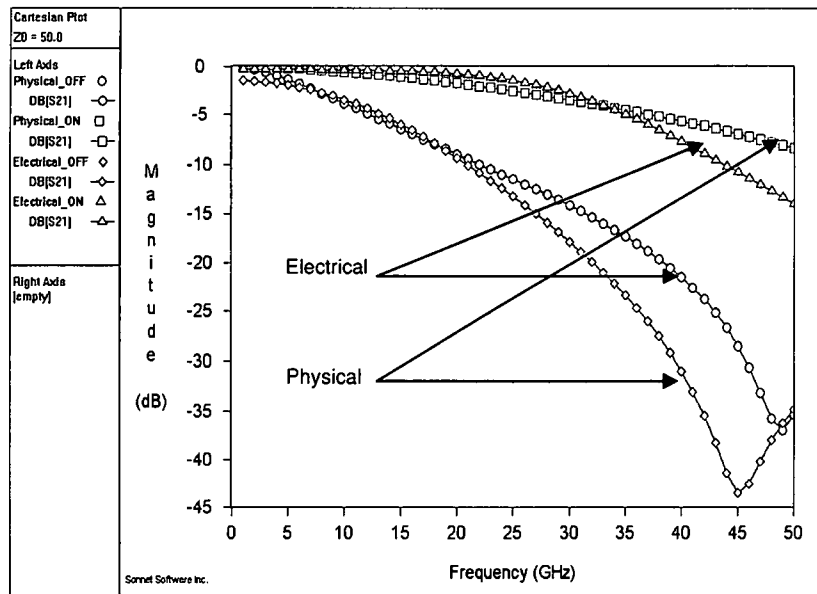


Fig. 5.25 : Compared simulations between the physical and electrical model (Fig. 5.12) for the isolation and insertion loss of the optimized device.

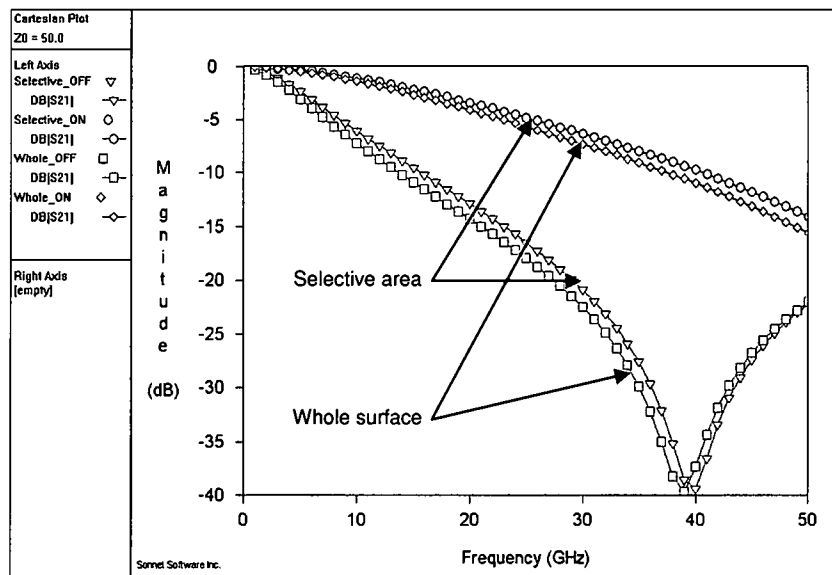


Fig. 5.26 : Compared simulated isolation and insertion loss between the selective area and entire surface deposition methods with an overlap area of $10 \times 10 \mu\text{m}^2$.

5.9 Discussion on experimental results

A ferroelectric varactor-based capacitive shunt switch with different overlap areas ranging from $2.5 \times 2.5 \mu\text{m}^2$ to $17.5 \times 17.5 \mu\text{m}^2$ have been designed, simulated, fabricated, and tested. The varactor shunt switches have been tested using HP8510 vector network analyzer (VNA), with a line-reflect-reflect-match (LRRM) calibration is performed over a frequency up to 45 GHz [31]. A bias voltage has been applied through the bias tee of the VNA and switch is probed using standard ground signal ground (GSG) probes. The experimental results have been obtained with different overlap area varactors fabricated using PLD process on a single chip. Fig. 5.27 and Fig. 5.28 show the experimental measurements of S_{21} and S_{11} with the varactor area $5 \times 15 \mu\text{m}^2$ without and with applying a bias voltage [8],[13]. The isolation of this switch is measured approximately 20dB at 35 GHz and the insertion loss is below 4dB up to 30 GHz [13]. The large change in the S_{11} and S_{21} between the ON and OFF states indicates that the device has very good voltage dependent dielectric tunability [13].

We fabricated multiple switches with the same varactor area for testing. Fig. 5.29 shows the experimental swept frequency for S_{21} and S_{11} for bias voltages from 0 to 9.5 V with a step size of 2 V. The isolation is found to be ~24 dB at the resonance frequency of 41 GHz in the OFF state (zero bias) of the switch and the insertion loss has been obtained approximately 7 dB at 41 GHz with the highest bias voltage (ON state) of 9.5 V [8].

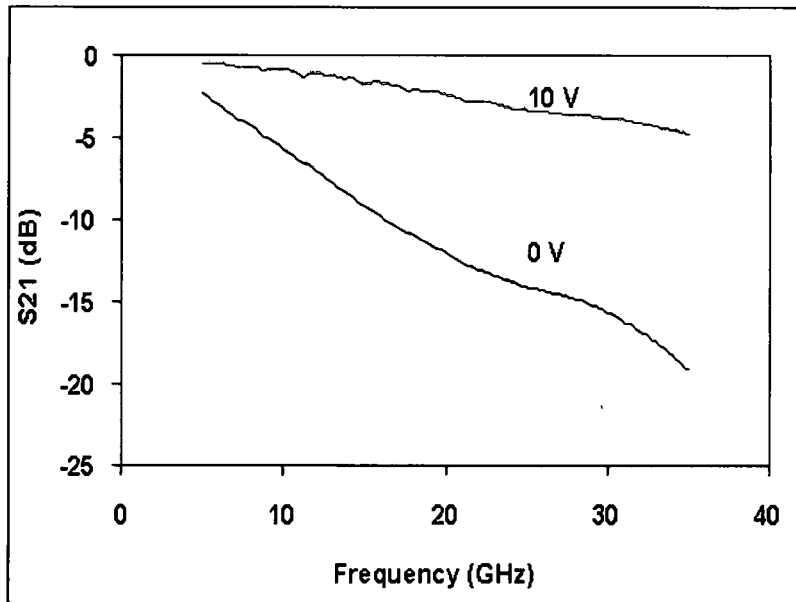


Fig. 5.27 : Experimental measurements of S_{21} for 0V (OFF state) and 10V (ON state) of the switch for an overlap area $5 \times 15 \mu\text{m}^2$.

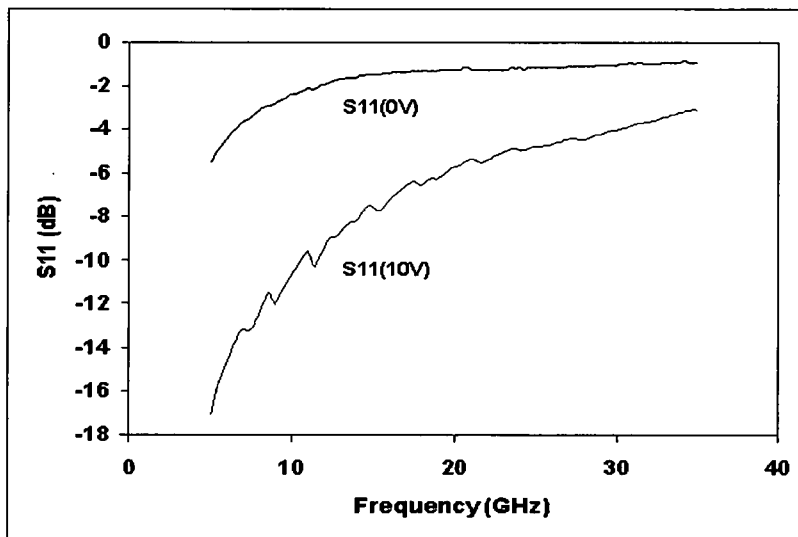
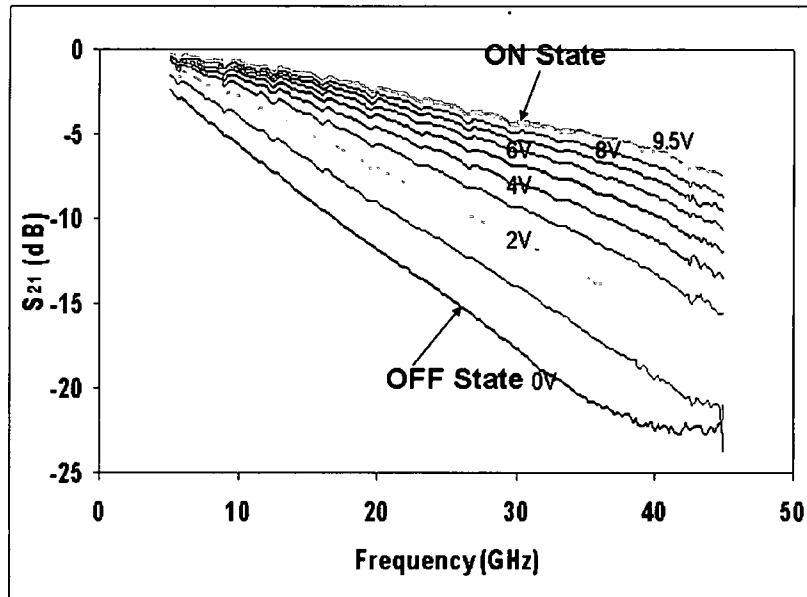
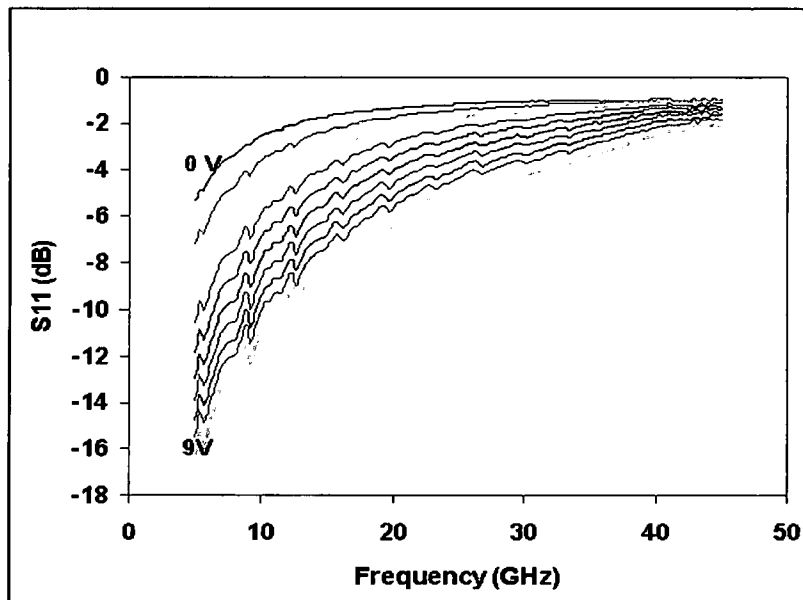


Fig. 5.28 : Experimental measurements of S_{11} for 0V (OFF state) and 10V (ON state) of the switch for overlap area $5 \times 15 \mu\text{m}^2$.

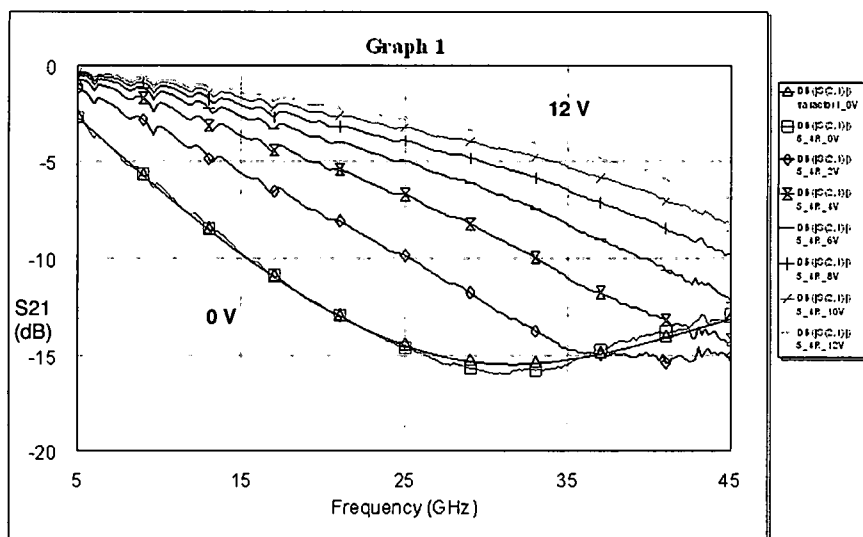


(a)

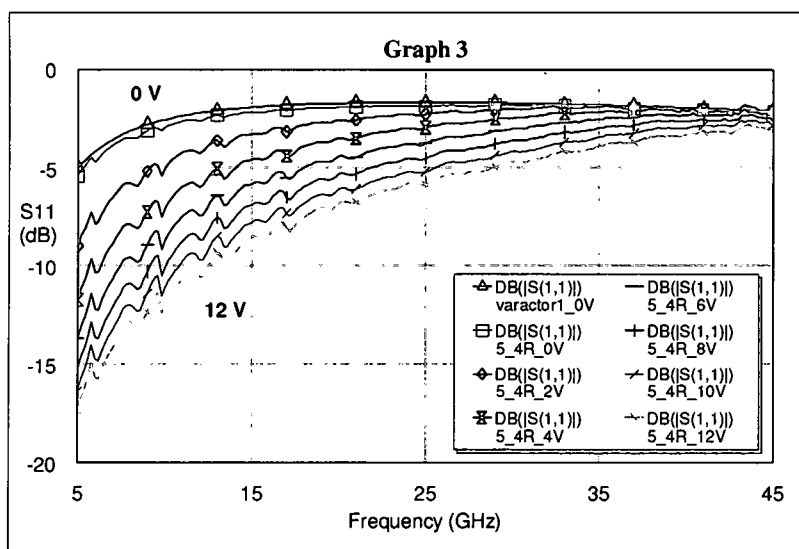


(b)

Fig. 5.29 : The experimental swept frequency for (a) S_{21} and (b) S_{11} with a $5 \times 15 \mu\text{m}^2$ varactor area for 0 V to 9.5 V with a step size of 2 V.

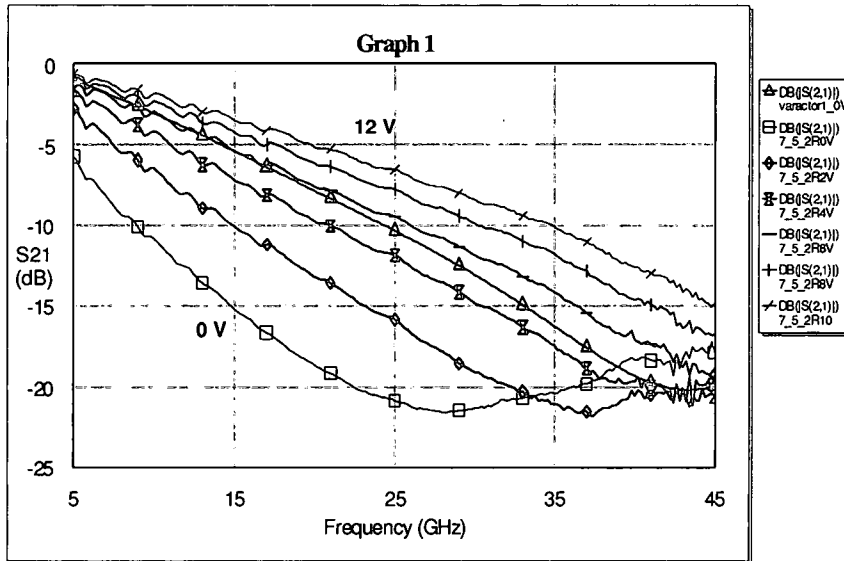


(a)

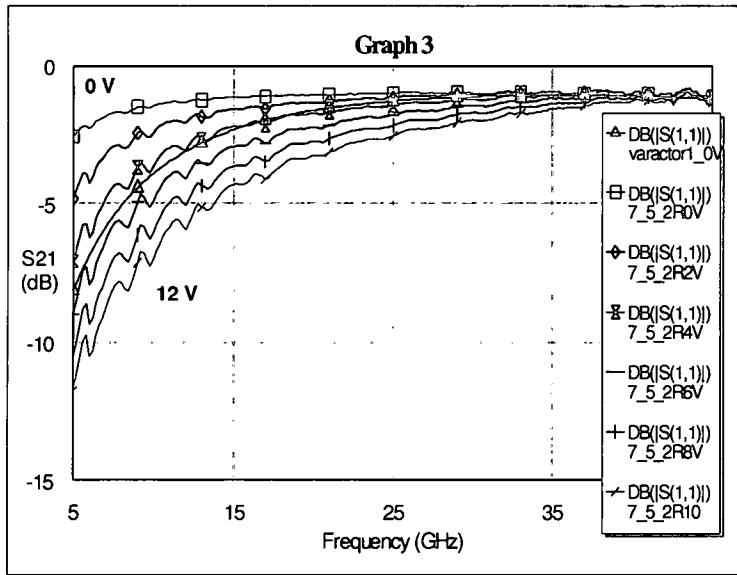


(b)

Fig. 5.30 : The experimental swept frequency for (a) S_{21} and (b) S_{11} with a $5 \times 5 \mu\text{m}^2$ varactor area for 0 V to 12 V with a step size of 2 V.



(a)

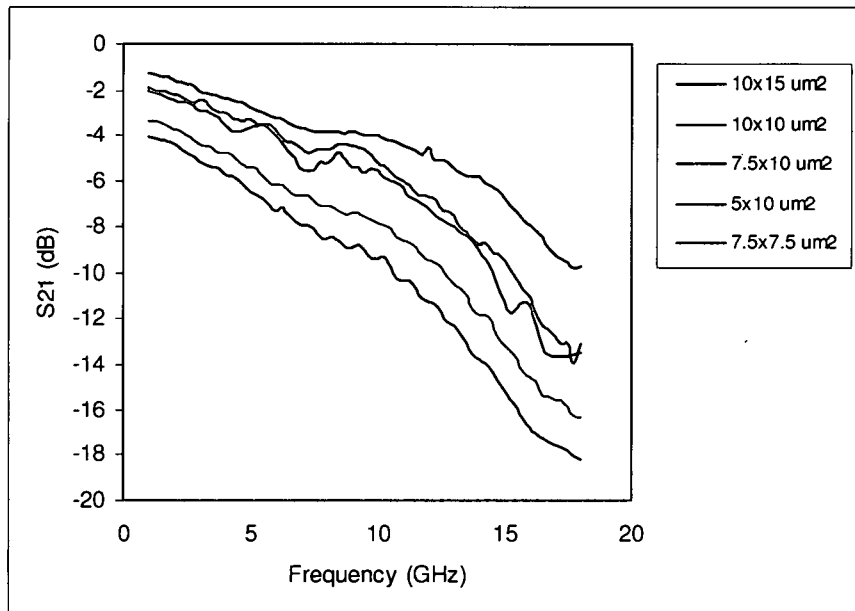


(b)

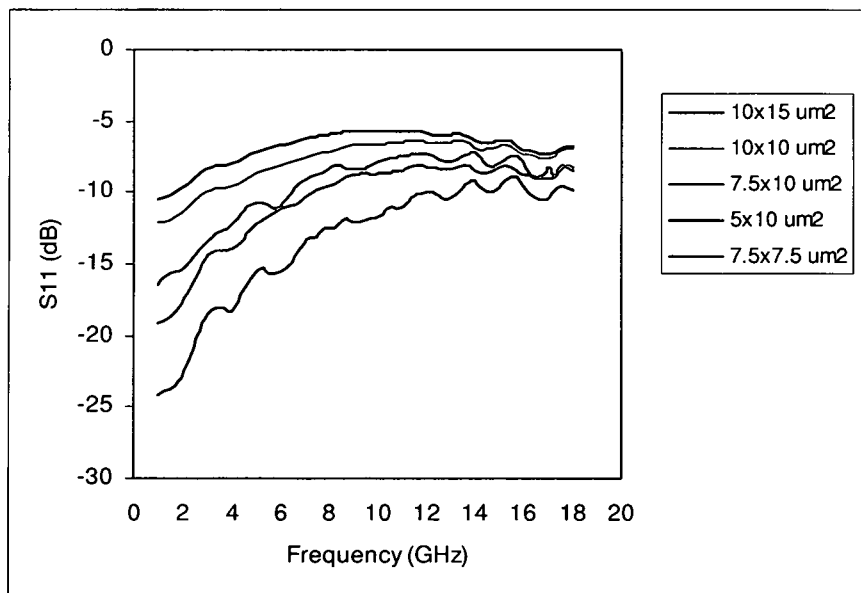
Fig. 5.31 : The experimental swept frequency for (a) S_{21} and (b) S_{11} with a $7.5 \times 7.5 \mu\text{m}^2$ varactor area for 0 V to 12 V with a step size of 2 V.

Fig. 5.30 and Fig. 5.31 show the experimental swept frequency responses of the varactor area of $5 \times 5 \mu\text{m}^2$ and $7.5 \times 7.5 \mu\text{m}^2$ respectively, for the bias voltages from 0 to 12 V with a step size of 2 V. The isolation and insertion loss for the varactor area of $5 \times 5 \mu\text{m}^2$ have been obtained approximately 16dB and 3 dB respectively at the resonance frequency of 32 GHz [31]. From Fig. 5.31, we see that the isolation can be improved using larger varactor area of $7.5 \times 7.5 \mu\text{m}^2$ at the expense of higher insertion loss. It is possible to obtain the isolation higher than 35 dB with a varactor area larger than $100 \mu\text{m}^2$, with the insertion loss above 10 dB [31]. Fig. 5.32 shows the experimental swept frequency for the different varactor area ranging from $7.5 \times 7.5 \mu\text{m}^2$ to $10 \times 15 \mu\text{m}^2$ without a bias voltage. From Fig. 5.32, we see that isolation is increasing with the larger varactor area due to increasing the capacitance.

The electrical parameters have been extracted by matching swept frequency response of the modeled (Fig. 5.12) to the experimental swept frequency response by using AWR's Microwave Office. Fig. 5.33 shows the size dependence of the electrical parameters as a function of the dc bias voltage of the shunt switches. Each of the devices is subjected to a different maximum bias voltage based on a maximum leakage current of 25 μA [31]. A generalized V_{max} is used in Fig. 5.33 and it is 12 V and 8 V for the varactor area of $5 \times 5 \mu\text{m}^2$ and $17.5 \times 17.5 \mu\text{m}^2$ respectively. The capacitance at the zero bias is 0.8 pF, and has been reduced to 0.18 pF at 12 V for the varactor area of $5 \times 5 \mu\text{m}^2$. For the

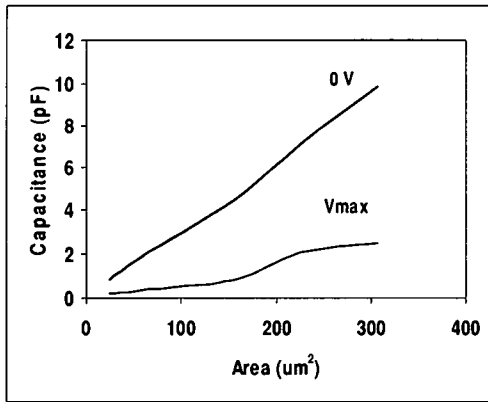


(a)

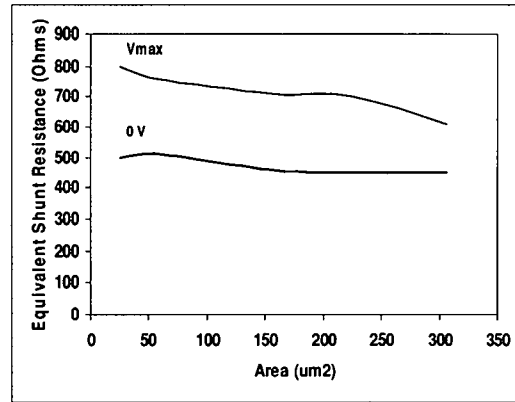


(b)

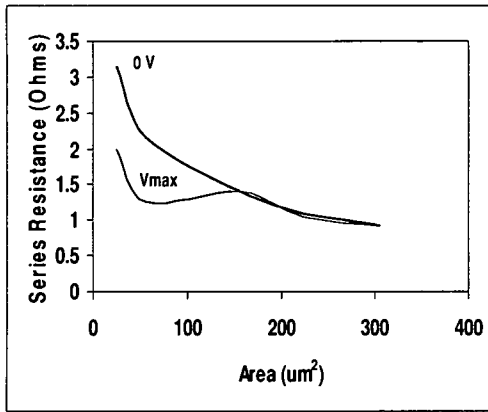
Fig. 5.32 : The experimental swept frequency for (a) S_{21} and (b) S_{11} for the varactor area from $7.5 \times 7.5 \mu\text{m}^2$ to $10 \times 15 \mu\text{m}^2$ without a bias voltage.



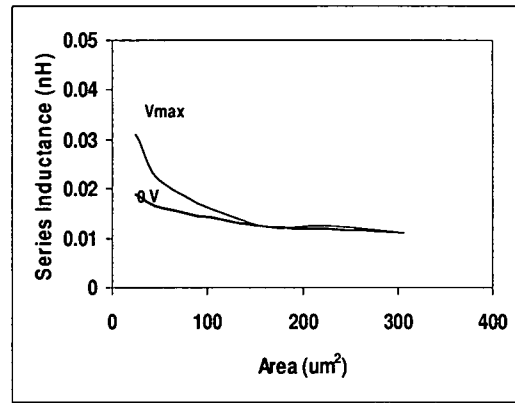
(a)



(b)



(c)



(d)

Fig. 5.33 : The extracted electrical parameters of the varactor shunt switch by comparing the response of the electrical model to the experimental frequency response.

capacitance is 9.86 pF at zero-bias, and has been reduced to 2.46 pF at 8V [31]. From Fig. 5.33 (c), we see that the equivalent series inductance (ESL) increased with increasing the bias voltage for the smaller overlap area due to the higher

conduction current in the dielectric layer with the higher bias voltage [31],[109]. We also see from Fig. 5.33 (d) that the equivalent series resistance (ESR) is bias dependent and is reduced with bias voltage due to the increasing shunt resistance of the capacitor. For the larger overlap area devices, the leakage currents are significantly higher, and results in less bias dependence for the ESL and ESR [31]. A current limit of 25 μA is set to prevent device breakdown.

The switching speed of the ferroelectric thin-films based varactor shunt switches has been determined using a continuous wave (CW) microwave signal and a dc step input to obtain both fall and rise times [31]. The measurement set up for the step response characterization is shown in Fig. 5.34. A YIG oscillator is used to generate a 10 GHz CW microwave signal. A calibrated diode is used to measure the output power. A thru-line calibration has been done before testing the device. Fig. 5.35 shows the step response of the input (with thru line) and output (with the device) for the varactor shunt switch with an overlap area of $5 \times 5 \mu\text{m}^2$.

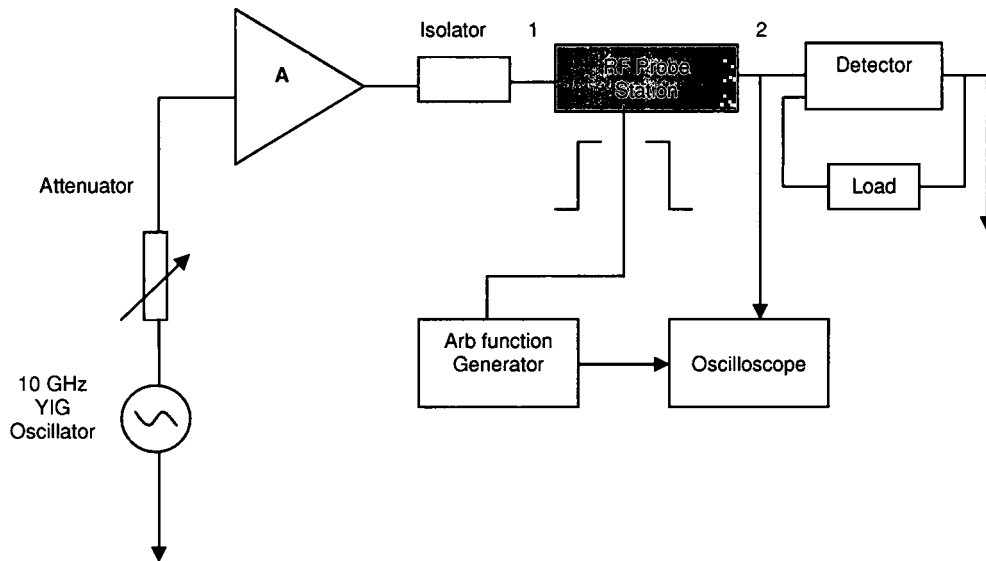
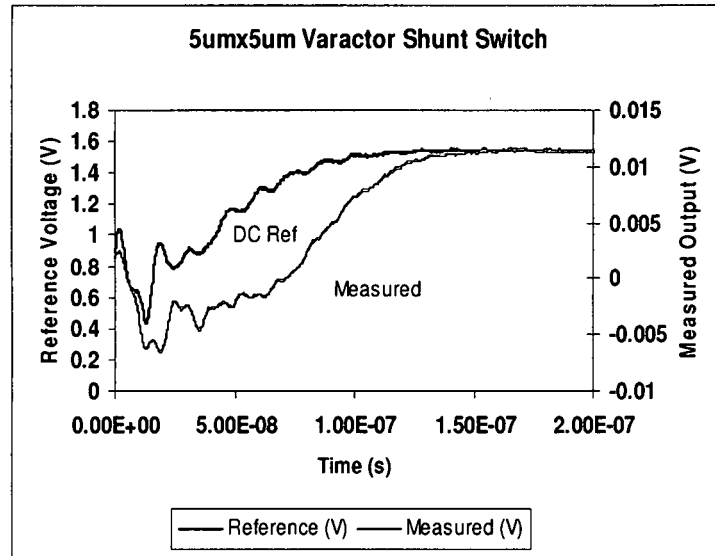


Fig. 5.34 : Experimental setup for switching - speed measurements.

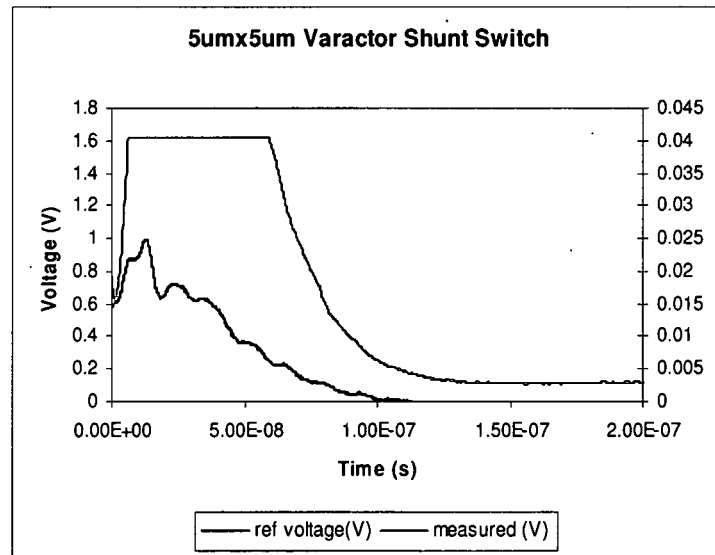
The rise time or fall time of the device is determined as follows [31][109]:

$$t_{device} = \left(t_{input}^2 - t_{output}^2 \right)^{\frac{1}{2}} \quad (5.13)$$

The switching speed has been determined to be approximately 43 ns based on rise and fall times of the devices.



(a)



(b)

Fig. 5.35 : Measured step response (a) rise time, and (b) fall time of the varactor shunt switch with an overlap area of $5 \times 5 \mu\text{m}^2$.

5.10 Applications

The ferroelectric materials of BST thin-films based capacitive shunt switch potentially can be used as switches, analog/continuous phase shifters, voltage controlled oscillator, tunable filters, impedance matching networks, wireless sensing devices and so on. Table 4 [29] shows the possible applications using the capacitive shunt switches in RF/Microwave applications.

Table 4 : Applications using capacitive shunt switches in RF/Microwave field.

Application	Frequency Range	Implementation	Attributes
Switching Device	1-100 GHz	Shunt switch (CPW), Si MMIC compatible	*Lower insertion loss for smaller devices
T/R switch	1-100 GHz	Shunt switch (CPW)	*20-25 dB isolation
Phase Shifter	1-100 GHz	Periodic Loading	*Analog, continuous *up to 75 deg/dB@ 5 GHz
Tunable filters	Microwave/millimeterwave	Periodic Loading	Low voltage tunable, CPW
Signal to Noise Enhancer	Microwave/Millimeterwave	Shunt Switch (CPW)	*High power signals allowed to pass thru
Tunable Impedance Matching Networks	Microwave/Millimeterwave	Periodic Loading + Stub	Voltage controlled Switches
Capacitive Sensors	Low Microwave	Shunt switch (CPW)	*Resonance frequency shift
Leakywave Antennas	Microwave/Millimeterwave	Shunt Switch array	Electronically Steerable

5.11 Performance comparison among solid state, RF MEMS and capacitive shunt switches

Table 5 [29] shows the performance comparison of the capacitive shunt switch with the solid state and RF MEMS switches.

Table 5 : Performance comparison among solid state Diodes, RF MEMS, and capacitive shunt switches.

Device characteristics and performance parameter	Solid state Diodes	RF MEMS Shunt switches (<u>Normally ON</u>)	Ferroelectric varactor shunt switch (<u>Normally OFF</u>)
Actuation voltage	Low (3-8V)	High(40-50V)	Low(<10V)
Switching speed	High(5-100ns)	Low (~10us)	High(<50ns)
Isolation	<20dB @20 GHz	>30dB @20 GHz	~20 dB @30 GHz
Insertion loss	>1 dB @20 GHz	<1 dB @30 GHz	~3 dB @30 GHz
Switching lifetime	High	Medium	High
Packaging cost	Low	Very high	Low
Power handling	Poor (0.5-5W)	Poor(<4.5W)	Poor (<5 W)
Power consumption	High (1-20mW)	Low	Very Low
Breakdown voltage	Low	Moderate	Low (<20 V)
Linearity	Low	High	High (expected)
IP3	Low(~+28dBm)	High(~+55dBm)	High (expected)
Integration capability	Very good	Good	Very good

5.12 Future research

BST thin-film based capacitive shunt switch is a new development in RF/Microwave fields. This section describes some of the potential research using the switches.

5.12.1 Sensor integration for remote activation and integration

One of the potential applications of the capacitive shunt switch is in wireless sensing. The ferroelectric varactor capacitive shunt switch can be used as a sensor because of the piezo-electric nature of the ferroelectric thin-films, which can be used for mass sensitive measurements such as force, pressure, or acceleration. Since the switches are very small area switches, arrays of such switches can be placed on a small area for effective sensing. Reference switches, which are not loaded, can be used for calibration purposes with the idea of removing the effects of temperature, humidity, etc., and effectively establishing a baseline. Any changes in the sensing switches in comparison with the reference switches could be effectively detected.

Theoretical model will be performed for the surface charge in the ferroelectric thin-film, taking into account the effects of mass loading, for a fixed strain, isothermal condition. Integrating with a rectifying antenna (rectenna), the sensor can be used for remote activation and interrogation. Issues such as calibration, minimum and maximum detection levels, sensitivity, and selectivity need to be addressed during the design.

A method of wireless activation and sensing can also be explored with a rectifying antenna integrated with the sensor network, as shown in Fig. 5.36. For simplicity, only one of the sensors is shown being remotely activated and integrated. The rectifying antenna converts the RF/microwave signal into a dc bias voltage, which will activate the switch network and allows for remote activation and integration. The bias voltage from the rectenna [110]-[116] will be applied to both the reference and the measurement sensor. The difference between the two gives us the indication on the measurand. Different types of

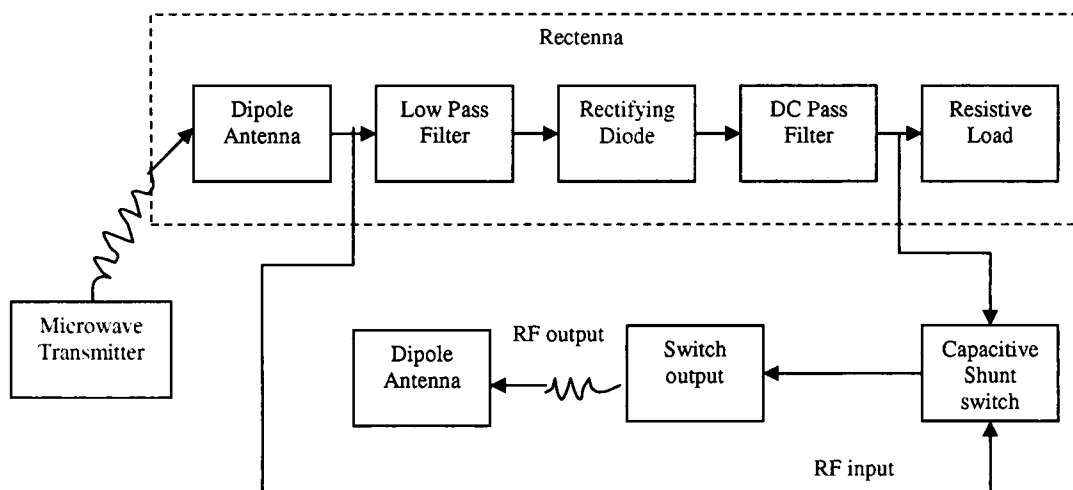


Fig. 5.36 : Rectifying antenna with switch for remote activation and integration.

rectifying antenna (rectennas) are used to convert RF-to-dc power at different frequencies. A circular polarized (CP) dipole rectenna can be used as it enables the receive or transmit antennas to be rotated without changing the output voltage [113],[115],[116]. The rectennas contain the several elements such as

dipole antennas, band reject filter (LPF), rectifying diode, low-pass filter (LPF), and a resistive load.

5.12.2 Low frequency applications

The varactor-based capacitive shunt switch can be used at a low frequency (<5 GHz) switching applications with a high isolation (>20 dB) and low insertion loss (<1 dB). One can obtain the maximum isolation and minimum insertion at low frequency by changing the capacitance of the varactor and series inductance of the shunt line. High series inductance increases the isolation as well as insertion loss. A longer shunt line is required to get the higher inductance which will give the high isolation. The overlap capacitance and series inductance of the shunt line need to be optimized to obtain the higher isolation and lower insertion loss at a low frequency.

To use this device at low frequency applications with high isolation and low insertion loss, a cascade switch can be used. Fig. 5.37 shows the device modeling for low frequency applications with high isolation in the OFF state and low insertion loss in the ON state. Simulations have been performed using AWR's Microwave Office. Capacitance of the varactor and series inductance of the shunt line required are approximately 1.73 pF (OFF), 0.23 pF (ON) and 0.446nH to obtain the higher isolation in the OFF state and the lower insertion loss in the ON state. From the simulation results in Fig. 5.38, one can see that

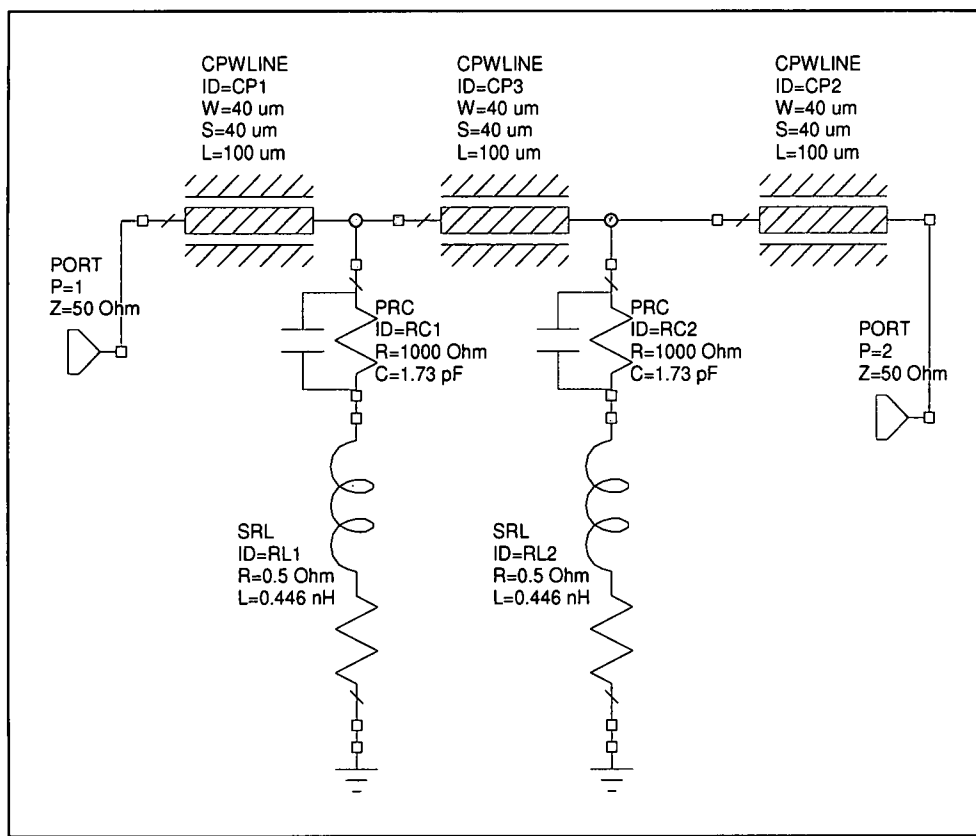


Fig. 5.37 : Device modeling for low frequency applications.

the isolation and insertion loss approximately 20 dB and 0.8916 dB respectively at 5 GHz. To get the above response we need a high quality thin-film which gives at least tunability 7:1. A meander line can be used to increase the inductance of the shunt line.

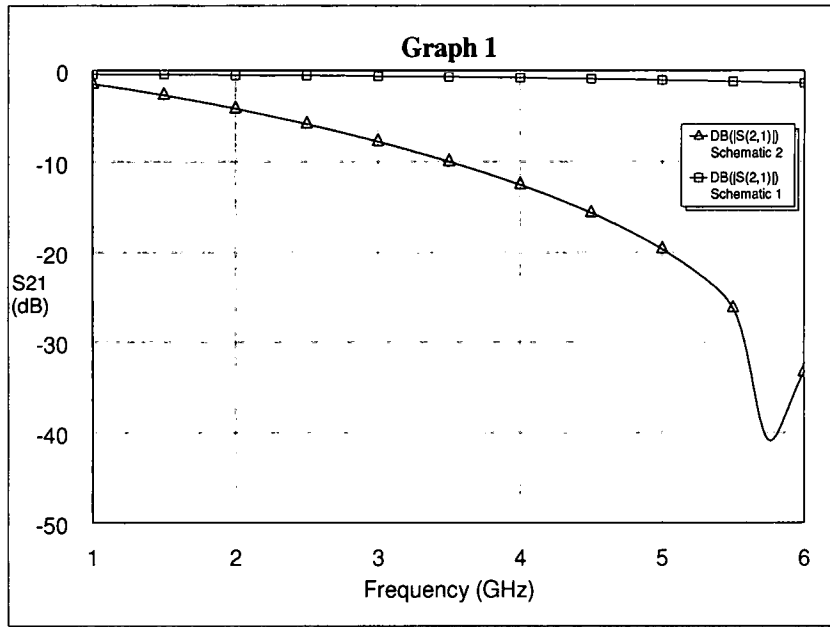


Fig. 5.38 : Simulated isolation (blue) in the OFF state and insertion loss (red) in the ON state of the cascaded capacitive shunt switches shown in Fig. 5.37.

5.12.3 Tunable filters

Ferroelectric materials of BST thin-films based capacitive shunt switches can be used as a tunable filter. The switch needs to be periodic loaded with the transmission lines according to Fig. 5.39. According to the type of filters

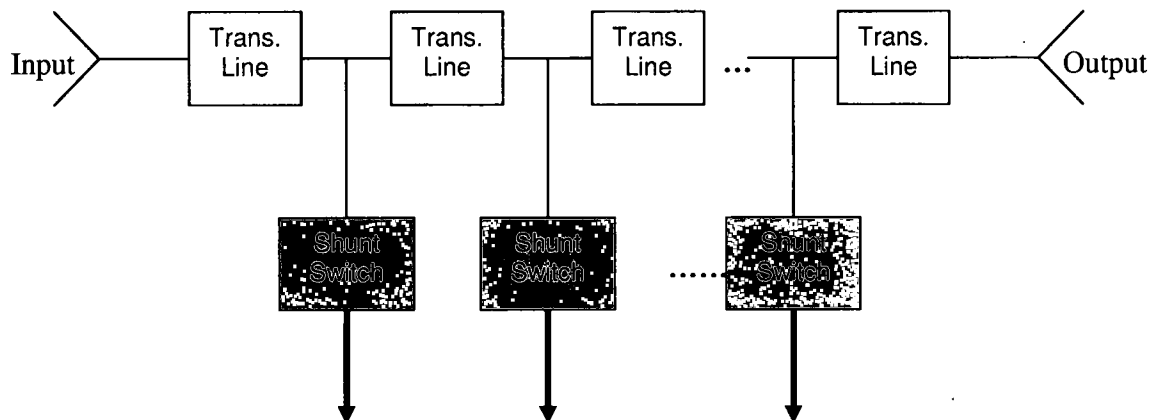


Fig. 5.39 : Switches periodically loaded with the transmission line as tunable filters.

implementation, the number of capacitive shunt switches are periodically loaded with the transmission line.

CHAPTER VI

CHARACTERIZATION OF THE BST THIN-FILMS BASED INTERDIGITAL CAPACITORS

6 Introduction

Conventionally, the parallel plate capacitor is the fundamental structure for many ferroelectric film-based devices but in recent years, there has been considerable research interest in developing ferroelectric thin-films based coplanar devices, i.e. devices with both electrodes on the surface of the ferroelectric film and no electrode layer between the film and the substrate [53]. Interdigital capacitors (IDCs) are one of the most promising components in microwave applications. They are widely used as lumped elements in monolithic microwave integrated circuits (MMICs) [117], slow wave devices, integrated optical (IO) modulators, deflectors, thin-film accoustoelectronic transducers [118], tunable devices, and dielectric characterization of thin films [119]. Recently, ferroelectric thin-films of Barium Strontium Titanate (BST) have initiated a renewed interest toward the electrically tunable devices based on interdigital capacitors [5].

This section describes the design techniques for the high voltage varactors that are designed on the multilayer substrates with a CPW configuration based on the tunable dielectric thin-films such as Barium Strontium Titanate (BST). From our recent work on tunable microwave devices, BST thin-films fabricated at the AFRL Materials and manufacturing directorate showed a large dielectric tunability as high as 4:1 in parallel plate varactor structure. The relative dielectric constant of the BST thin-films at zero-bias is ~ 500 and reduces to ~ 120 with a biasing dc electric field approximately 250 kV/cm. In this section, we discuss the design issues, modeling, theoretical analysis, optimization, electromagnetic simulation and experimental results of the interdigital capacitors.

6.1 Design

In this design, if we assume that 400 V will be the voltage that gives the maximum bias electric field of 250 kV/cm, the required spacing between electrodes can be calculated as 16 μm . Since it is impractical to implement a 16 μm thick parallel plate varactor, planar varactors have been selected for the implementation of the high voltage varactors. Among the planar varactors, we have the following choices: 1. gap capacitors with coplanar electrodes; and 2. interdigital capacitors (IDCs). Recent work by Yoon et al. has showed that reduced intermodulation distortion is possible with coplanar gap capacitors with careful design of dc bias schemes [120]. Highly resistive bias lines has been used to bias the gap capacitor without attenuating the RF signal [120]. The IDCs are suitable for the high voltage varactors as we can easily synthesize varactors

with different values. It is determined by our group that the IDCs offer the potential for higher tunability and ease of design. We have focused our attention on the design of interdigital capacitor (IDC) using Sonnet™ electromagnetic simulation tools. Theoretical and electromagnetic simulation models are considered and the results have been compared with the experimental data. The results are demonstrated the accuracy of these models. Based on the models and electromagnetic simulations performed, several IDCs are designed for a step and repeat 4"x4" mask plate.

The IDCs are designed on multilayer substrate with CPW transmission line configuration. Fig. 6.1 and Fig. 6.2 show the different layers structure and top view of the IDC respectively. To get the 50Ω characteristic impedance, the width of the feed line and spacing between the feed line and ground conductors of the CPW line has been taken 75 μm and 62.5 μm respectively.

Metal (P/Au/Pt) (1 μm)
BST (400nm)
SiO ₂ (300nm)
High resistivity Si Substrate (500μm)

Fig. 6.1 : Structure of the IDC showing the different layers

The general structure of the interdigital capacitor is shown in Fig. 6.2. The long conductors or “fingers” provide coupling between the input and output ports across the gaps. In general, the gaps (S)/spacing between the fingers and at the end of the fingers (S_{end}) may also be different but in this current design is assumed to be the same. The length (L) and the width (W) of the fingers are also specified. Also for the analysis purpose, the width (W) of the fingers and the width (W_1) of the terminal are assumed to be the same. Since the conductors are deposited on the multilayer substrates, its characteristics will also effect on performance. Of particular importance are the thickness of the substrates and its dielectric constant. The electrode spacing, width, length, thickness of the electrode (finger) and number of fingers have different influences on the capacitance. The influence of the film thickness on the IDC capacitance varies as the film property changes [55].

6.2 Modeling

Compared with parallel plate capacitors, the capacitance of an interdigital capacitor (IDC) is determined by many more geometrical parameters as shown in Fig. 6.2. Theoretical work has been done and various models have been developed to reveal the dependence of the capacitance on electrode configuration [119]. In our work, we chose the model described in [119] and [120] to calculate the capacitance of IDCs. The IDCs have been fabricated on a layered structure of BST/SiO₂/Si substrates. A top BST layer, which is planned to be deposited, using a shadow mask, can improve the effective dielectric constant

and the overall dielectric tunability of the IDC. A dielectric tunability of 4:1 results in a capacitance changes in the IDC of $\sim 2.5:1$. Fig. 6.3 shows the electrical modeling of the IDC shown in Fig. 6.2. In Fig. 6.3, C_1 is the capacitance of the IDC and R is the shunt resistance with C_1 for the BST thin-films and also C_2 , R_s , L_s are the parasitic capacitance, series resistance and series inductance of the IDC respectively. The capacitance of the interdigital capacitor has been calculated using [118] and [54]. The line parameters of the transmission line and IDCs have been evaluated using [97] and [123] for the electrical modeling.

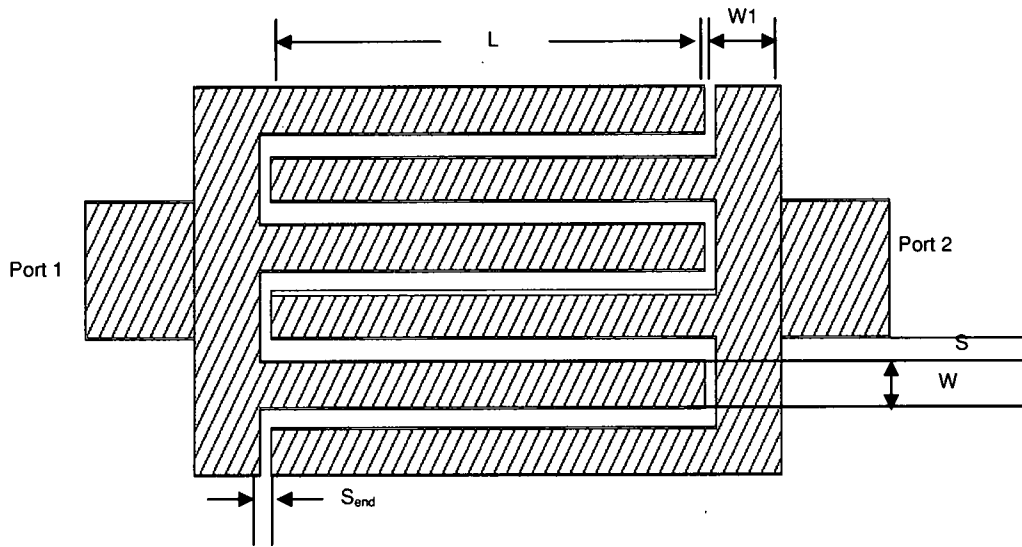


Fig. 6.2 : General structure of the IDC.

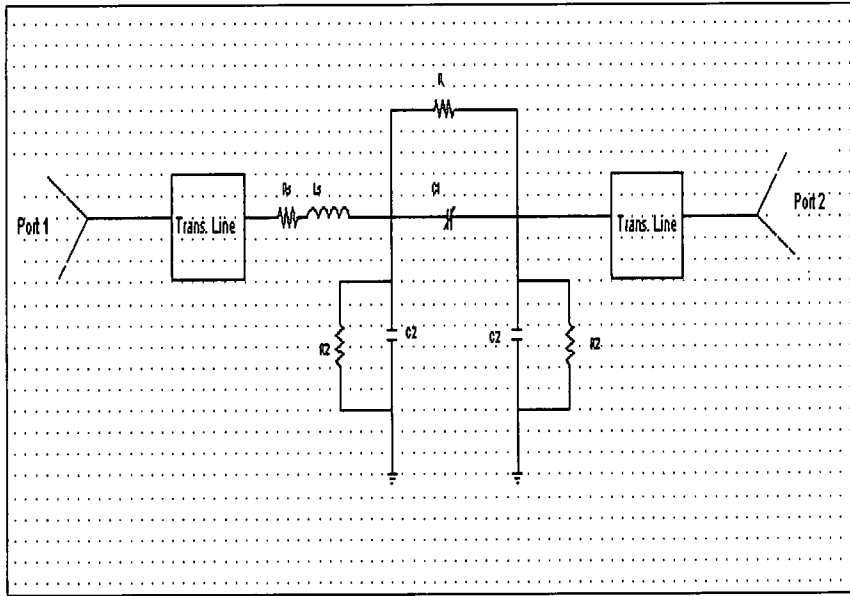


Fig. 6.3 : Electrical model for the IDC described in Fig. 6.2.

6.3 Theoretical analysis

The conformal mapping technique [118] is used to evaluate the closed form expression for capacitance of the IDCs. The derivation is based on the partial capacitance method [54],[118],[121],[122] and takes into account the capacitance between the fingers and the fringing capacitance of the finger ends. The total capacitance of the interdigital capacitor can be considered as the sum of the capacitance between the fingers plus capacitance of the outer edge finger ends [117] and the end part of each finger [55]. The total capacitance, C_{tot} of the interdigital capacitor can be expressed as:

$$C_{tot} = C_n + C_1 + C_2 \quad (6.1)$$

Where C_n is the capacitance of the periodical section, $C1$ is the capacitance of the outer edge finger ends and $C2$ is the capacitance of the end part of each section. C_n can be expressed using [5] for the finger number $n \geq 4$ as follows:

$$C_n = (n-3)\epsilon_0\epsilon_{eff} \frac{K(k_0)}{K(k'_0)} L \quad (6.2)$$

where L is the length of the finger and n is the number of fingers and also ϵ_{eff} is the effective dielectric constant and can be defined is as follows:

$$\epsilon_{eff} = 1 + 0.5(\epsilon_1 - 1)q_1 + 0.5(\epsilon_2 - \epsilon_1)q_2 + 0.5(\epsilon_3 - \epsilon_2)q_3 \quad (6.3)$$

where ϵ_1 , ϵ_2 , and ϵ_3 are the dielectric constant of the Si, SiO₂, and BST thin-films respectively. Also q_1 , q_2 , and q_3 are the filling factors of the Si, SiO₂, and BST thin-films and can be calculated by the following:

$$q_i = \frac{K(k_i)}{K(k'_i)} \frac{K(k'_0)}{K(k_0)} \quad (6.4)$$

where $K(k)$ is the complete elliptic integral of first kind with modulus k , k' the complementary modulus, $k' = \sqrt{1-k^2}$. Here, $k_0 = \frac{W}{W+2S} \sqrt{\frac{2W}{2W+S}}$ and k_i can be defined as;

$$k_i = \frac{\sinh\left(\frac{\pi W}{4h_i}\right)}{\sinh\left(\frac{\pi(W+S)}{4h_i}\right)} \sqrt{\frac{\cosh^2\left(\frac{\pi(W+S)}{4h_i}\right) + \sinh^2\left(\frac{\pi(W+S)}{4h_i}\right)}{\cosh^2\left(\frac{\pi W}{4h_i}\right) + \sinh^2\left(\frac{\pi(W+S)}{4h_i}\right)}} \quad (6.4)$$

where $i=1, 2, 3$, and h is the height of the different layers. The capacitance of the outer edge finger ends, $C1$ can be defined as follows:

$$C1 = 4\epsilon_0\epsilon_e \frac{K(k'_{0f})}{K(k_{0f})} L \quad (6.5)$$

where ϵ_e is the effective dielectric constant given by;

$$\epsilon_e = 1 + 0.5(\epsilon_1 - 1)qf_1 + 0.5(\epsilon_2 - \epsilon_1)qf_2 + 0.5(\epsilon_3 - \epsilon_2)qf_3 \quad (6.6)$$

$$\text{Here, } qf_i = \frac{K(k_{if})}{K(k'_{if})} \frac{K(k'_{0f})}{K(k_{0f})} \text{ and } k_{0f} = \frac{W}{W+2S} \sqrt{\frac{1 - \left(\frac{W+2S}{W+2W1+2S}\right)^2}{1 - \left(\frac{W}{W+2W1+2S}\right)^2}} \text{ and also}$$

$$k_{if} = \frac{\sinh\left(\frac{\pi W}{4h_i}\right)}{\sinh\left(\frac{\pi(W+2S)}{4h_i}\right)} \sqrt{\frac{1 - \sinh^2\left(\frac{\pi(W+2S)}{4h_i}\right)}{1 - \sinh^2\left(\frac{\pi W}{4h_i}\right)} \frac{\sinh^2\left(\frac{\pi(W+2W1+2S)}{4h_i}\right)}{\sinh^2\left(\frac{\pi(W+2W1+2S)}{4h_i}\right)}}$$

where $i=1, 2, \text{ and } 3$

The capacitance of the end part of n fingers can be obtained from [55] :

$$C2 = n\epsilon_0\epsilon_{eff} \frac{K(k_0)}{K(k'_0)} L_{ext} \quad (6.7)$$

Here,

$$L_{ext} = \frac{A}{12.5 \times 10^{-6}} \times \left[-4 \times 10^{-6} (S/2A)^2 + 9 \times 10^{-6} (S/2A) + 8 \times 10^{-6} \right] \times \left[1 + \left(\frac{A}{W1+A} \right)^3 \right]$$

$$\text{where } A = \frac{S+2W}{4}.$$

The capacitance of the interdigital capacitors has been calculated based on the above expressions. If the substrates layer thickness is very thin, the above

expression gives an error in determining the filling factor; in that case an assumption [121] is made to calculate the filling factor.

6.4 Results and discussion

The capacitance of the interdigital capacitor depends on the finger length, spacing between the fingers, width of the finger, number of the fingers, thickness and dielectric constant of the thin-films. Fig. 6.4 shows the variation of the capacitance with the length of the finger of the interdigital capacitor. The higher the length of the fingers, the higher the capacitance of the IDCs. One can see in Fig. 6.5 that smaller the spacing between the fingers results in the higher capacitance. Capacitance increases with increasing the number of the fingers (Fig. 6.6). Conformal mapping technique [118],[119] is used to obtain the dielectric constant of the BST thin-films. Fig. 6.7 shows the dielectric constant with the capacitance of the interdigital capacitors. From Fig. 6.7, we see that dielectric constant of the BST thin-films increases with increasing the capacitance. Fig. 6.8 shows the compared S_{21} values with frequency among the simulation, experimental data, theoretical analysis, and lumped element model using both SonnetTM electromagnetic simulation tools and Microwave office. From Fig. 6.8, we also see that the experimental results and electrical modeling (lumped element) results using Microwave Office and SonnetTM are quite close but there is a small difference between the theoretical (Matlab), and experimental results due to couple of assumptions that have been made to evaluate the

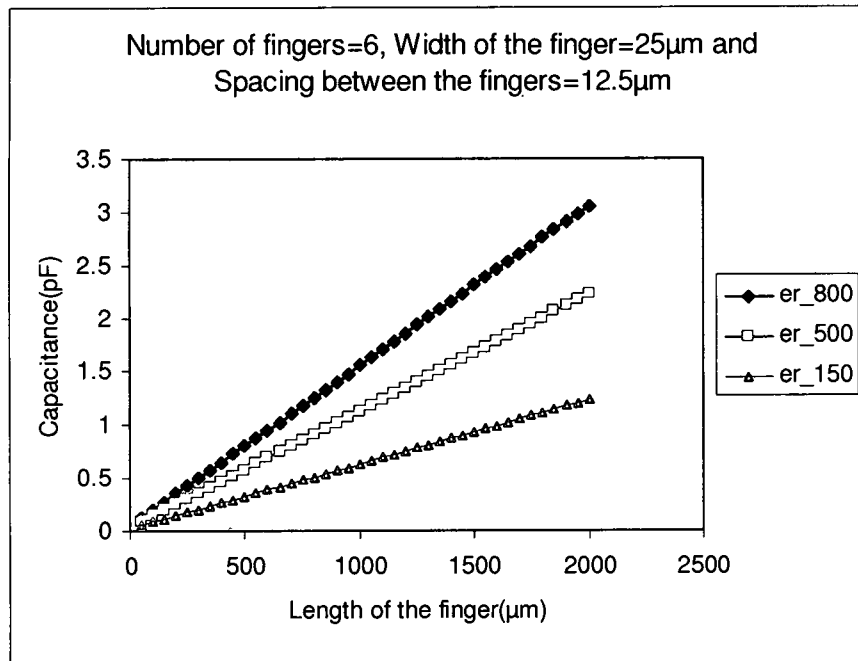


Fig. 6.4 : Variation of the capacitance with the length of the finger.

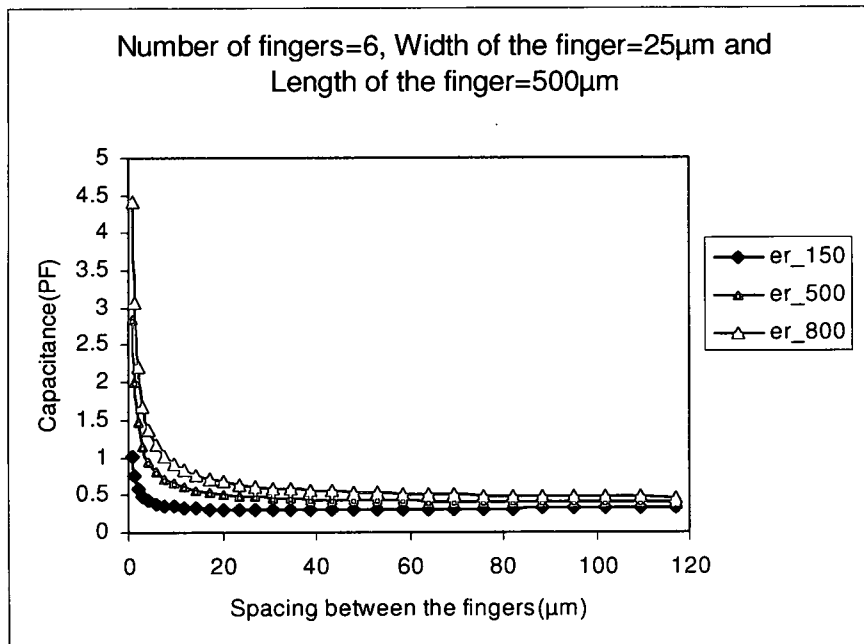


Fig. 6.5 : Capacitance versus spacing between the fingers of the IDCs.

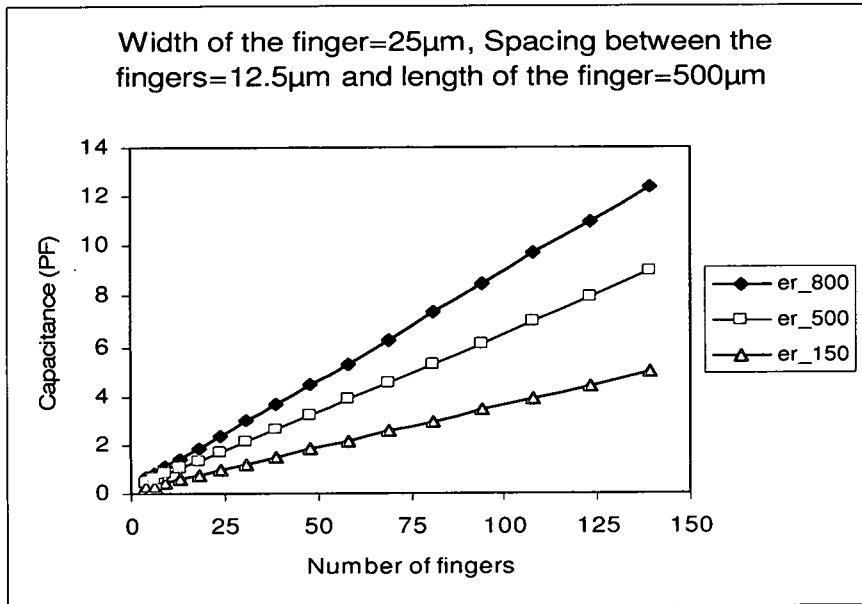


Fig. 6.6 : Variation of the capacitance with the number of the fingers.

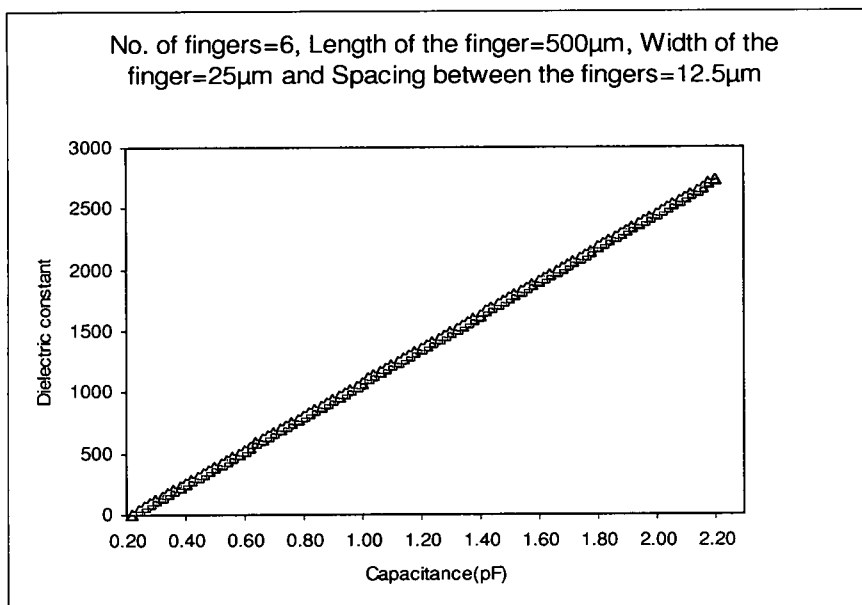


Fig. 6.7 : Dielectric constant versus the capacitance of the BST thin-films of the interdigital capacitors. This figure can be used in determining the dielectric constant of the BST layer once we know the capacitance of the IDC.

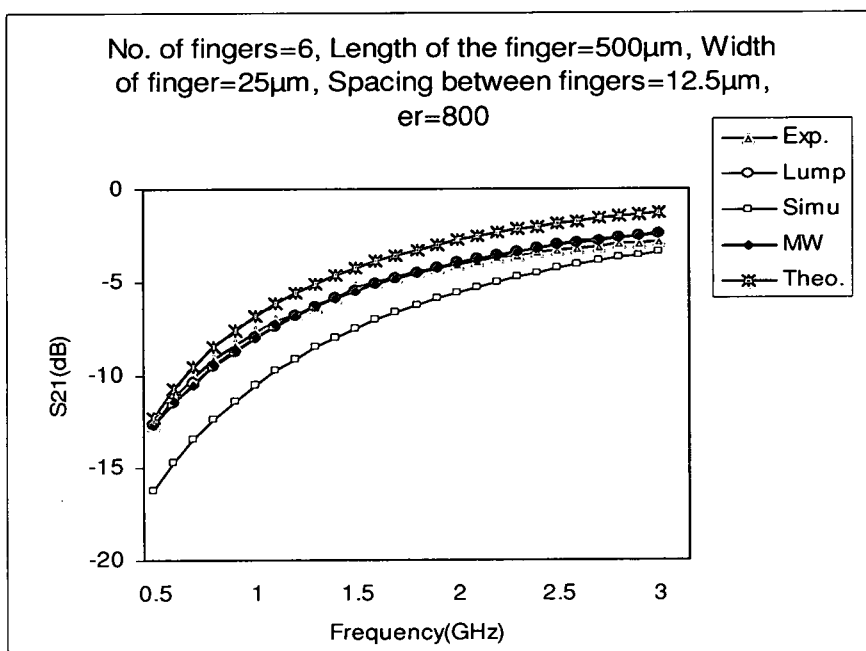


Fig. 6.8 : S_{21} value versus frequency for the interdigital capacitance.

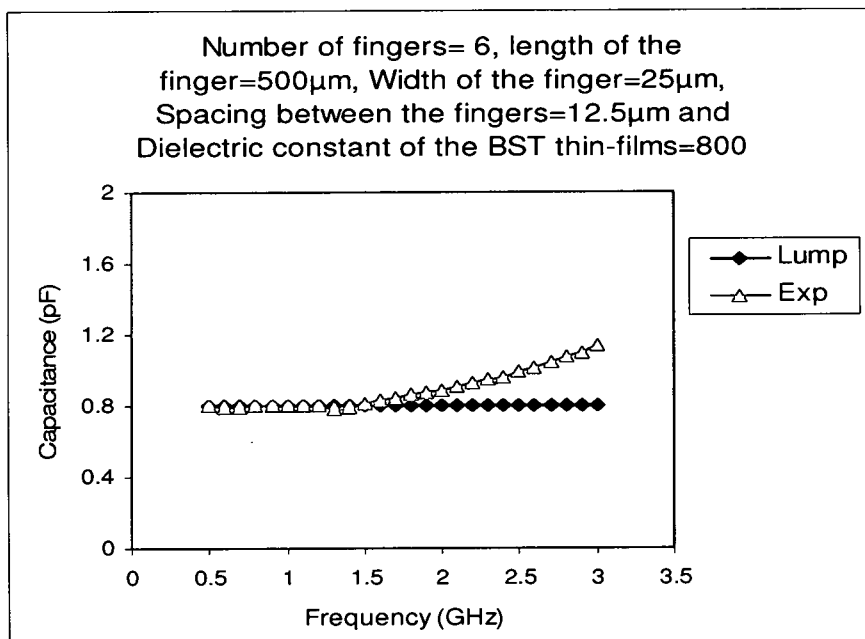
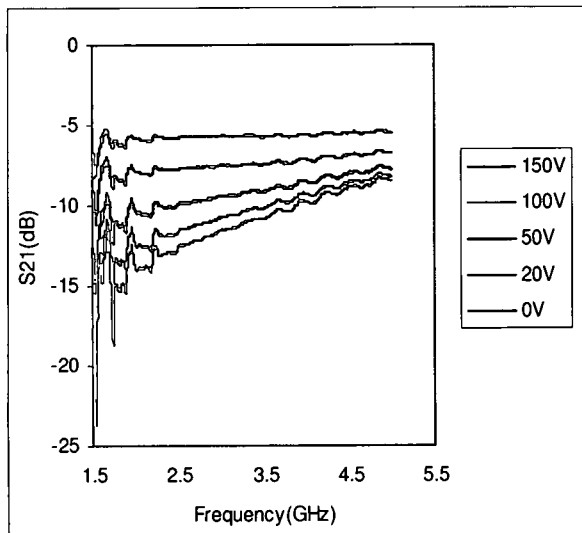


Fig. 6.9 : Extracted capacitance from S_{21} versus frequency.

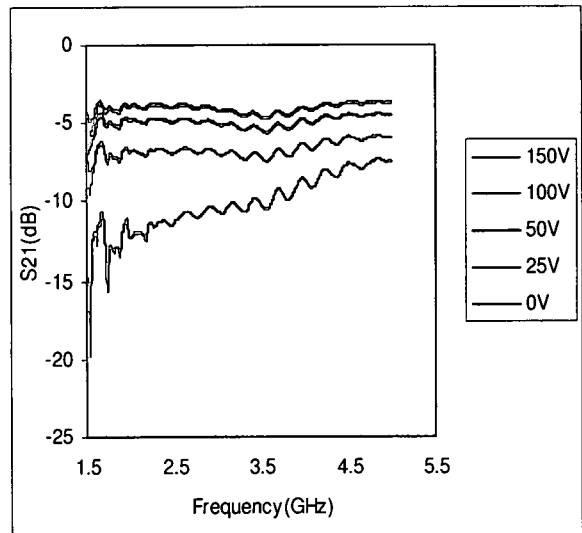
theoretical S_{21} . We also see from Fig. 6.8 that a large difference is observed between the simulation and experimental results due to the lower capacitance value in the electromagnetic simulation results created by the other parasitic effects. Fig. 6.9 shows the extracted capacitance from the S_{21} values based on the theoretical analysis. From Fig. 6.9, one can observe that the extracted capacitance values between the experimental and lumped model are closer to each other at the lower frequency but at the higher frequency, the capacitance values are different because of the simplified lumped element model used to extract the capacitance from the S_{21} data.

A large number of devices (IDC's) have been tested with a high voltage bias tee at NASA Glen Research Center and data are analyzed using the simplified model. Fig. 6.10 shows the experimental swept frequency S_{21} with different voltages for the several devices. From Fig. 6.10, we see that the value of S_{21} is not quite accurate at the lower frequency due to the effect of the bias. The capacitance of the IDC is extracted from S_{21} value (Fig. 6.10) based on the simplified electrical model. Fig. 6.11 shows the extracted capacitance from the experimental S_{21} (Fig. 6.10) data with frequency for the different devices. The extracted capacitance has been plotted from 2 GHz because of the high voltage bias tee effect at the lower frequency. More than 3:1 capacitance tunability $((C(0)-C(V))/C(0))$ has been obtained for all the devices of the IDC is shown in Fig. 6.11. The maximum and minimum voltages are applied 150 V and 0 V for all the devices (reference to Fig. 6.10 and Fig. 6.11). Theoretical results (Fig. 6.12)

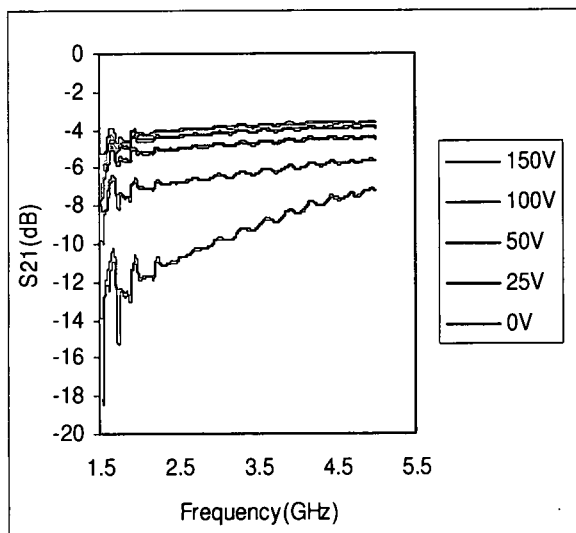
show that the capacitance of the IDC can be improved using two layers (top and bottom) of BST thin-films instead of single layer. Fig. 6.12 shows clearly that the capacitance increases with two layers (tbst as shown in Fig. 6.12) BST thin-films when compared with the single layer (BST as shown in Fig. 6.12) BST thin-films for the variation of the different parameters of the IDC.



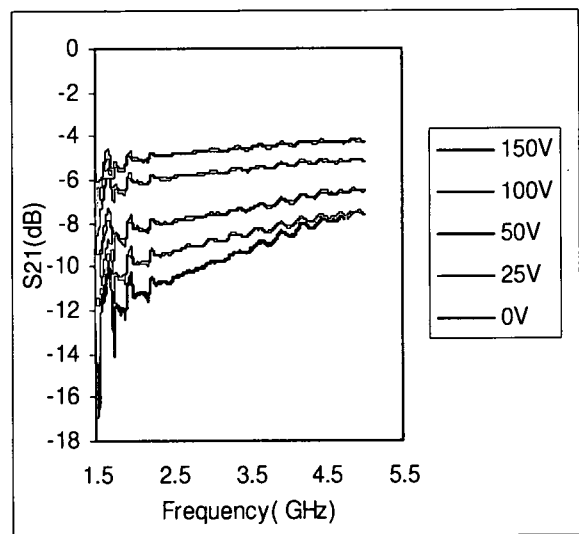
(a)



(b)

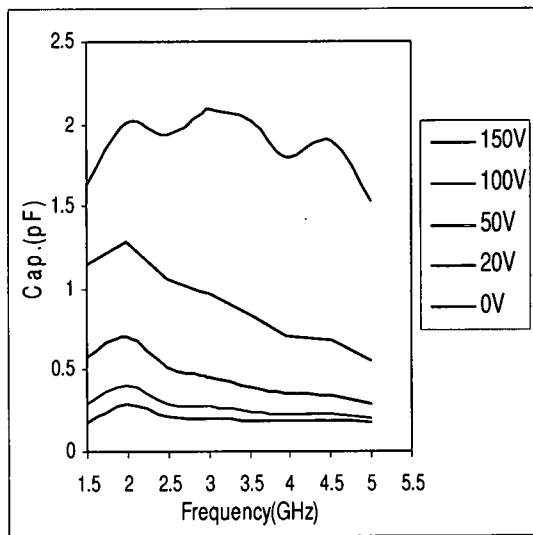


(c)

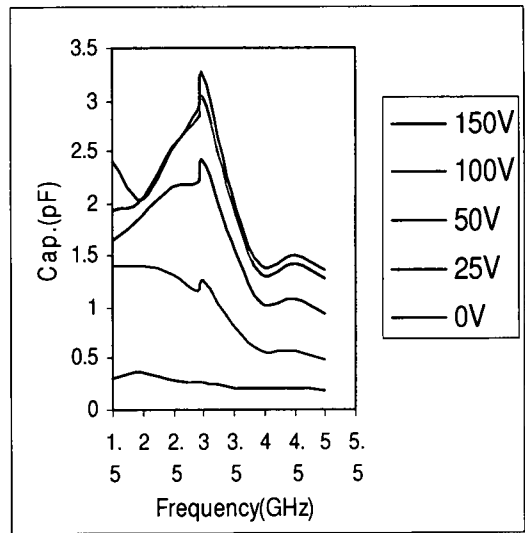


(d)

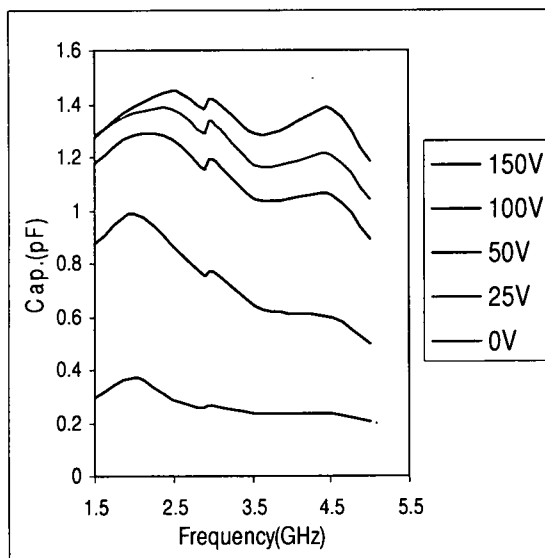
Fig. 6.10 : Experimental swept frequency S_{21} with different voltages for (a) device 3, (b) device 6, (c) device 9, and (d) device 10.



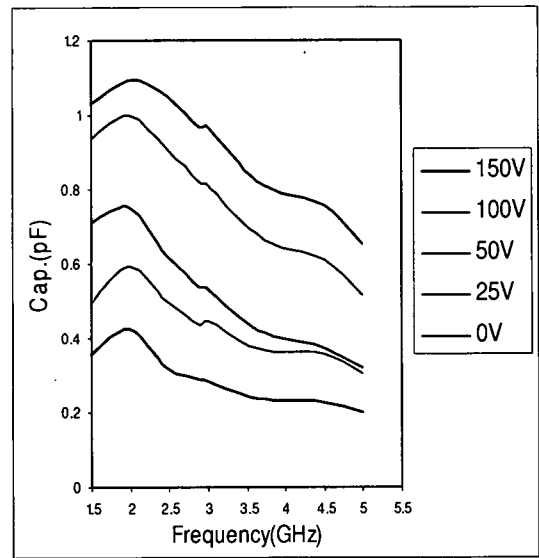
(a)



(b)

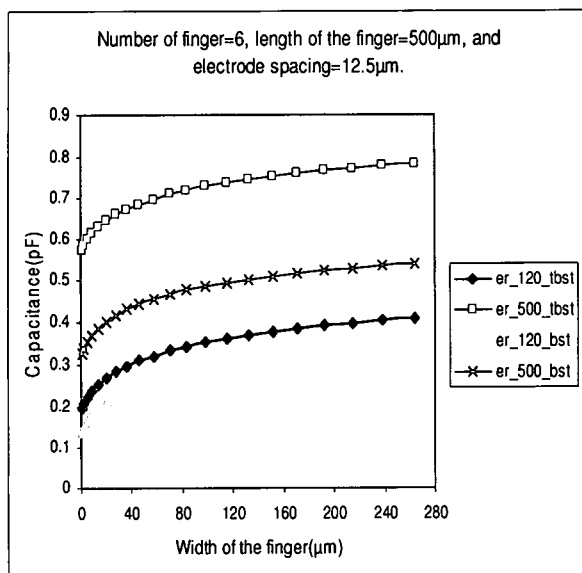


(c)

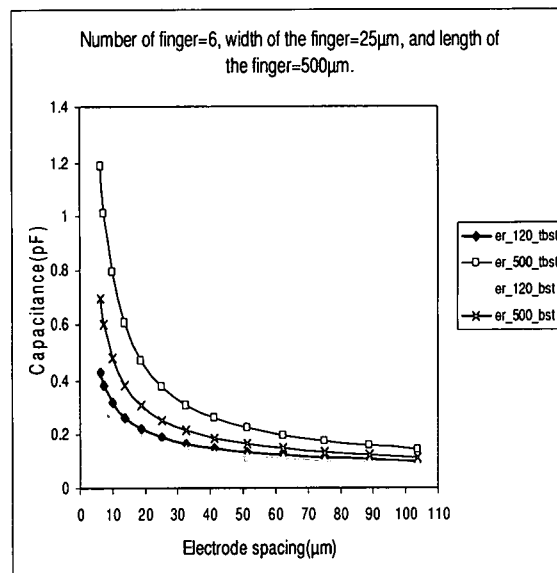


(d)

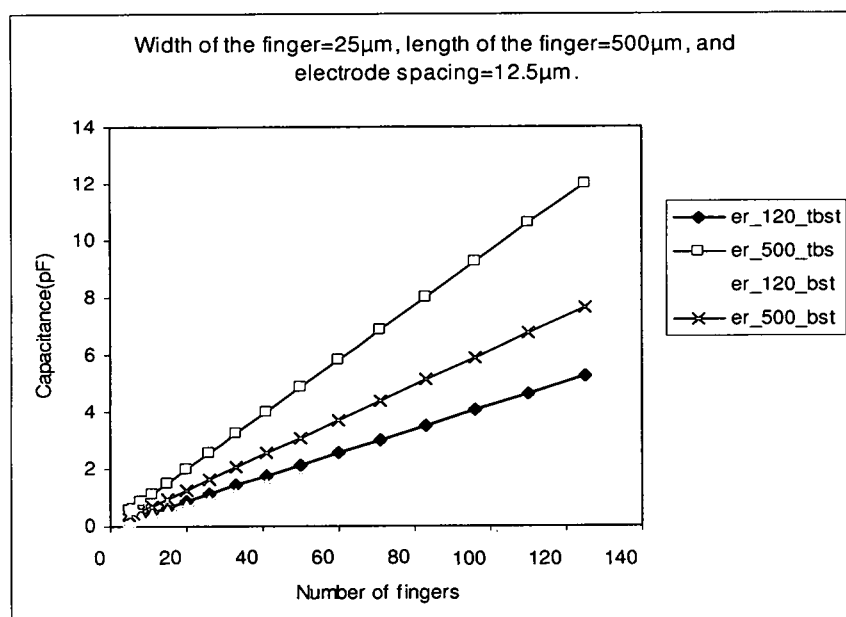
Fig. 6.11 : Extracted capacitance with frequency at the different voltages for (a) device 3, (b) device 6, (c) device 9, and (d) device 10.



(a)



(b)



(c)

Fig. 6.12 : Comparison of capacitance of two layered BST thin-film based IDC and a single layer BST thin-film IDC.

6.5 Conclusions

Design, modeling, optimization, simulation, theoretical analysis, and experimental verification of the BST thin-films based interdigital capacitors are discussed and presented here. The experimental results are much closer to the electrical model based on theoretical analysis. This section also provided the general model of the IDC and that is quite independent of the particular application and can be applied for any spacing, number of fingers, and width of the fingers and for any number of layers with different thickness and dielectric constant.

CHAPTER VII

SUMMARY AND CONCLUSIONS

This dissertation has successfully demonstrated a BST thin-film based capacitive shunt switch for tunable/reconfigurable circuits. Design, theory of operation, simulations, modeling, theoretical analysis, fabrication, optimization, and experimental results of the capacitive shunt switches have been discussed and presented in this dissertation work. The switch is designed on a multilayer substrate with a CPW transmission line configuration. The normally OFF capacitive shunt switch is a simple device when compared with the normally ON RF MEMS shunt switches. The varactor shunt switch is turned ON by the application of a dc bias voltage which reduces the loading varactor capacitance to a minimum. The switching performance depends on the dielectric tunability of the BST thin-films. A ferroelectric material of $\text{Ba}_{0.6}\text{Sr}_{0.4}\text{TiO}_3$ thin-film with a composition ratio 60/40 (Ba/Sr) is used for all the devices, and deposited on the entire surface. A pulsed laser deposition method is used to deposit the BST thin-films at 75 mT oxygen partial pressure and 750 degrees C processing temperature with an average grain size of 60 nm. The devices have been fabricated on high resistivity ($>6 \text{ K}\Omega\text{-cm}$) Si substrates.

Simulation results, theoretical analysis, and experimental results have been provided the proof for the switching concept. The capacitor shunt switches with different varactor areas ranging from $2.5 \times 2.5 \mu\text{m}^2$ to $17.5 \times 17.5 \mu\text{m}^2$ are designed, simulated, fabricated, and tested. SonnetTM tools are used to perform the electromagnetic simulations and devices are tested using HP8510 and HP8720B Vector Network Analyzer (VNA) over a wide frequency range from 1 to 45 GHz. The dielectric constant of the BST thin-films is reduced from 500 (0 V) to 120 (~10 V) by applying a dc voltage. Also, loss tangent of the BST thin-films is ~0.045 at 0 V and reduced to ~0.03 at 10 V. The capacitance of the varactor shunt switches are tunable and obtained more than 4:1 tunability for all the devices with a dc bias voltage below 12 V. The capacitance value depends on the varactor area, dielectric constant of the BST thin-films and thickness of the dielectric layer. Larger varactor areas result in better isolation in the OFF state, with higher insertion loss in the ON state of the device. Experimental results showed that the isolation of a switch with a varactor area of $75 \mu\text{m}^2$ is approximately 20 dB and insertion loss is below 4.5 dB at 35 GHz. The electrical parameters have been extracted using AWR's Microwave Office and showed the equivalent-series resistance (ESR), and equivalent series inductance (ESL) are bias dependent for the smaller devices. The switching speed of the devices has been estimated to be approximately 43 ns based on the fall and rise times. One can improve the device performance by using the selective area deposition of the BST thin-films instead of the entire surface.

The varactor-based capacitive shunt switch is very simple in nature and easy to fabricate when compared with the RF MEMS and solid state switches. The device can be easily integrated with other active and passive components for RF/Microwave applications. The switch has a higher switching life time, power handling capability, less packaging cost, and very low biasing voltage when compared with RF MEMS switches.

The ferroelectric thin-film based capacitive shunt switch can be used such as microwave/millimeterwave switches, circulators, tunable/reconfigurable filters, continuous analog phase shifters, voltage controlled oscillators and wireless sensors. The switch could also be used at low frequency applications by using the higher series inductance of the shunt line. Since, this is the first time this type of a switch is being reported in RF/Microwave applications, therefore, many opportunities exist for future research using this device.

Appendix A

Let the capacitance of the ground pad and varactor are C and C_1 respectively. (sections 5.3 and 5.6). Also let the impedance of the ground pad, varactor and total be Z_g , Z_v and Z_T . Since the ground pad capacitance is in series with the varactor capacitance, so, therefore, we can write,

$$Z_T = Z_g + Z_v \quad (1A)$$

We can write the impedance in terms of capacitance,

$$\frac{1}{j\omega C_T} = \frac{1}{j\omega C} + \frac{1}{j\omega C_1}$$

$$\text{or, } \frac{1}{C_T} = \frac{C + C_1}{CC_1}$$

$$\text{or, } \frac{1}{C_T} = \frac{1}{C_1} + \frac{1}{C} \quad (2A)$$

(Dividing by CC_1 both denominator and numerator in the right side)

If $C_1 \gg C$, then $\frac{1}{C_1} \approx 0$, so, Eq. (2A) reduces to

$$\frac{1}{C_T} = \frac{1}{C}$$

$$C_T = C$$

So, therefore, total capacitance would be the smaller one. Since the large ground pad capacitance is in series with the varactor capacitance of the capacitive shunt switch, so, the effective capacitance would be the capacitance of the varactor.

Appendix B

Fig. 5.17 describes to determine the S-parameters of the ferroelectric varactor-based capacitive shunt switch. We can write the backward traveling wave in port 1 and port 2 is as follows,

$$V_1^- = S_{11}V_1^+ + S_{12}V_2^+ \quad (1B)$$

and

$$V_2^- = S_{22}V_2^+ + S_{21}V_1^+ \quad (2B)$$

From Eq. (1B), we get,

$$V_1^- = S_{11}V_1^+ + S_{12}V_2^+$$

$$\text{or, } S_{11} = \left. \frac{V_1^-}{V_1^+} \right|_{V_2^+=0} = \Gamma_{in} = \frac{Z_{in} - Z_s}{Z_{in} + Z_s} \quad (3B)$$

and

$$Z_{in} = (((Z_0 + Z_1) \parallel Z_2)) + Z_1 \quad (4B)$$

where Γ_{in} is the reflection coefficient at input port1, and Z_s is the source impedance which is equal to Z_0 . The reflection coefficient at port1 can be determined from S_{11} . After finding Z_{in} in Fig. 5.17 and substituting in Eq. (3B), one can easily write the reflection coefficient of S_{11} ;

$$S_{11} = \frac{(Z_0 + Z_1 + Z_2)(Z_1 - Z_0) + Z_2(Z_0 + Z_1)}{(Z_0 + Z_1)(Z_0 + Z_1 + 2Z_2)} \quad (5B)$$

Now, we know,

$$V_1 = V_1^- + V_1^+ = V_1^+ \left(1 + \frac{V_1^-}{V_1^+} \right) = V_1^+ (1 + S_{11})$$

$$\text{or, } V_1 = V_1^+ (1 + S_{11}) \quad (6B)$$

Again, we know,

$$V_2 = V_2^- + V_2^+$$

$$\text{or, } V_2 = V_2^-, (V_2^+ = 0)$$

Now we need to find out the voltage at port2 when applying at port1. So, we can write,

$$V_2^- = V_2 = \frac{V_1}{(Z_1 + Z')} * \frac{Z'}{(Z_0 + Z_1)} * Z_0 \quad (7B)$$

$$\text{where } Z' = Z_2 \parallel (Z_1 + Z_0)$$

Again, from Eq.(2B), we can write,

$$S_{21} = \left. \frac{V_2^-}{V_1^+} \right|_{V_2^+ = 0}$$

By using Eqs. (5B) (6B), (7B) and the value of Z' , we can easily write,

$$S_{21} = \frac{2Z_0 Z_2}{(Z_0 + Z_1)(Z_0 + Z_1 + 2Z_2)} \quad (8B)$$

Eq. (8B) describes the expression both for the isolation and insertion loss in the OFF and ON states of the varactor based capacitive shunt switch.

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