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Design and Fabrication of Passive Barium Strontium Titanate (BST) Thin Film Varactor Based Phase Shifters for Operation within a 5-15 GHz Bandwidth

Devin William Spatz
University of Dayton

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Honors Thesis

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Abstract

Two passive, analog phase control circuit designs utilizing ferroelectric varactors are presented. The tuning capabilities of single layer and parallel plate varactors deposited on a $Ba_{0.6}Sr_{0.4}TiO_3$ (BST) thin film are characterized. Phase control is demonstrated through cascading multiple shunt varactors along a coplanar waveguide (CPW) structure. Through the application of a 0V – 8V DC bias, the capacitance in the circuit is tuned to control the transmission phase shift (angle of S21). Simulations of both phase control device structures are performed in AWR Microwave Office and compared with measurement data. Both circuit and mathematical models are developed and compared to simulation results. Multiple phase shifter devices of a varying number of varactor segments are fabricated on a high resistivity Si or sapphire wafer. Standard microelectronic processing techniques are used for fabrication of the phase shifter circuit. BST thin film is deposited using a large area pulsed laser deposition (PLD) system available in our lab. All circuits are tested from 1 - 20 GHz using an on-wafer probe station and a vector network analyzer. The phase shifter design consisting of 20 parallel plate varactor segments achieved the highest figure of merit (FOM) of 27.54 degrees/dB at a frequency of 15 GHz.

Acknowledgements

First and foremost, I would like to thank my honors thesis adviser, Dr. Guru Subramanyam, for his time and dedication. Through his guidance, I have been able to gain experience in performing research and explore the field of microwave engineering as an independent study.

I would also like to thank all of my colleagues in the Microwave Electronics laboratory for their support and patience as I have undergone the thesis process. Hailing Yue has assisted me through every step of the thesis process including performing simulations, testing devices and analyzing results. I owe my understanding of device simulations to Shu Wang who taught me to use the AWR Microwave Office software. Additionally, Shu performed the BST deposition as part of the device fabrication process. I would also like to thank Kuan-Chang Pan who assisted me in the modeling of the varactor devices and taught me how to perform on wafer testing. I would have not been successful in completing this thesis if it wasn't for all of these people.

UNIVERSITY of DAYTON

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INTRODUCTION

Over the course of mid-to-late-20th century and continuing into the 21st century, wireless systems have undergone rapid development and have evolved from fixed frequency systems into complex multiple-input and multiple-output (MIMO) systems which operate across the frequency spectrum. This rapid development has enabled 3G and 4G wireless communications networks, sophisticated radio detection and ranging (RADAR) systems, and phased array antennas to emerge. As these technologies continue to develop, there is a growing need for "flexible" or "reconfigurable" electronics which allow systems ranging from mobile handsets all the way down to individual electrical components to change functionality while in the field. Examples of this include wireless transceivers that can operate on multiple frequency bands and frequency dependent components such as filters and antennas that can switch between center frequencies or pass and reject bands. One component of particular interest is the phase shifter circuit.

A phase shifter is a two port device that controls the transmission phase angle of an electrical network. From widespread use in telecommunications systems, RADAR, phased array antennas, and beam steering, phase control is an essential aspect of modern RF and microwave systems. Given this wide range of applications, "tunable" phase shifters offer the potential to meet application specific phase shifter requirements and in turn offer optimized system performance. As the development of RF and microwave systems continue, there is a growing interest in phase shifters with low insertion and return loss that have a consistent amplitude across the entire bandwidth of phase shifter operation. [1]

1.1 Objectives of this research

This thesis was conducted to demonstrate phase control using thin film Barium Strontium Titanate (BST) varactors. Building on parallel plate varactor research previously conducted by my lab group, single layer varactors were developed and tested alongside variations of the parallel plate varactor to further explore the behavior of BST thin film for phase shifter applications. Additionally, modeling of these single layer and parallel plate varactor devices through circuit schematics and mathematical models was explored in order to characterize the behavior of these ferroelectric varactors.

1.2 Why use Ferroelectric Varactors?

Thin film ferroelectric varactors have been frequently demonstrated in phase shifter design due their capacitance tuning ability with a very low (under 10V) DC biasing voltage. [2] This behavior is enabled through the use of nonlinear dielectric materials such as BST which was a focus of this thesis. Thin film BST exhibits a high dielectric constant ($\varepsilon_r = 500 - 700$) which can be reduced by up to a factor of 5 through the application of a low DC biasing voltage. [3] When integrated into a metal-insulator-metal (MIM) capacitor design, this results in a wide capacitance tuning range and in turn a high phase shift potential.

The varactors used in this thesis include both single layer and parallel plate designs. Both of these varactors use thin film BST as the insulating dielectric material. In the parallel plate design, the BST thin film is deposited between two conducting plates, while in the single layer design, the metal layer is deposited on top of the BST thin film layer. Despite this difference in fabrication process, the two varactor designs operate in the same manner. By cascading multiple single unit varactors, a transmission phase shift of 360 degrees is

demonstrated at ~15-18 GHz while the transmission loss is maintained at a stable level (-5 dB - -8 dB) as DC bias is increased from 0-10V. This results in a maximum observed figure of merit (FOM) of ~28 degrees/dB at ~15GHz, which represents a successful demonstration of phase shifter application.

1.3 BST Thin-Film Varactor Based Phase Shifters in Literature

Before establishing design criteria for the proposed phase shifters, a literature review was performed to survey recent and past phase shifter designs. Table 1 summarizes a number of papers that explore the use of thin film BST based varactors in phase shifter design. Criteria include the FOM, maximum phase shift produced, insertion loss and bias voltage are among the metrics compared. The selected papers show calculated FOM values between 20-110 degrees/dB with the most common FOM values falling in the 40-50 degrees/dB range. While having good FOM values at frequencies within the specified bandwidth for this thesis, these phase shifters require higher bias voltages (ranging from 20-90V) and produce relative phase shift between 60-260 degrees. This overview of thin film BST varactor based phase shifters displays the current strengths and weaknesses in phase shifter design.

Table 1: Overview of Thin Film BST Varactor Based Phase Shifters

Reference	FOM (°/dB)	Phase Shift (°)	Insertion Loss (dB)	Frequency (GHz)	Bias Voltage (V)	Substrate
[4]	31.13	84.67	-2.72	16	30	TiO2/Si
[4]	107.3	147	-1.37	16	50	TiO2/Si
[5]	44	260	-5.9	8	50	Al2O3
[6]	23	135	-5.9	60	30	Si
[6]	25	150	-5.9	60	90	Si
[7]	42	72	-1.7	10	20	Sapphire
[7]	49	120	-2.6	10	20	Sapphire

1.4 Scope

The main focus of this thesis is devoted to ferroelectric varactor tuned phase shifter development. BST ferroelectric varactors fabricated on a sapphire substrate are utilized in all phase shifter designs. Maximum phase shift and insertion loss over a bandwidth of 5 GHz - 15 GHz are of interest for simulations and testing as this range covers many common microwave devices. Device modeling is limited to single segment varactor devices and aims to model the device with and without an applied DC bias voltage.

1.5 Outline

This thesis begins with a literature review on phase shifter design. Chapter 2 presents background information on electrical phase angles, analog vs. digital phase control, types of phase shifters, and a provides a comparison of phase shifter technologies. Ferroelectric varactors and the properties of BST are emphasized in this section since they are the focus of this thesis. Chapter 3 covers an analysis of single layer and parallel plate varactors. First, the physical structures of each varactor type are presented and described in terms of electrical functionality. Next, both electrical and mathematical models are developed. These models are based upon existing literature and are adapted to the new device structure. In Chapter 4, simulations are run for the varactor based phase shifter devices. Device materials are specified and simulation methodologies are compared. Simulated S-parameter data for insertion loss and phase angle is compared between varactor designs. Electrical model extraction is performed using the simulated results. Chapter 5 explains the testing setup and experimental procedures. This includes brief details on the device fabrication process. Additionally, the test setup and vector network analyzer (VNA) calibration procedure is documented. Chapter 6 covers the results and

discussion where the experimental results for both varactor based phase shifters are presented and compared to simulated results. Finally, Chapter 7 states conclusions that are drawn from the thesis research and suggests recommendations for potential future work on the topic.

LITERATURE REVIEW

2.1 Introduction

The purpose of this section is to introduce phase shifter concepts and review different types of phase shifter technologies and designs that are commonly used in literature. As phase shifter research and development has continued over the past few decades, the number of technologies and topographies associated with phase shifter design continue to increase. The following sections will discuss the performance characteristics and behaviors of each aspect of phase shifter design.

2.2 Phase Angle

All electrical signals can be expressed in terms of magnitude and phase angle. These signal components are derived from the real and imaginary, or resistive and reactive, portions of a signal.

$$|R + jX| = \sqrt{R^2 + X^2} \tag{1}$$

$$\angle(R + jX) = \tan^{-1}\left(\frac{X}{R}\right) \tag{2}$$

Based solely on these expressions, either the resistive, R, or reactive, X, component of the signal impedance must be actively modified to control the phase angle of an electrical network. Modifying the resistive portion of the signal impedance is undesirable as this will increase/decrease the insertion loss, or energy dissipated, as a signal passes though the device. While this method would allow for the control of the phase shift angle, it would inadvertently cause the signal magnitude to be variable which is highly undesired in phase shifter development. This leaves two viable options: implement a variable inductance or a variable capacitance.

The first viable option in controlling the phase angle is implementing a variable inductor in the phase control circuit. Since inductance is purely reactive, the phase angle will be frequency dependent and additional power will not be dissipated in the device. The resulting phase angle is high at low frequencies but exponentially decreases towards zero as the input signal approaches microwave frequencies. As a result, there is little to no phase shift potential within the desired bandwidth. Additionally, tuning the inductance in such a circuit often requires active elements and is associated with high power consumption, both of which are outside the scope of this project. [2]

The second viable option in controlling the phase angle of a signal is utilizing a variable capacitor (varactor). Similar to an inductor, an ideal capacitor is purely reactive meaning that the phase shift angle is frequency dependent and power will not be dissipated. Unlike an inductor, the phase angle due to capacitance increases as the source frequency increases. For this reason, a variable capacitor is preferred since there is a high phase shift potential at microwave frequencies rather than at direct current (DC) to radio frequencies (RF).

2.3 Analog vs Digital Phase Shifters

In the development of any electrical system or device, analog and digital topologies must be considered for the optimization of device capabilities and performance. Analog devices have an infinite number of "states" within a specified range. In terms phase shifter design, this means that the amount of phase shift produced is continuously variable between a minimum and maximum phase shift angle. Advantages of analog topologies include reduced system inputs and increased system flexibility in terms of device states.

From an integration standpoint, analog devices require additional hardware such as an analog to digital converter (ADC) to be used in a digital system.

Contrarily, digital devices are based on a set of quantized states with a fixed resolution. In a binary system, these states are represented by bits, or 1's and 0's. In terms of phase shifter design, a digital topology translates to a set of discrete phase shift angles that are achievable by the device. This set of discrete phase shift angles is determined by multiple phase bits, or input lines. The downfall in this design methodology is that the insertion loss in a digital phase shifter is associated with the number of bits of resolution of the device to the degree of ~2 dB loss for each additional bit of resolution. [8] Aside from increased insertion loss, digital phase shifters require a higher amount of chip area and offer less phase angle precision as compared to their analog counterparts. [9]

2.4 Types of Phase Shifters

When designing phase shifters, there are many different types of designs that can be considered. These designs vary widely in terms of complexity, practicality and fabrication/packaging requirements. Additionally, each design aspect presents a tradeoff between device features and performance. In order to quantify the performance of phase shifter design, a figure of merit (FOM) is commonly used which describes the degrees of phase shift that can be achieved at a specified frequency per decibel of loss in the device. Some common types of phase shifters and device types are detailed as follows:

2.4.1 Switched-Line

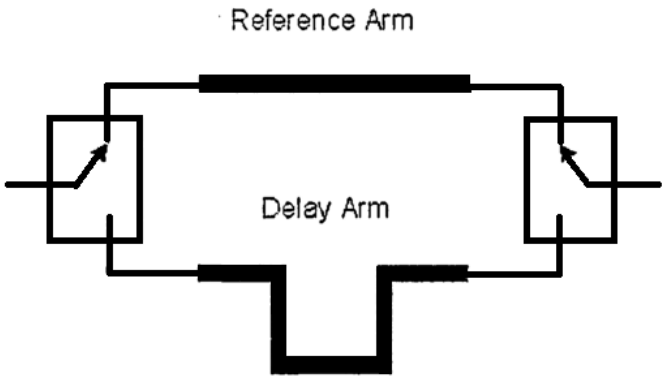


Figure 1: Switched-Line Phase Shifter

The switched-line phase shifter is an electromechanical device that enables a single, fixed amount of phase shift. Consisting of two delay lines of fixed electrical length, the switched-line phase shifter transitions between states through the use of switches. Recalling that phase shift is defined as the difference between two phase angles, the phase shift achieved is the difference between the electrical length of the reference arm and delay arm of the device as depicted in Figure 1. This type of phase shifter works well for obtaining large phase shift angles such as 90° or 180°. [10] Despite large phase shift capability, this type of phase shifter has low resolution (ie. Only two obtainable phase shifts ±ø) and relies on single-pole double-throw (SPDT) switches as the switching mechanism. [10] The resulting phase shift is the difference of the two electrical lengths as follows:

$$\boldsymbol{\Delta\phi = \phi_{delay} - \phi_{reference}} \tag{3}$$

2.4.2 Loaded-Line

Loaded-line phase shifters are tunable devices that achieve phase shift though tuning the lumped-element equivalent of a transmission line. Tuning in these devices can be attained though variable capacitors or active inductors. The usage of active inductors is often avoided due to high power consumption. The tuning behavior in loaded-line phase

shifters is therefore often enabled by varactors or switching capacitors. Usage of loaded-line phase shifters is limited to applications requiring 45° or less phase shift steps. [10]

2.4.3 Varactor Tuned Transmission Lines

A varactor tuned transmission line based phase shifter is a purely electrical device in which phase shift is created through the tuning of the lumped element equivalent structure. The tuning element in this phase shifter is commonly a varactor, but tuning through active inductors can also be achieved despite having high power consumption and increased circuit complexity. [9] These phase shifter structures are designed using a distributed highpass or lowpass structure in a T-configuration or Π-configuration.

2.5 Phase Shifting Technologies

Considering the wide range of applications that require phase control, there are many methods for the design and fabrication of phase control devices. In order for a phase shifter to have an adjustable phase angle, a phase shifting mechanism must be implemented. The most commonly used switching mechanisms electrically controlled, but mechanical and magnetic control is also possible. Magnetic phase shifting mechanisms can utilize ferromagnetic materials such as NiFe/SiO nanocomposite thin films in order to shift the resonance frequency as demonstrated in [11]. In the presence of an applied magnetic field, the change in material permeability will result in a shift in the resonance frequency. Mechanical elements are commonly used in phase shifters for the development of MEMS devices. Purely mechanical phase shifting mechanisms are much less common and are designed to change the physical length of the transmission line in order to alter the phase angle. For this thesis project, the research scope will be limited to electrical switching mechanisms. Potential electrical switching mechanisms include micro-electro-mechanical

systems (MEMS) switches, semiconductor diodes, and BST thin-film varactors which are all described in depth in the following sections.

2.5.1 MEMS Switches

MEMS switches are used in phase shifter design as an alternative to semiconductor diodes and FETs. As demonstrated in [12], a common MEMS switch is the cantilever beam structure where a conducting metal contact is suspended over a lower metal contact. The metal bridge is pulled down to make contact with the lower metal contact through the application of an actuation voltage. [13] MEMS, or more specifically RF MEMS capacitors, are commonly used in phase shifter design due to their low power consumption and 5:1 capacitance tuning ratio. [3] Unfortunately, these MEMS devices require a high tuning voltage and have a slow switching speed. Additionally, MEMS devices have been found to have reliability issues which results in a limited switching lifetime. [2]

2.5.2 Semiconductor Diodes

Semiconductor technologies such as PIN diode switches and field effect transistors (FETs) are heavily utilized in sold-state microwave circuit design. Based on GaAs, SiGe, or InP, semiconductor diodes exhibit fast switching times and low power consumption. When implemented as a tunable component, a low bias voltage of less than 10V is required for a 3:1 capacitance tuning ratio. [2] Unfortunately, semiconductor devices are not well fitted for high power applications as they have very poor power handling capabilities and exhibit low linearity.

2.5.3 Ferroelectric Varactors

Thin film ferroelectric varactors have been demonstrated throughout literature for phase shifter development. [14] Making use of nonlinear dielectrics such as Barium

Strontium Titanate, ferroelectric varactors have the capability to exhibit a decrease in capacitance when a voltage bias is applied. Unlike other types of phase shifter technologies, thin film ferroelectric varactors can be tuned with a very low DC biasing voltage. [3] Aside from the low tuning voltage, ferroelectric varactors have been successfully demonstrated to exhibit fast switching times and high power handling capabilities. This combination of low insertion loss and fast switching times makes a strong case for the use of BST based ferroelectric varactors in phase shifter design.

2.5.4 Comparison of Phase Shifters in Literature

A brief overview of phase shifters in literature is given in Table 2.

Table 2: Comparison of Phase Shifters in Literature

Reference	FOM (°/dB)	Phase Shift (°)	Frequency (GHz)	Insertion Loss (dB)	Substrate	Type
[4]	107.3	142	16	50	TiO2/Si	Ferroelectric Varactor
[5]	44	260	8	50	Al2O3	Ferroelectric Varactor
[15]	-	360	20	-	GaAs	MEMS
[16]	42	92	76	2.4	Si	MEMS
[17]	46.2	360	11-13	7.8	-	Semiconductor

2.6 Barium Strontium Titanate

Barium Strontium Titanate $Ba_xSr_{(1-x)}TiO_3$ (BST) is a ferroelectric compound of Barium Titanate $BaTiO_3$ and Strontium Titanate $SrTiO_3$. The composition of BST is based upon the desired critical temperature, with $Ba_{0.6}Sr_{0.4}TiO_3$ possesing a critical temperature near that of room temperature. [2] As a dielectric material, BST exhibits nonlinear dielectric behavior under the influence of an applied voltage bias which has been widely explored for applications in highly tunable microwave circuits. While many standard

dielectric materials have a dielectric constant in the range of $\varepsilon_r = 1 - 100$, thin film BST has an unusually high dielectric constant of $\varepsilon_r = 500 - 700$. As demonstrated in [18], an increase in capacitance of up to 20 percent is seen when a voltage between 0-12 V is applied to the BST thin film varactors. The tuneability of BST can be expressed using the following equation from [3].

$$\tau = \frac{\epsilon_{rE} - \epsilon_{r0}}{\epsilon_{r0}} \tag{4}$$

PHASE SHIFTER DESIGN

Phase shifters based on ferroelectric varactor tuned transmission lines operate through the tuning of the varactor capacitance. In order to design a varactor that provides sufficient tuning potential, both the conductor geometry and insulating dielectric material must be carefully selected and designed. Both varactor structures defined within the scope of this thesis (parallel plate and single layer) are examined in this section. Lumped element electrical models and mathematical models are developed and adapted from literature to adequately model the insertion loss and phase angle of the device.

3.1 Single Layer Varactor Design

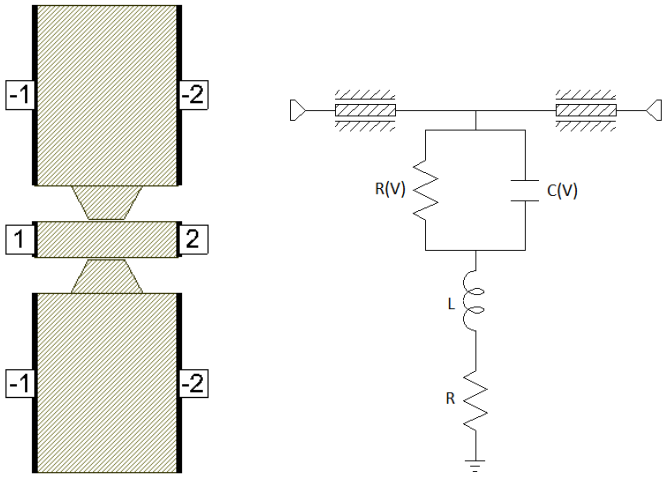


Figure 2: Single Layer Varactor and Equivalent Lumped Element Model

In the single-layer varactor design, the conducting metal layer is deposited on top of a BST thin film layer. The capacitance in this design is derived from the gap between the signal line and the top and bottom ground planes. Due to the thickness of the conductor, this gap forms a metal-insulator-metal (MIM) parallel-plate capacitor which has a capacitance of the following form,

$$C = \frac{\varepsilon_r \varepsilon_o A}{d} \tag{5}$$

Where A is the area of the capacitor plates, ε_r is the relative permittivity of the dielectric and d is the distance between the plates. Since BST is not directly deposited between the two conductors, a fill factor is associated with calculating the effective dielectric constant. For modeling purposes, it is assumed that the effective dielectric constant is essentially that of BST.

The single layer varactor conductor geometry is shown in Figure 2 along with an equivalent electrical model. A simple analysis of the conductor geometry shows that the structure is based on a coplanar waveguide (CPW) signal line with an input impedance of approximately 50 Ω. A constant width of 50 μm is maintained between the 50 μm wide CPW line and each ground plane in order to attain this input/output impedance. This structure passes nearly all of the signal through in the absence of a capacitance and increases in signal loss and phase angle as the capacitance increases. In modeling the capacitor, a standard high frequency capacitor model is used as is shown in the right half of Figure 2.

3.2 Parallel Plate Varactor Design

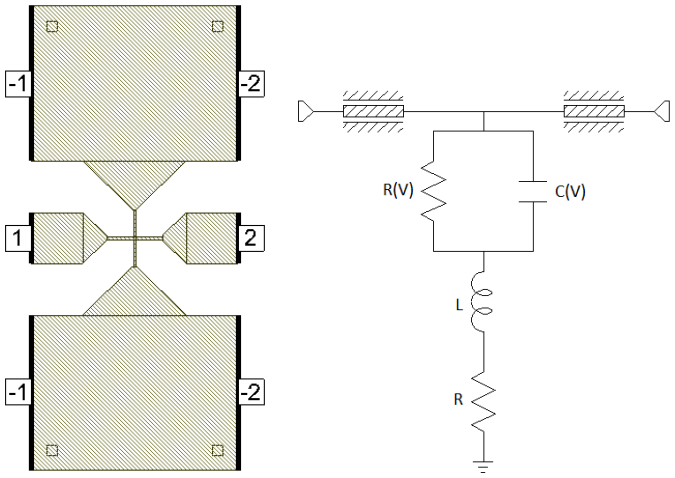


Figure 3: Parallel Plate Varactor and Equivalent Lumped Element Model

Much like the single layer varactor design, the parallel plate varactor derives its capacitance from a MIM parallel plate capacitive structure. The insulating dielectric layer is now placed in-between the top and bottom conducting metal layers. The capacitance is derived from overlapping area between the signal line of the top metal layer and the ground plane of the bottom metal layer. The general parallel plate capacitor equation from Equation 4 is again used for the calculation of the capacitance. The electrical model for the parallel plate capacitor is the same as the one used for the single layer varactor.

3.3 Varactor Tuning

When designing phase shifters, the primary function of ferroelectric varactors is to alter the electrical length of the transmission line. Through the application of a DC biasing voltage to thin film BST layer, the capacitance, and in turn electrical length of the phase shifter, is decreased. The difference between the electrical length with and without a DC biasing voltage is the effective phase shift created by the device. As more unit varactor segments are cascaded, the effective capacitance of the phase shifter increases along with the potential for higher phase shift.

3.4 Mathematical Model

A mathematical model can be derived to closely approximate the S-parameters of the varactor based phase shifter devices. The two main elements of the phase shifter are the CPW transmission line and the shunt varactor as described by the electrical model. While there are many approaches to developing a mathematical model, ABCD parameters best facilitate the interaction between these elements. ABCD parameters can be cascaded simply through matrix multiplication and converted to S-parameters with little difficulty. The ABCD parameter matrices for a shunt impedance, series resistance and transmission line can be found in [19] as follows.

$$Shunt\ Impedance: \begin{bmatrix} 1 & 0 \\ \frac{1}{Z} & 1 \end{bmatrix} \tag{6}$$

$$Series\ Resistance: \begin{bmatrix} 1 & R \\ 0 & 1 \end{bmatrix} \tag{7}$$

$$Transmission\ Line: \begin{bmatrix} \cosh(\gamma l) & Z_o \sinh(\gamma l) \\ \frac{1}{Z_o}\sinh(\gamma l) & \cosh(\gamma l) \end{bmatrix} \tag{8}$$

The first element in this model of the phase shifter is the capacitance contributed by the shunt varactor. At higher frequencies, a simple capacitor model is unable to accurately model the device. Considering that the device is lossy, the shunt capacitor is modeled to include a capacitance, parasitic inductance and series and shunt resistances to account for material based losses. Modeling the shunt capacitance along with these high frequency parasitics is accomplished by determining the equivalent shunt impedance as follows.

$$Z = \left(\frac{1}{R_p} + \frac{1}{\frac{1}{j\omega C}}\right)^{-1} + j\omega L + R_s \tag{9}$$

The capacitance and shunt resistance are in parallel with each other and mutually in series with the inductance and series resistance as is obtained from the high frequency capacitor electrical model. This equivalent impedance is simplified to obtain the following expression.

$$Z = \frac{R_p + R_s - \omega^2 R_p LC + j\omega\left(R_p R_s C + L\right)}{1 + j\omega R_p C} \tag{10}$$

The resulting expression is in terms of the RLC network components and the source frequency ω. Each of the RLC network components can be farther expressed in terms of material properties and physical dimensions of the device as covered in [20]. The varactor capacitance is approximated using the parallel plate capacitor equation.

$$C = \frac{\varepsilon_o \varepsilon_r w l}{d} \tag{11}$$

In this expression, w is the conductor thickness, l is the length of the overlap between the conductors and d is the distance between the conductors. A relative permittivity of $\varepsilon_r = 500$ is used for modeling thin film BST in this section.

The series resistance R_s which models the conductor losses can be calculated as,

$$R_s = \frac{l}{\sigma w t} \tag{12}$$

where l is the conductor length, w is the width of the conductor, t is the thickness of the conductor and σ is the conductivity of the conducting material.

The shunt resistance R_p which models the dielectric losses can be calculated as,

$$R_p = \frac{1}{\omega C \tan\delta} \tag{13}$$

where ω is the source frequency, C is the shunt capacitance and $\tan\delta$ is the loss tangent of the dielectric.

Finally, the series inductance can be calculated as,

$$L_s = \frac{Z_o}{\omega}\sin(\beta l) \tag{14}$$

where Z_o is the characteristic impedance, ω is the source frequency, β is the phase constant and l is the length of the transmission line.

The analysis of coplanar waveguides is covered in [21-22]. In this analysis, conformal mapping methods are used to obtain the effective permittivity of the waveguide. Unlike the conventional model of a coplanar waveguide, the phase shifter makes use of layered dielectrics.

$$k_o = k_3 = k_4 = \frac{s}{s+g} \tag{15}$$

$$k_1 = \frac{sinh(\pi s/2h_1)}{sinh(\pi(s+g)/2h_1)} \tag{16}$$

$$k_2 = \frac{sinh(\pi s/2h_2)}{sinh(\pi(s+g)/2h_2)} \tag{17}$$

$$k'_n = \sqrt{1 - {k_n}^2} \tag{18}$$

In order to calculate the effective permittivity, elliptical integrals must be used.

$$\varepsilon_{eff} = 1 + \frac{(\varepsilon_{r1}-1)}{2}\frac{K(k_1)}{K(k'_1)}\frac{K(k'_o)}{K(k_0)} + \frac{(\varepsilon_{r2}-\varepsilon_{r1})}{2}\frac{K(k_2)}{K(k'_2)}\frac{K(k'_o)}{K(k_0)} \tag{19}$$

$$q_1 = \frac{K(k_1)}{K(k'_1)}\frac{K(k'_o)}{K(k_0)} \tag{20}$$

$$q_2 = \frac{K(k_2)}{K(k'_2)}\frac{K(k'_o)}{K(k_0)} \tag{21}$$

The transmission line is considered to be lossless for modeling purposes. The loss due to the shunt capacitance far exceeds the loss of the transmission line. For this reason, the propagation constant, γ, is considered to have only an imaginary component called the phase constant.

$$\gamma = j\beta \tag{22}$$

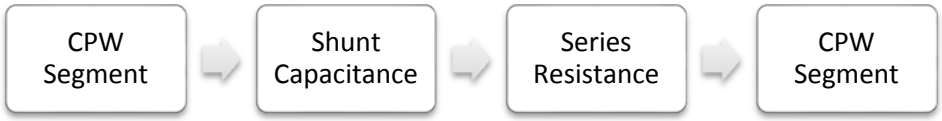


Figure 4: Cascaded Structure

The ABCD parameters for the complete device can be obtained through matrix multiplication of the ABCD parameters of each of the circuit elements. In this case, a single device is the combination of a CPW line segment cascaded with a shunt impedance cascaded with another CPW line segment.

Since it is possible to translate between sets of parameters, the S-parameters for S11 and S21 can be obtained using the expressions from [20] as shown below.

$$Z_{01} = Z_{02} = Z_o \, , R_{01} = R_{02} = \mathbb{R}(Z_o) \tag{23}$$

$$S_{11} = \frac{AZ_{02}+B-CZ_{01}^{*}Z_{02}-DZ_{01}^{*}}{AZ_{02}+B+CZ_{01}Z_{02}+DZ_{01}} \tag{24}$$

$$S_{21} = \frac{2\sqrt{R_{01}R_{02}}}{AZ_{02}+B+CZ_{01}Z_{02}+DZ_{01}} \tag{25}$$

3.5 Varactor Electrical Model

In order to understand the electrical properties of the presented phase shifters, it is necessary to first understand the electrical properties of the individual ferroelectric varactors. This can be accomplished through finding an equivalent electrical model for the varactors. From the literature review, it is found that the phase control circuit described thus far can be modeled as a transmission line in order to simplify the design. [18] A basic transmission line model consists of a resistance, capacitance, inductance and conductance. With this in mind, control over the phase angle can be achieved by tuning the lumped element equivalent of the transmission line.

Using this information, the electrical model for a varactor segment will consist of a shunt resistive-inductive-capacitive (RLC) network. In this RLC network, a resistor and inductor are placed in series with a variable resistor and variable capacitor which are in parallel to each other. The resulting electrical model is shown in Figure 5.

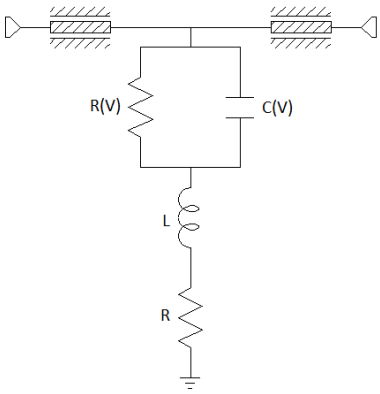


Figure 5: General Varactor Electrical Model

For modeling purposes, a CPW line element has three parameters: gap width, conductor width and conductor length. Each of these parameters are dependent on the physical layout of the EM structure. In order to have an input and output impedance of 50 Ω, the gap and conductor widths are fixed to 50 µm. The conductor length is defined as the length of the CPW line for which these gap and conductor widths are equal to 50 µm in the EM structure. This results in a length of 50 µm for each of the CPW line segments based upon the EM structure. For the remaining lumped elements, a variable capacitance and resistance are modeled. The second resistor models the source resistance and the inductor models the parasitic inductance.

The value of each of the lumped elements in the electrical model is undefined until simulations are run on the EM structure. Using the simulated measurements from the EM

structure, each lumped element in the electrical model can be “tuned” until the measurements of each device representation are the same.

SIMULATIONS

4.1 Scattering Parameters

Scattering parameters (S-parameters) are electrical measurements used to describe the behavior of a linear system in response to a steady state input. In a passive two port device, there are four S-parameters measurements of interest which are listed as follows:

S11 is the input port voltage reflection coefficient

S12 is the reverse transmission coefficient

S21 is the forward transmission coefficient

S22 is the output port voltage reflection coefficient

Since all of these measurements are in complex form, all S-parameters can be expressed in terms of magnitude and phase angle. The magnitude corresponds to the voltage at the port of interest relative to a reference port. Similarly, the phase angle corresponds to the phase angle at the port of interest relative to the reference port. In the S_{21} measurement, the magnitude represents the insertion loss (output voltage relative to input voltage) and the phase angle represents the phase angle (output phase angle relative to input phase angle). When evaluating simulation results, only the input port reflection coefficient, S_{11}, and the forward voltage gain, S_{21}, will be considered with an emphasis on the S_{21} measurements.

4.2 Materials

The fabrication of single layer and parallel plate varactor based phase shifters use a Sapphire/BST/Au or Sapphire/Au/BST/Au material stack up, respectively. The fabricated layers of the single layer phase shifter are shown in Figure 6. In both cases, the base layer of Sapphire serves as an insulating substrate. The BST thin film layer deposited either directly on the Sapphire or on a bottom metal layer serves as the main dielectric layer

for the formation of a capacitive structure. The material properties for all of the layers are summarized in Table 3.

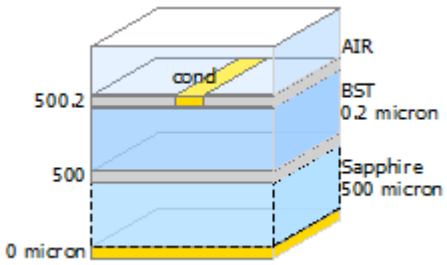


Figure 6: Material Stackup

Table 3: Material Definitions

Material	Thickness (um)	Dielectric Constant	Loss Tangent	Conductivity
Sapphire	500	9.7	0.005	N/A
$Ba_{0.6}Sr_{0.4}TiO_3$	0.20	500	0.02	N/A
Au	1	N/A	N/A	2e7

4.3 Electrical Model Tuning

When researching CPW based phase shifters, it was determined that the transmission line model can be used as the equivalent electrical model. This model consists of four parameters; resistance, capacitance, inductance and conductance as shown in Figure 5. In order to extract the transmission line parameters from the varactor devices, the S-parameters of the varactors must be obtained using an electromagnetic simulator such as AXIEM. Once the S-parameters are obtained through simulation, the individual component values in the electrical model can be varied (tuned) in order to match the S-parameters of

the varactor and the equivalent electrical model. The S_{11} and S_{21} matching results are shown in Figures 7-8.

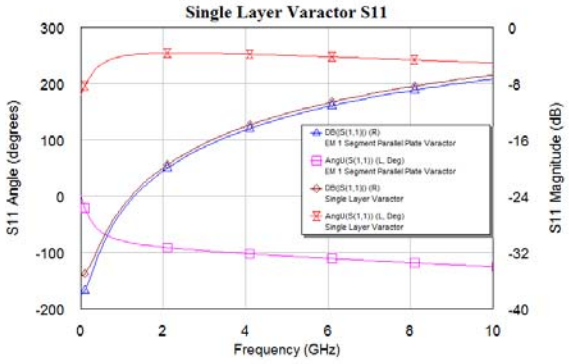


Figure 7: Varactor S_{11} Tuning

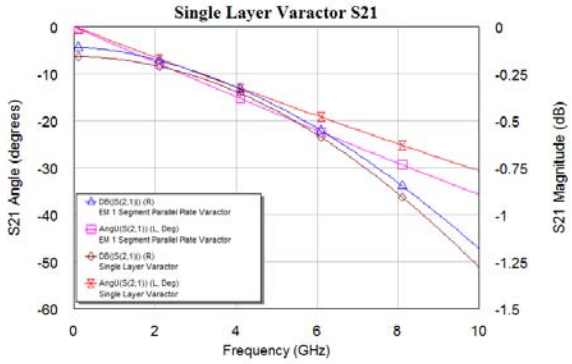


Figure 8: Varactor S_{21} Tuning

In examining the matching results, the equivalent electrical model is found to be a good fit over the 0 – 10 GHz range. Since the purpose of a phase shifter is to control the phase angle at the output of the device, the magnitude and angle of S_{21} are the most important measurements to match. Looking at the tuning results for S_{21} within the frequency range of interest, the magnitude has a maximum error of 0.06 dB and the phase angle has a maximum error of 5 degrees. The results of interest for the simulated phase shifter and equivalent electrical model are summarized in Table 4.

Table 4: EM Simulation vs Electrical Model S-Parameters

	Mag|S_{21}| (dB)		Ang|S_{21}| (Degrees)		Mag|S_{11}| (dB)		Ang|S_{11}| (Degrees)	
	5 GHz	10 GHz	5 GHz	10 GHz	5 GHz	10 GHz	5 GHz	10 GHz
Simulated	-0.4214	-1.790	-18.5	-35.78	-12.75	-7.390	-106.7	-105.4
Electrical Model	-0.4480	-1.282	-15.88	-30.67	-12.28	-6.821	249.6	236.0

The equivalent electrical model for the unit single layer varactor has an equivalent capacitance of 0.33 pF. When the varactor segments are cascaded multiple times, the capacitances and phase angles will add resulting in a phase shifter with good phase shift potential. A summary of the equivalent values for each of the transmission line parameters is given in Table 5 and the equivalent electrical model with equivalent component values is shown in Figure 9.

Table 5: Electrical Model Component Values

	C1	L1	R1	R2
Single Layer Electrical Model	0.33 pF	0.03 nH	1.4 kΩ	1 Ω

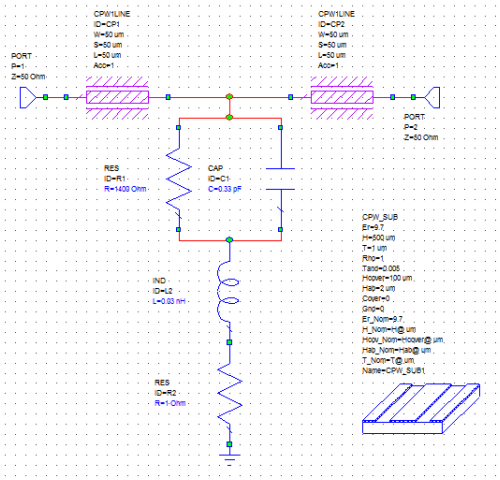


Figure 9: Tuned Electrical Model

4.4 Simulation Methods

Electromagnetic simulations are computationally demanding to perform. This results in complex EM structures, such as cascaded devices, taking large amounts of time and computational resources to simulate. AWR Microwave Office provides two methods that can be used to simulate cascaded electromagnetic structures. The first method is to cascade each unit varactor segment within the EM structure and simulate the cascaded

structure in its entirety. While highly accurate, this method is computationally intensive and can only be used for a limited number of segments. The second method involves cascading the varactor "subcircuit" in the circuit schematic view. By using this method, the S-parameters from the simulation of the varactors are extracted and converted to transfer parameters (T-parameters). The resulting T-parameters can then be multiplied using matrix multiplication and converted back to S-parameters to determine the effects of cascading multiple 2-port networks. This method results in very close simulation results for EM structures that could not be easily simulated otherwise. To illustrate this point, the EM structure and Schematic View simulation results from a 10 segment single layer varactor device are compared in Figures 10 and 11.

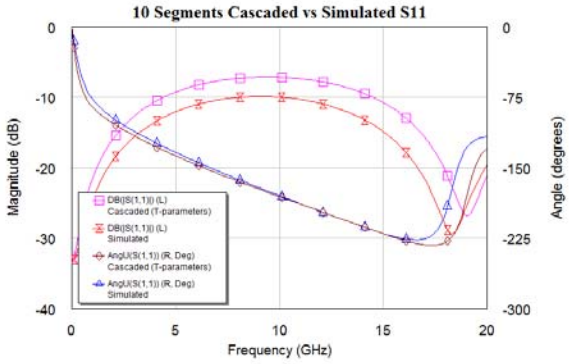


Figure 10: S_{11} Cascaded vs. Simulated

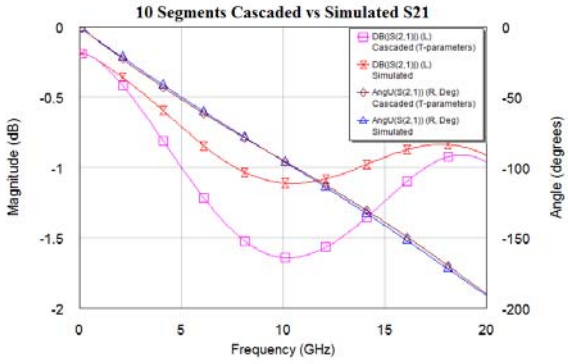


Figure 11: S_{21} Cascaded vs. Simulated

The graph shown in Figure 10 compares the S_{11} magnitude and phase angle of the EM simulation and the mathematically cascaded results. At frequencies towards the upper and lower ends of the simulated frequency spectrum, there is nearly no difference between the simulated S-parameters. Towards the center of the frequency spectrum, there is more significant difference in the S_{21} magnitude with a half decibel difference at 10 GHz. In the graph shown in Figure 11, the S_{21} angle is nearly identical throughout the entire frequency spectrum and only has slight variances at higher frequencies. Considering that phase

control is the desired application, this slight variance between the EM simulation and mathematical cascading is not a problem for predicative purposes.

4.5 Device Modifications

One of the primary challenges in designing phase control devices is stabilizing performance across the entire bandwidth. Initial simulations of the presented single layer varactor based phase shifter show that the insertion loss in the circuit is nonlinearly dependent on frequency. This is undesirable as device performance will vary as the input frequency is varied. Fortunately, there are multiple ways to stabilize the performance including modifying the conductor geometry or material composition of the device. For the remainder of this chapter, all simulation results will be of phase shifter consisting of 25 cascaded single layer varactor segments with the relative permittivity of BST fixed at $\varepsilon_r = 500$ unless otherwise specified.

4.6 Single Layer Varactor Conductor Geometry

In the initial analysis of the conductor geometry, it was determined that the phase shifter is based on a coplanar waveguide structure. The extension of the ground plane toward the signal line forms a parallel plate capacitor governed by the gap width, length and conductor thickness. While the gap width and conductor thickness are fixed for fabrication purposes, the gap length, L1, can be modified to increase or decrease the capacitance per varactor segment. Additionally, the modification of width L2 can be used to stabilize the performance of the device across the device bandwidth. The parameters L1 and L2 are shown on a single varactor segment as is seen in Figure 12.

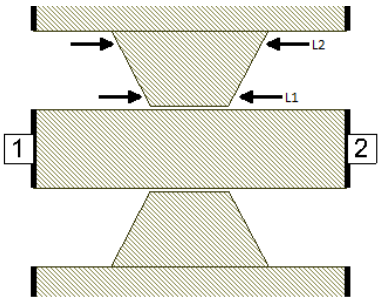
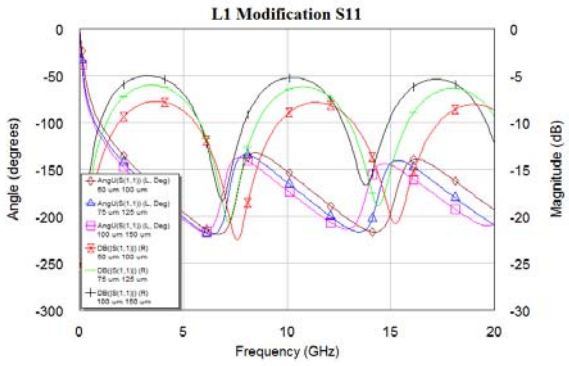


Figure 12: EM Structure Modification Parameters

The first device modification to be considered is increasing the width labeled L1 in the figure above. Considering the parallel pate capacitor equation, the width of the conducting plate is linearly proportional to the device capacitance. The initial values for L1 and L2 are 50 µm and 100 µm, respectively. In order isolate the effect of increasing L1, the width of L2 is also increased by the same amount as L1 in order to maintain a consistent angle with respect to the polygon sides. The S-parameters for the modified values of L1 are shown in Figures 13 and 14.



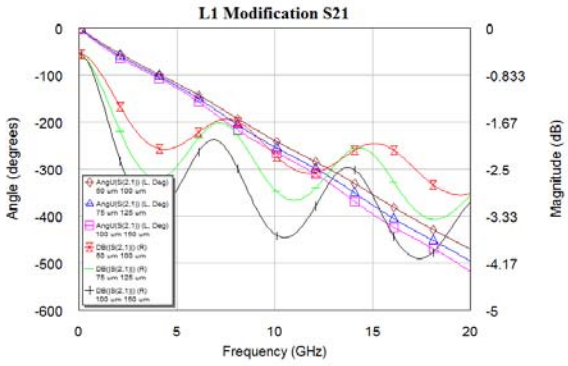


Figure 13: Phase Shifter L1 Modification S_{11}

Figure 14: Phase Shifter L1 Modification S_{21}

In examining the effect of increasing L1 on the phase shifter S-parameters, it can be observed for both S_{11} and S_{21} that the frequency response characteristics shift to lower

frequencies as L1 is increased. The insertion loss, Mag|S(2,1)|, increases as L1 is increased and becomes increasingly unstable with small changes in input frequency. With this in mind, the capacitance in the phase shifter is increased as L1 increases resulting in the phase angle at an input frequency of 15 GHz increasing from 378 degrees to 424 degrees.

The next conductor geometry modification to be considered is increasing the width of L2. Unlike the previous case, the width of L1 will remain fixed in order to observe the effect of increasing or decreasing the angle that L1 has with respect to the polygon sides. The resulting S-parameters are shown in Figures 15 and 16.

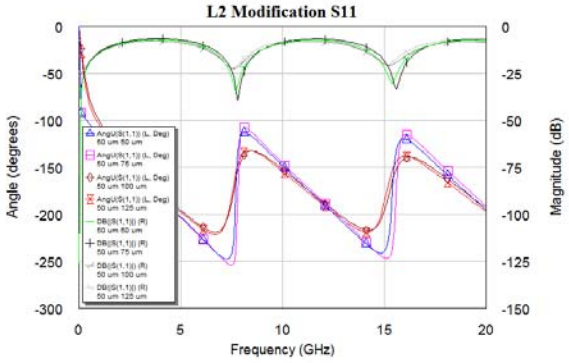


Figure 15: Phase Shifter L2 Modification S_{11}

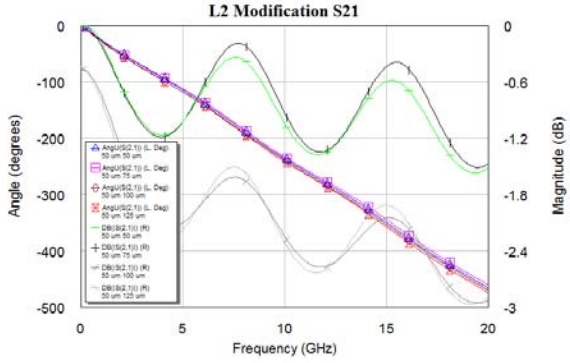


Figure 16: Phase Shifter L2 Modification S_{21}

Through simulations, it is found that modifying L2 has a significant effect on the S-parameters of the phase shifter. Looking at the magnitude and phase of S_{11}, the frequency response becomes much more rigid as L2 decreases. In terms of the magnitude and phase of S_{21}, this translates into a slight decrease in phase angle, yet a large decrease in insertion loss as L2 decreases. Overall, the phase shifter becomes more stable over the entire bandwidth as L2 increases at the expense of an increased insertion loss.

4.7 BST Fill Layer

Taking in to consideration the electrical fields in the single layer varactor, there will be a higher density of electric field lines in the BST layer than in the air filled gap between the signal line and ground plane(s). Since a higher device capacitance is desired in order to increase the maximum phase angle, the device can be modified to use BST as the dielectric between the conductors. A modified conductor geometry with BST in between the signal line and ground plane is shown in Figure 17.

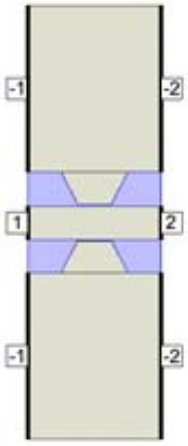


Figure 17: Single Layer Unit Varactor with BST Fill

If this device is to be fabricated, a thin film BST layer will first be deposited on the Sapphire substrate. The BST layer is then selectively etched in order to create "wells" for the deposition of the conducting layer. A gold conducting layer will then be deposited in the etched "wells" resulting in BST filling the gap between the signal line and the ground plane. A consequence of the etching process is that all of the BST will be removed from the well. This results in gold conductor being directly deposited on the sapphire layer.

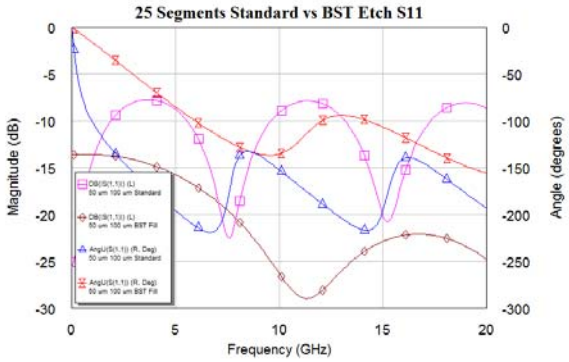


Figure 18: $|S_{11}|$ Standard vs. BST Fill

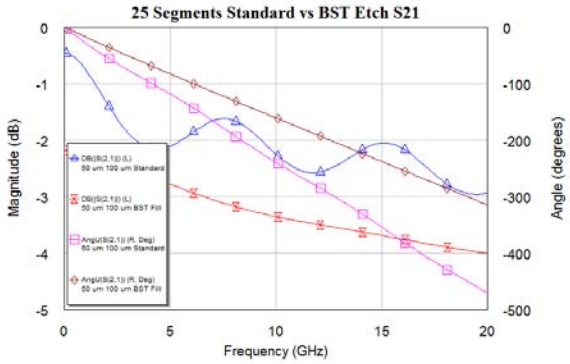


Figure 19: $|S_{21}|$ Standard vs. BST Fill

Looking at Figure 18, there is a significant decrease in the maximum phase angle between the original EM structure and the modified BST filled gap structure. While this decrease in phase angle is not necessarily desirable, the new structure has a nearly linear insertion loss over the desired bandwidth as shown in Figure 19. Between the frequencies of 3 GHz and 17 GHz, the S_{21} magnitude remains nearly unchanged with only a slight linear increase as frequency increases. By comparison, the insertion loss in the original EM structure changes significantly with frequency and will provide varying performance depending on the frequency of operation.

4.8 DC Voltage Bias

A main component of phase shifter functionality is the ability to shift between phase angles. From the literature review, it was discovered that the capacitance in BST varactors can be decreased by applying a DC biasing voltage to the device. When a voltage bias is applied, the dielectric permittivity of BST is reduced. The single layer varactor based phase shifter structure (L1 = 50 µm, L2 = 100 µm) is simulated with different permittivities and the resulting S-parameters are shown in Figures 20-23.

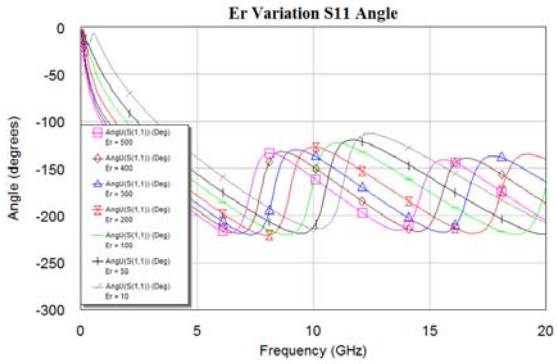


Figure 20: Voltage Bias S_{11} Angle

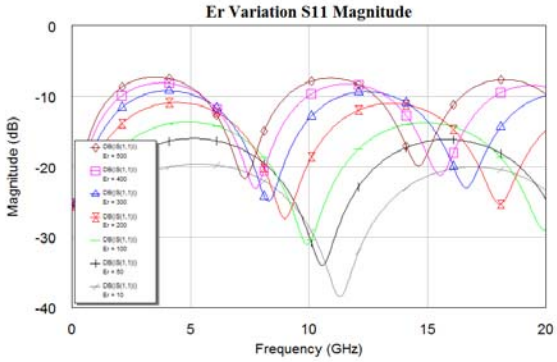


Figure 21: Voltage Bias S_{11} Magnitude

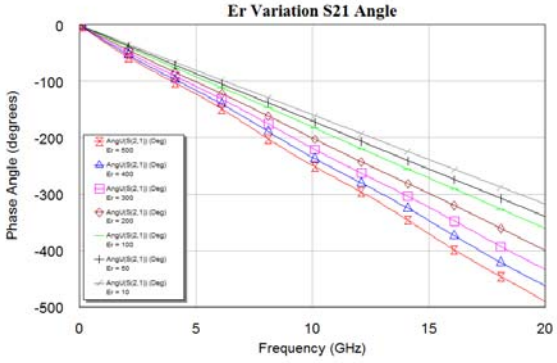


Figure 22: Voltage Bias S_{21} Angle

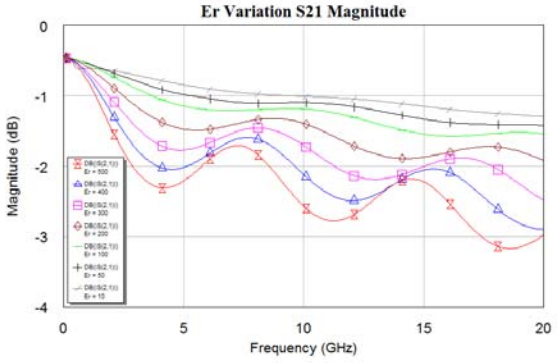


Figure 23: Voltage Bias S_{21} Magnitude

In simulating the effect of an applied DC bias, it can be observed that the phase angle does decrease as expected. For simulation purposes, the permittivity of BST is considered to be $\varepsilon_r = 500$ at 0V DC. In the absence of a DC bias, the phase shift angle at 15 GHz is 370.2 degrees. When the DC bias is increased so that the effective permittivity is $\varepsilon_r = 200$, the phase shift angle at 15 GHz decreases to 298.6 degrees. From this observation, it can be concluded that through the application of a DC voltage bias, there is a high degree of phase tuning ability in the device. In addition to the change in phase shift angle, the

insertion loss in the phase shifter decreases and becomes consistent across the entire bandwidth as the permittivity of BST decreases.

EXPERIMENTAL PROCEDURE

Experimental testing of microwave circuits is essential for the verification of computer simulations and electrical models. In order to do this, a photolithography mask set is created by Photo Sciences Inc. which contains all of devices as designed in the Applied Wave Research (AWR) Microwave Office software. Single layer and parallel plate phase shifters consisting of 10, 15, 20 and 25 cascaded varactor segments are fabricated using the mask set and standard microelectronic processing techniques. The BST thin films are deposited in a class 100 clean room at the University of Dayton using a pulsed laser deposition (PLD) system. Following the fabrication process, the phase shifter devices are ready for on wafer testing.

5.1 Measurement Setup

The S-parameter measurements for each phase shifter are obtained using an HP 8720B 130 MHz – 20 GHz vector network analyzer (VNA). A MATLAB script is run on a connected laptop computer to perform a frequency sweep and collect data at a specified number of points. The wafer containing the phase shifter devices is secured on a JMicro Technology Corporation LMS-2709 microwave laboratory microprobing station and Ports 1 and 2 of the VNA are connected to ACP probes. A high voltage bias tee is placed in line with Port 1 and connected to a source meter for the application of DC biasing voltage. A complete list of equipment including manufactures and model numbers is given in Table 6.

5.2 Calibration

At high frequencies, electrical test equipment needs to be carefully calibrated to ensure measurement accuracy. A Cascade Microtech impedance standard substrate (ISS)

(P/N 101-190) is used to calibrate the network analyzer. The ISS consists of 5 identical sets of short, thru and load structures. These structures have a ground-signal-ground configuration and support probe pitches of 100-250 μm. In order to calibrate for two-port measurements, the ports are first individually calibrated under open, short and load conditions. The first of these calibration measurements is the open-circuit measurements in which the resistance between the probe leads is effectively infinite. This can be accomplished by raising the ACP probes off of the wafer until the probes no longer make contact with the wafer. According to the ISS datasheet, the manufacturer recommends raising the probe 250 μm or greater off of the wafer. Next, the short-circuit measurement can be taken by aligning each of the probes with the short circuit transmission line on the ISS. The short circuit structure is a single trace that creates path of negligible resistance between the signal and ground leads of the probe. The final single port calibration is the load measurement. Each of the probes are aligned with the load transmission line on the ISS in order to calibrate the network analyzer to an ideal 50 ohm load. After all of these steps are performed for both port 1 and port 2, the calibration result is computed by the network analyzer and displayed. Provided that the resulting calibration is consistent across the entire frequency spectrum of interest, the calibration can be saved and the device is ready for taking measurements.

5.3 Measurement Procedure

The wafer containing the fabricated phase shifter devices is placed on the chuck of the probing station, aligned and secured through the use of a vacuum pump. Using the x, y, and z axis alignment knobs, the wafer position is adjusted until the 10-segment phase single layer phase shifter device is located directly under the microscope. Using the x, y,

and z axis alignment knobs on the microwave probe holders, each of the ACP probes are aligned with the probing pads of the phase shifter device and lowered until contact is made with the device. Through the use of the computer connectivity of the network analyzer, a MATLAB script is run to measure all of the two-port S-parameters over the full frequency range of the network analyzer. After the initial measurements of the device without a DC bias are taken, the DC bias is increased in 1V steps and measurements are repeated until a DC bias of 8V is reached. These measurement steps are used for testing the single layer and parallel plate 10, 15, 20, and 25 segment phase shifter devices.

Table 6: Equipment List

Name	Manufacturer	Model #
130 MHz – 20 GHz Network Analyzer	Hewlett-Packard	8720B
High Voltage Bias Tee	Picosecond Pulse Labs (Tektronics)	5531
Source Meter	Keithley	2400
Microwave Probe Holder	JMicro Technology	KRN-09S
ACP Probe	Cascade Microtech	ACP40-GSG-150
Microwave Laboratory Microprobing Station	JMicro Technology	LMS-2709
Impedance Standard Substrate	Cascade Microtech	P/N 101-190, S/N 230437

RESULTS AND DISCUSSION

This chapter examines the frequency domain S-parameter measurements for each of the phase shifter designs. The experimental measurements are compared to the simulated S-parameter measurements in order to understand the simulation accuracy. Measurements are taken for both the single layer and parallel plate phase shifter designs of lengths of 1, 10, 15, 20 and 25 segments. All testing is performed at room temperature and a DC bias sweep from 0V to 8V is applied to each device in order to observe the phase shifting behavior.

6.1 Single Layer Phase Shifter

When testing the single layer varactor based phase shifter, results were only able to be obtained in the absence of a DC bias. No changes were seen in the S_{11} or S_{21} measurements as the voltage bias was increased up to 8V. This is due to the larger gap of 2.5 μm (compared to the 0.18-0.25 μm gap in the parallel plate varactor design) between the conducting capacitor plates. In order to obtain the same electric field (40 kV/cm) that was applied to the parallel plate phase shifter design, it is necessary to apply 10 times the voltage to the device (0-80V). At this high voltage, testing would cause the wafer and all devices to be damaged. Results are presented below for the 0V DC bias measurements as well as simulations.

6.1.1 Phase Shifter – 1 Segment

The single layer unit varactor is simulated using a relative permittivity of thin film BST of $\varepsilon_r = 500$ and a conductivity of Au of $\sigma = 2x10^6$. The electrical model described in the simulations section of this thesis is used to extract the electrical parameters of the device. Figures 24-25 show the matching results for the S_{11} and S_{21} parameters,

respectively. The electrical model extraction for the device shows that the varactor capacitance is 0.33 pF. The full extraction results are shown on the electrical circuit schematic as depicted in Figure 26.

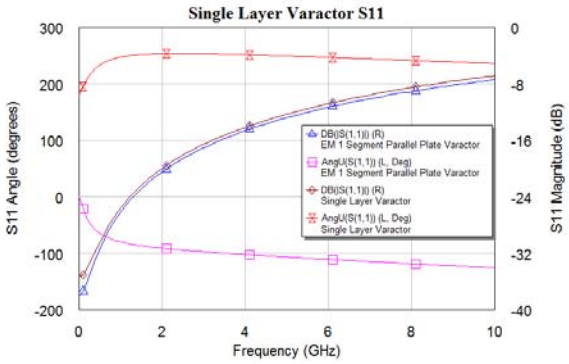


Figure 24: Single Layer S_{11} Tuning

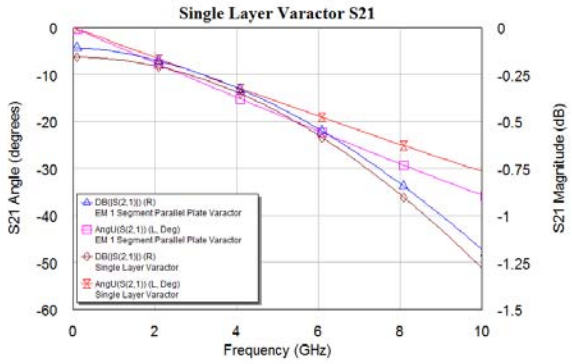


Figure 25: Single Layer S_{21} Tuning

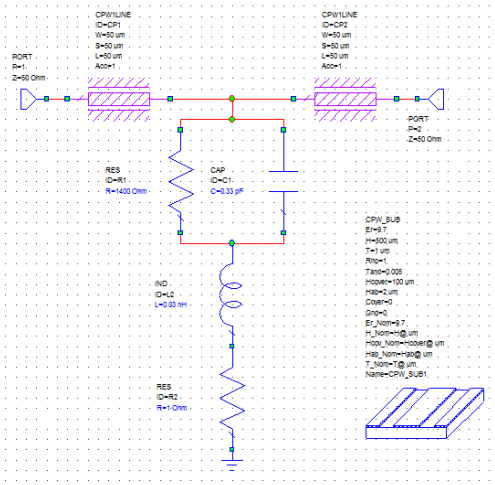


Figure 26: Single Layer Varactor - Tuned Electrical Model

6.1.2 Phase Shifter – 15 Segments

While there are no tuning results to show, it should be noted that the simulation results are close to those found through experimental measurements. As an example of the

simulation vs. experimental accuracy, the S_{21} magnitude and phase results are shown for the 15 segment phase shifter in Figures 27-28, respectively. Looking at these results, both the magnitude and phase angle of the 15 segment single layer phase shifter are approximated through the simulated device.

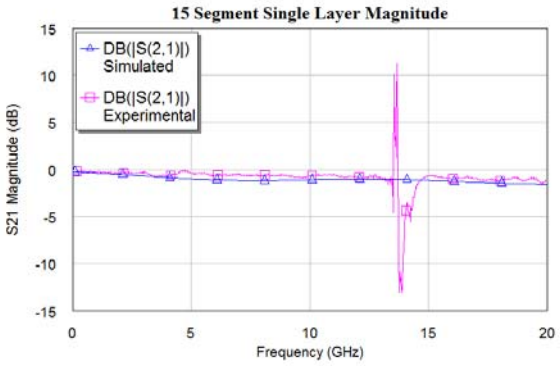


Figure 27: 15 Segment Single Layer Phase Shifter – S_{21} Magnitude

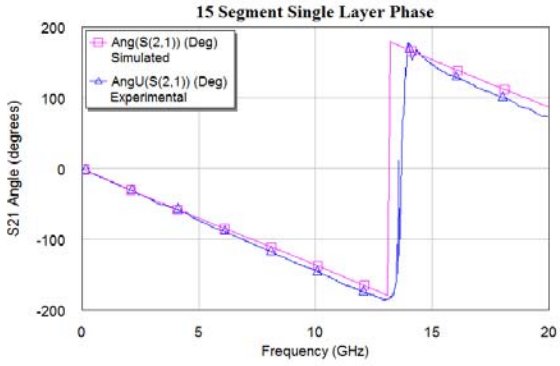


Figure 28: 15 Segment Single Layer Phase Shifter – S_{21} Phase Angle

6.1.3 Phase Shifter – Experimental Results

While it is not advantageous to plot the simulated vs. experimental results for each of the phase shifters at 0V DC bias, there are some useful trends that can be discovered through plotting all of the experimental results in one graph. Figures 29-30 show the S_{21} magnitude and phase, respectively. As the number of varactor segments in the phase shifter increase, the measured insertion loss only slightly increases. Meanwhile, the phase angle of each phase shifter increases proportionally to the number of varactor segments that are cascaded. The spike seen around 15 GHz is measurement noise and should be ignored in the analysis of results. Unlike many of the phase shifters examined in the literature review, these single layer phase shifters exhibit very low insertion loss (less than 3 dB across the entire bandwidth). Based on the high phase angle produced along with this small insertion

loss, the FOM can be expected to be very high if the application of a DC bias results in a similar reduction in capacitance as seen in the parallel plate phase shifters.

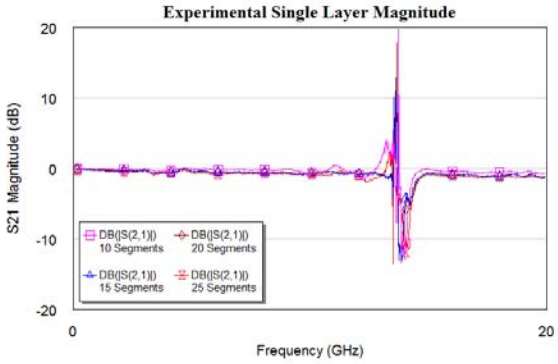


Figure 29: Experimental Phase Shifter - S_{21} Magnitude

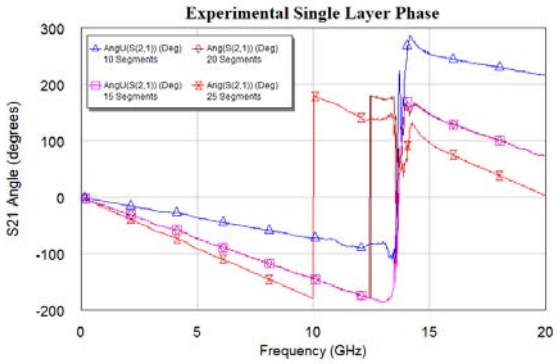


Figure 30: Experimental Phase Shifter - S_{21} Phase Angle

6.2 Parallel Plate Phase Shifter

The experimental testing of the parallel plate varactor based phase shifters produced results consistent with what our lab has seen in the past. Through the application of a 0-8V DV bias voltage to the 10, 15, 20, and 25 segment phase shifters, varying degrees of phase shift was achieved. The S-parameter measurements and simulation results are shown in the following sections as well as computed the computed FOM for each phase shifter at 15 GHz.

6.2.1 Phase Shifter - 10 Segments

The frequency sweep of the magnitude and phase angle of S_{21} is shown in Figures 31-32. At a length of 10 parallel plate varactor segments, the phase shifter has a figure of merit of 22.99 degrees/dB at 15 GHz. At this frequency, the phase shift is 292.2 degrees and the insertion loss is -7.31 dB.

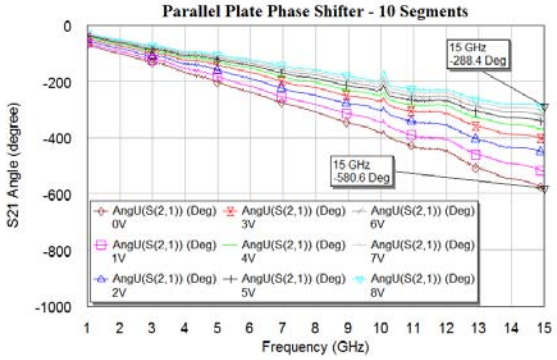


Figure 31: 10 Segment Phase Shifter - S_{21} Phase Angle

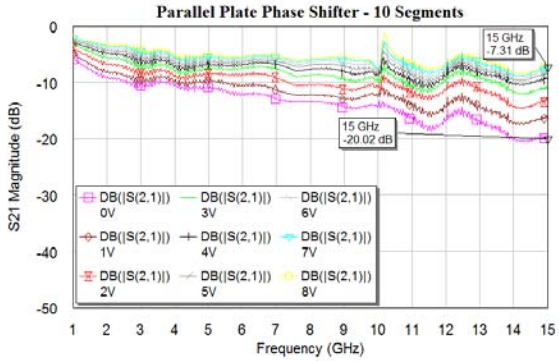


Figure 32: 10 Segment Phase Shifter - S_{21} Magnitude

$$FOM(15\ GHz) = \frac{\angle S_{21}(8V) - \angle S_{21}(0V)}{|S_{21}|_{dB}(8V) - |S_{21}|_{dB}(0V)} = \frac{580.6 - 288.4}{20.02 - 7.31} = 22.99$$

$$< degree/dB >$$

6.2.2 Phase Shifter - 15 Segments

The frequency sweep of the magnitude and phase angle of S_{21} is shown in Figures 33-34. At a length of 15 parallel plate varactor segments, the phase shifter has a figure of merit of 24.90 degrees/dB at 15 GHz. The phase shift at this frequency is 413.1 degrees with an insertion loss of -10.1 dB.

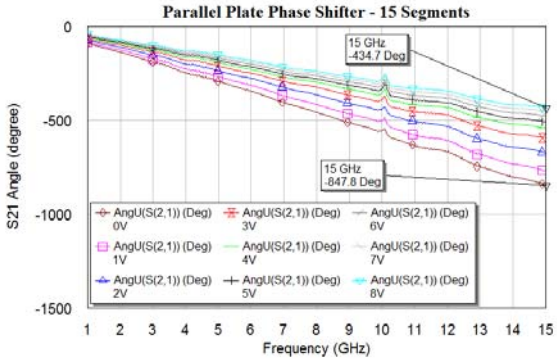


Figure 33: 15 Segment Phase Shifter - S_{21} Phase Angle

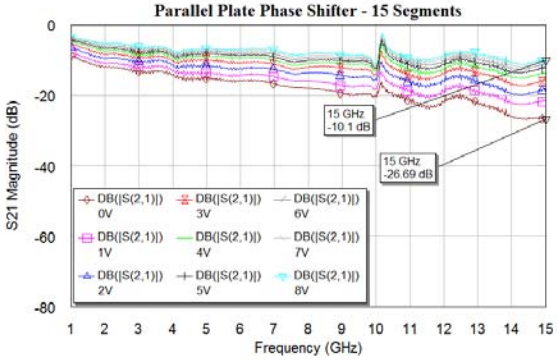


Figure 34: 15 Segment Phase Shifter - S_{21} Magnitude

$$FOM(15\ GHz) = \frac{\angle S_{21}(8V) - \angle S_{21}(0V)}{|S_{21}|_{dB}(8V) - |S_{21}|_{dB}(0V)} = \frac{847.8 - 434.7}{26.69 - 10.1} = 24.90$$

$$< degree/dB >$$

6.2.3 Phase Shifter - 20 Segments

The frequency sweep of the magnitude and phase angle of S_{21} is shown in Figures 35-36. At a length of 20 parallel plate varactor segments, the phase shifter has a figure of merit of 27.54 degrees/dB at 15 GHz. At this frequency, the phase shift is 533.7 degrees and the insertion loss is -13.15 dB.

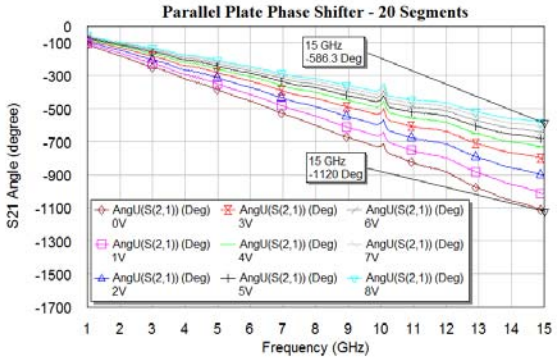


Figure 35: 20 Segment Phase Shifter - S_{21} Phase Angle

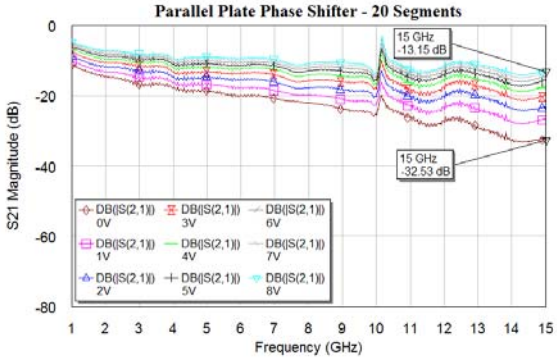


Figure 36: 20 Segment Phase Shifter - S_{21} Magnitude

$$FOM(15\ GHz) = \frac{\angle S_{21}(8V) - \angle S_{21}(0V)}{|S_{21}|_{dB}(8V) - |S_{21}|_{dB}(0V)} = \frac{1120 - 586.3}{32.53 - 13.15} = 27.54$$

$$< degree/dB >$$

6.2.4 Phase Shifter - 25 Segments

The frequency sweep of the magnitude and phase angle of S_{21} is shown in Figures 37-38. At a length of 25 parallel plate varactor segments, the phase shifter has a figure of merit of 19.33 degrees/dB at 15 GHz. At this frequency, the phase shifter exhibits a phase shift of 658.8 degrees and has an insertion loss of -14.56 dB.

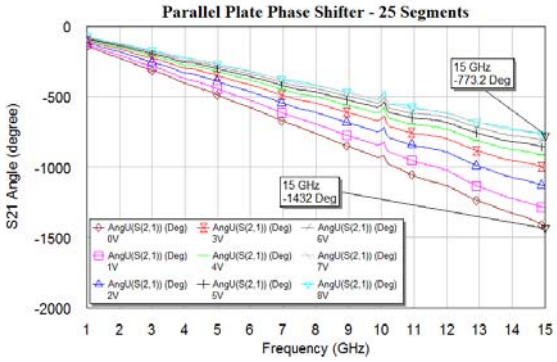


Figure 37: 25 Segment Phase Shifter - S_{21} Phase Angle

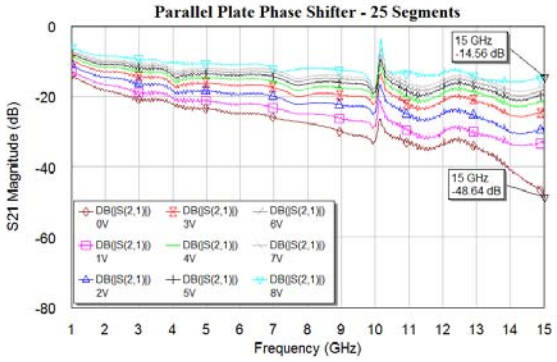


Figure 38: 25 Segment Phase Shifter - S_{21} Magnitude

$$FOM(15\ GHz) = \frac{\angle S_{21}(8V) - \angle S_{21}(0V)}{|S_{21}|_{dB}(8V) - |S_{21}|_{dB}(0V)} = \frac{1432 - 773.2}{48.64 - 14.56} = 19.33$$

$$< degree/dB >$$

6.3 Summary

Experimental testing of the parallel plate varactor based phase shifters yielded results that were closely related to the simulation results for both the S_{21} magnitude and phase angle. Tests of phase shifters of 10, 15, 20, and 25 segments in length yielded a FOM between 20-28 degrees/dB of phase shift at 15 GHz. With high phase shift angles ranging from ~300 - ~650 degrees, these phase shifters provide strong performance.

Phase shift was unable to be demonstrated with the single layer varactor based phase shifters. For the 10, 15, 20, and 25 segment phase shifters, the 8V dc bias was insufficient to create a noticeable difference in the phase angle. As was discussed previously, this is due to the higher gap width which reduces the electric field by a factor of 10. Experimental results at 0V DC bias shows potential for phase shift if a high enough voltage were able to be applied to the BST thin film. Additionally, simulation results matched well with the experimental results.

CONCLUSIONS AND FUTURE WORK

7.1 Conclusions

This section concludes the findings, both theoretical and experimental, on varactor based phase shifter functionality. The experimental testing of the parallel plate varactor based phase shifter yielded results that are consistent with simulated behaviors. As was evident for the 10, 15, 20 and 25 segment phase shifters, the experimental magnitude and phase angle were highly consistent with simulated results over the 5-15 GHz bandwidth of interest. The application of a 0-8V bias voltage successfully reduced the device capacitance in each phase shifter and created a sizeable phase shift. The FOM for the parallel plate phase shifters at 15 GHz ranged from 20-28 degrees/dB.

The experimental testing of the single layer phase shifters was successful in the absence of a DC bias voltage, but did not exhibit phase shifting behavior under the application of a 0V-8V voltage bias. Under these conditions, there was little to no changes seen in magnitude or phase angle of the phase shifter. This is attributed to the BST filled gap between the conductors being 10 times wider than in the parallel plate design. With this is mind, voltages of up to 80V would be required to see similar tuning performance in the single layer design as was seen in the parallel plate design due to the gap being 10 times larger. Testing at these voltages is not possible as it would result in the other devices on the wafer being damaged. Despite this setback, the measurements obtained from the single layer phase shifter are promising as they exhibited a relatively large phase angle and a very low amount of insertion loss.

7.2 Future Work

In order to better understand the tuning capabilities of the single layer varactor based phase shifter, more measurements need to be taken. This requires the application of a high voltage (up to 80V) bias in order to observe the same phase shifting behavior seen in the parallel plate varactor based phase shifter designs. Additionally, a single segment single layer varactor needs to be fabricated and tested in order to perform an accurate electrical model extraction. This proposed work will help in the development and verification of the single layer varactor models that have been presented throughout this thesis work.

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