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## Frequency agile low noise amplifier using barium strontium titanate (BST) thin film capacitors

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**FREQUENCY AGILE LOW NOISE AMPLIFIER USING  
BARIUM STRONTIUM TITANATE (BST)  
THIN FILM CAPACITORS**

Thesis

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the Degree

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by

Kari Groves

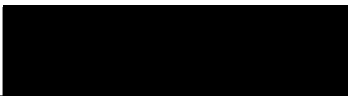
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## Frequency Agile Low Noise Amplifier using BST Thin Film Capacitors


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## **ABSTRACT**

### **FREQUENCY AGILE LOW NOISE AMPLIFIER WITH BARIUM STRONTIUM TITANATE (BST) THIN FILM CAPACITORS**

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The current advancements in military and wireless applications create the need for increased functionality with reduced cost and size. Highly integrated tunable electronics are necessary to meet these new requirements. Barium Strontium Titanium Oxide (BST) is a viable technology for these applications. This ferroelectric material offers significant benefits with its high tuning range, high power handling capability and low control voltages. While there is great interest in the development of BST technology, little research has been published regarding integrated matching networks using BST thin film parallel plate capacitors for an X-Band Low Noise Amplifier (LNA).

A frequency agile X-Band LNA design using BST thin film parallel plate capacitors for tuning capabilities is presented in this project. The LNA is designed for a tuning range between 9 and 11 GHz with a noise figure less than 3 dB. The LNA also maintains a bandwidth of 1.1 GHz throughout the tuning range. This design demonstrates the frequency tuning capabilities of the BST thin film capacitors in a critical RF front-end circuit.

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## INTRODUCTION

Current military advancements in Unmanned Air Vehicles (UAVs) and Micro Air Vehicles (MAVs) have resulted in strict requirements for high performance systems that limit acceptable tuning components. Conventional tuning devices such as RF MEMS and varactor diodes either require expensive packaging or have higher insertion loss leaving the need for a cost effective and low power technology with high tunability.

Barium Strontium Titanate (BST) material offers such capabilities as high tunability, fast switching speed, and lower control voltages. Along with their high integration potential, these properties help make BST material very appealing for new tunable technologies. This ferroelectric material can be used in many applications including frequency tuning. To demonstrate BST's frequency tuning capabilities, this project focuses on a design for an X-Band low noise amplifier (LNA) using BST capacitors in the matching networks.

## **CHAPTER I**

### **Defining the Project and Brief Background Information**

Frequency agile systems offer the ability to have one adaptable system meet multiple frequency band requirements without additional hardware. Tunability also allows for system optimization by compensating for fabrication variations. A viable technology for these emerging tunable systems is Barium Strontium Titanate (BST) thin films capacitors with their high tuning range and high potential for integration. This chapter introduces the LNA design along with the BST thin film capacitors. The objective of this project and overall process are described, as well as brief background information on the project.

#### **1.1 Objective**

The increasing interest in tunable electronics offers opportunities for voltage tunable dielectrics such as BST thin films for multiple applications. The objective of this project is to demonstrate the application of BST thin films in the design of a frequency agile X-Band LNA using the BST thin film capacitors for frequency tuning capability.

#### **1.2 Main Goals of the Project**

The main goal of the project is to design a frequency agile LNA along with related dropout circuits. Even though the desire is to have a highly integrated

solution for the LNA design, a hybrid circuit approach has been selected due to the limitations of the current fabrication technology to merge a microwave monolithic integrated circuit (MMIC) process with the BST thin film process. The overall objective is to develop the understanding of using the BST technology for radar and commercial applications with the development of the LNA that is a critical component of the RF front-end architecture. In view of the lack of a fully integrated processing technology, the LNA is designed with the idea of combining a commercial HJ-FET device with surface mount components packaged on a high resistivity silicon substrate. The surface mount components are used for the bias and stability networks of the LNA. The matching networks are fully designed using the components implemented on the BST thin film substrate.

The dropout circuits designed are (1) a simplified LNA design without bias networks, (2) the BST thin film capacitors used in the design, (3) the matching networks and (4) a set of resonant circuits. The resonant circuits are included for dielectric characterization.

### **1.3 Significance of the Project**

The dielectric constant tunability of BST thin films has many applications such as tunable filters, phase shifters and alternative gate dielectrics for devices. While much research has been done on using BST thin films in tunable matching networks, the novelty of this project is the design of the fully integrated BST thin film parallel plate capacitors in the matching and the biasing networks for the

coplanar waveguide (CPW) X-Band LNA. As a critical circuit in the RF front-end architecture for receivers, frequency agile LNAs offer the ability for operation over for multiple frequency bands. They can be used to reduce the cost and power of systems by implementing the thin films. Also the potential for high integration also makes the BST tuning highly desirable.

The shunt tuning capacitors in the matching networks of the amplifier use the BST material as the dielectric in a parallel plate capacitor structure. These capacitors can tune the LNA over the X-Band frequency range and increase the overall bandwidth of the amplifier. This also demonstrates an attractive application for the BST thin films.

#### **1.4 LNA Design and Specifications**

For transceiver applications utilized in both commercial and military systems, the noise figure of the amplifier greatly affects the overall system noise [1]. The noise figure of a receiver is defined as a measure of degradation of the signal to noise ratio. The LNA design often yields a trade-off between a desirable low noise figure and an acceptable gain [2]. These prove to be critical metrics for the overall design of the amplifier.

The LNA is designed to maintain a low noise figure while still providing maximum gain. In addition, the LNA is designed to have a tuning range from 9 – 11 GHz with an instantaneous bandwidth of 1 GHz. The amplifier will be optimized for the best performance at the center frequency,  $f_c$ , which is 10 GHz.

The input and output matching impedances of the LNA is to 50 ohms. Table 1.1 summarizes the specifications for the LNA design.

**Table 1.1: LNA Design Specifications**

<b>Requirement</b>	<b>Specification</b>	<b>Units</b>
Input Type	Single-Ended	-
Input Return Loss	-10	dB
Output Type	Single-Ended	-
Output Return Loss	-10	dB
Tuning Range	9 - 11	GHz
Bandwidth	1	GHz
Small Signal Gain	10	dB
Noise Figure	< 3	dB
Input BST Bias	<10	V
Output BST Bias	<10	V

Dropout circuits are designed to assist in the verification and the debugging process of the amplifier. These circuits are critical in determining the tuning capabilities of the BST thin film capacitors and the verification process of the substrate definition used in the simulations. All simulations of the amplifier and other designs use Microwave Office (MWO) version 7.01 from Applied Wave Research Inc. (AWR).

## **CHAPTER II**

### **BST Thin Film Background and Applications**

Currently there is a significant interest in the research of reconfigurable and tunable microelectronics for military and commercial applications. Ferroelectric thin films such as BST offer advantages over currently used devices in this market. In communication applications, the main devices used for tunable circuits are RF microelectromechanical systems (MEMS) and solid state varactor diodes. The mechanically based RF MEMS offer low insertion loss, excellent power handling and high linearity [3]. The main drawbacks are the high control voltage necessary (50-100V) along with the slow switching speed and the expensive large vacuum sealed packaging necessary for operation [4]. Another common alternative for RF MEMS are solid state varactor diodes. While these have a lower control voltage and faster tuning speed than the MEMS, they tend to have a higher insertion loss and have poor power handling capabilities in many applications [5]. BST thin films have the advantages of high tunability, fast switching speed and lower insertion loss. They also have low control voltages ( $<10\text{V}$ ) for high tunability and the capacity to be integrated in multiple substrates for different applications [6], [7]. These properties make them suitable for tunable systems. The general background of thin film BST material and different applications are explored in this chapter.

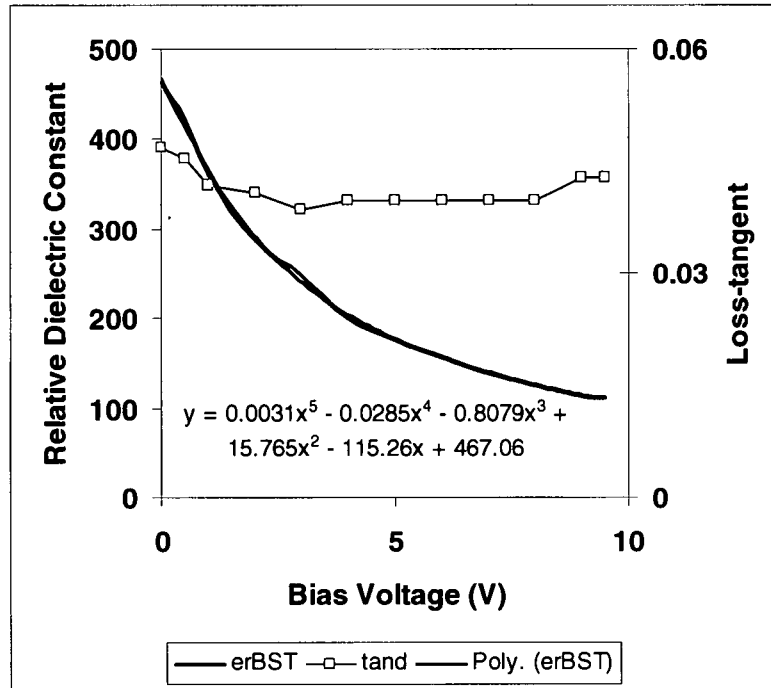


## 2.1 General BST Thin Film Characteristics

A ferroelectric material is a material whose permittivity can be changed by an applied DC electric field [8], [9]. This occurs due to the polar nature of these materials that the electric dipoles spontaneously re-orient or reverse when the field is applied. The maximum permittivity occurs at a temperature, referred to as the Curie-point, where the ferroelectric material switches to a paraelectric state [8]. Along with the high permittivity, ferroelectric materials have a high breakdown voltage that allow for high power handling capabilities [9].

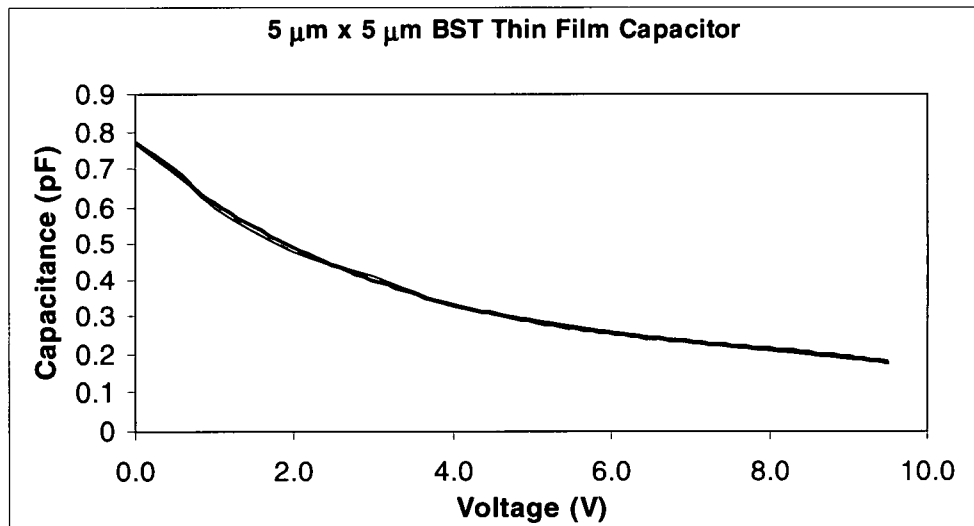
Since BST thin film materials have ferroelectric properties, an applied electrical field creates a nonlinear response in the electrical polarization [10]. When a small bias voltage between 0 - 10V is applied, the permittivity of thin film is changed causing a decrease in the dielectric constant of the BST thin film while maintaining a low loss tangent [11]. This characteristic makes BST thin film a good candidate for tunable applications.

BST thin films have a high dielectric constant of  $\epsilon_r \sim 300-700$  without an applied voltage [9]. This high dielectric material can be used for small-area capacitors and as the gate dielectric for MOSFET applications due to the high breakdown voltage associated with it. Figure 2.1 shows range of the dielectric constant with an applied bias voltage for a shunt  $5\ \mu\text{m} \times 5\ \mu\text{m}$  BST thin film capacitor [12]. Also this figure shows how the loss tangent of the BST thin film capacitor remains relatively constant as the bias voltage is applied.



**Figure 2.1: Relative Dielectric Constant and Loss-Tangent Based on the Bias Voltage**

The BST thin film's high tuning range with typical capabilities of 3:1 makes them appealing for tunable filters and phase shifters [11]. A design of a  $5 \mu\text{m} \times 5 \mu\text{m}$  BST thin film capacitor with a bias voltage range from 0-10 V can be tuned between 0.77 pF to 0.185 pF. This demonstrates a tuning range of 4:1. Figure 2.2 shows the nonlinear curve of this capacitance versus voltage applied. Capacitances of up to 200 pF are achievable, but require a larger surface area for the capacitor [13]. As the surface area increases, the loss tangent of the capacitor also increases. This may not be desirable in certain higher frequency applications.



**Figure 2.2: Nonlinear Capacitance Based on the Bias Voltage Plot**

## **2.2 Applications for Thin Film BST Materials**

The most common application for BST thin film capacitors are tunable filters and matching networks. These applications take advantage of the large tuning range available with BST thin film capacitors [14 - 20]. An article published in the 2001 *Microwave Symposium Digest* presented multiple tunable filters using BST thin film capacitors [4]. A tunable 3<sup>rd</sup> Chebychev lowpass filter using BST thin film capacitors was designed and measured to have a 3 dB cut-off frequency ranging from 160 MHz to 210 MHz with a bias voltage of 9V. This demonstrated a 30% tunability range for the filter. A second filter was designed as a 5<sup>th</sup> order tunable lowpass filter with BST thin film capacitors. This filter measured a 3 dB cut-off frequency ranging from 120 MHz to 170 MHz with a tuning range of 40%. A bandpass filter with BST thin film capacitors resulted in 45% tuning range with a center frequency ranging from 140 MHz to 200 MHz with a bias voltage of 10 V. This clearly demonstrates the high tuning capabilities

of the BST thin film capacitors in filter applications. In the 2005 *IEEE Microwave Theory and Techniques*, a research team demonstrated a 3<sup>rd</sup> order tunable combline bandpass filter using BST thin film interdigitated capacitors (IDC) [10]. An individual IDC showed a 12% tuning range with a bias voltage of 35 V at 1 MHz. The bandpass filter showed 16% tunability with a bandwidth of 400 MHz. Overall the BST thin film capacitors have high tuning range making them ideal for tunable filters and matching networks.

Another application where BST thin films can be used is in phase shifters. Electronic beam steering of phased array antennas use phase shifters to adjust and control the width and angle of the beam [21]. The large number of phased array applications provides many opportunities for more efficient and cost effective phase shifters. Applying voltage to the BST thin film layer changes the permittivity and alters the phase velocity of the propagating wave [22]. A research team from the Electronics and Telecommunications Research Institute in Korea demonstrated a voltage tunable BST varactor with a dielectric tunability of 69% used in an X-Band phase shifter [23]. The figure of merit for this phase shifter was 28.7 deg. /dB at 10 GHz [23]. This also demonstrates how the phase shifter can be integrated onto the same substrate as microwave components reducing the need for multiple substrates [21]. Another study from the University of California, Santa Barbra demonstrated a BST thin film Ka-Band phase shifter that had a continuous 0 – 157 degree phase shift at 30 GHz [24]. The phase shifter was based on a CPW transmission line that was periodically loaded with BST capacitors. Overall 9 BST capacitors were used in the phase shifter. The

high tuning range of the BST thin film and the potential low cost are the benefits of using phase shifters with BST thin film dielectric layers.

Along with the phase shifters, microstrip antennas for many radar applications show great promise for BST thin films. Current microstrip antennas offer lower fabrication costs for large, light weight arrays but are often limited by the bandwidth. Adding tunability to microstrip antennas offers a greater bandwidth while still maintaining the necessary performance [25]. In an article from the 1999 *Smart Materials and Structures*, a group at Pennsylvania State University fabricated a microstrip patch antenna with a BST thin film dielectric [26]. The dimensions for the microstrip antenna were 4.60 cm by 3.35 cm. The bandwidth of the antenna without an applied voltage was measured as 1%. With an applied DC voltage, the bandwidth of the antenna was increased to 3% or a 3:1 increase. By adjusting the dielectric constant of the BST thin film layer with a varying bias voltage, the resonant frequency of the antenna resulted in an increase of the antenna's overall bandwidth [25], [26]. The tuning capability of the thin films will help to develop larger bandwidths for antennas.

The MOSFET industry is also interested in ferroelectric materials. Dynamic random access memory (DRAM) using MOSFETs with alternative gate dielectrics are in response to the need for reduction in power and chip size. This ongoing movement towards reduced chip size and power consumption has resulted in an increased gate leakage current for MOSFETs with SiO<sub>2</sub> gate dielectrics. The high dielectric constant of the BST thin films and their low leakage current make them a strong option for alternative gate dielectrics in

MOSFETs [27]. An article published in the 2005 *Journal of Physics: Conference Series* presented a study on the comparison of traditional SiO<sub>2</sub> MOSFETs and MOSFETs with alternative gate dielectrics for DRAM cells [28]. The group found that SiO<sub>2</sub> MOSFETs held a '1' value for 37 ns while the DRAM with the devices that had BST dielectric held a '1' value for 224 ns. Using BST thin films for the gate dielectric improved the performance by holding the correct value for significantly longer than the traditional SiO<sub>2</sub> MOSFETs. This development can help to break the way for gigabit density memory [8].

Also another application for BST thin film materials is in voltage controlled oscillators (VCO). A VCO is an oscillator that is controlled by a voltage input designed for oscillation at a specific frequency. In communication systems, these VCOs are a critical part of a phased locked loop. The tunability of the BST thin film varactors offers an opportunity for tunable VCOs along with other benefits. A group at the University of Colorado presented a VCO based on a Colpitts architecture with BST varactors [29]. The BST thin film varactor had a tunability of 17% for a 3V variation in the bias voltage. The VCO had a tunability of 4% with a minimum frequency of 577.3 MHz. The group suggested that the VCO's tunability was reduced due to the non-tunable parasitic capacitances and that the VCO's tunability has the potential to be equal to the BST varactor. This demonstrates one of the benefits of the BST thin film tunability over traditional semiconductor varactors. In the 2004 IEEE *Radio and Wireless Conference*, a research team from North Carolina State University presented their study on the comparison of a VCO with a traditional semiconductor varactor and a VCO with a

BST thin film varactor for the tuning element [13]. The BST thin varactor had a capacitance of 200 pf with a tuning range of 3:1 with a bias voltage from 0 - 12 V. The VCO with the BST thin film varactor had 11 dB more second harmonic rejection compared to the semiconductor VCO. This result is very critical for many VCO applications. BST varactor based VCO can increase the tunability of VCO designs and offer better harmonic rejection capabilities.

## **CHAPTER III**

### **Parts and Materials**

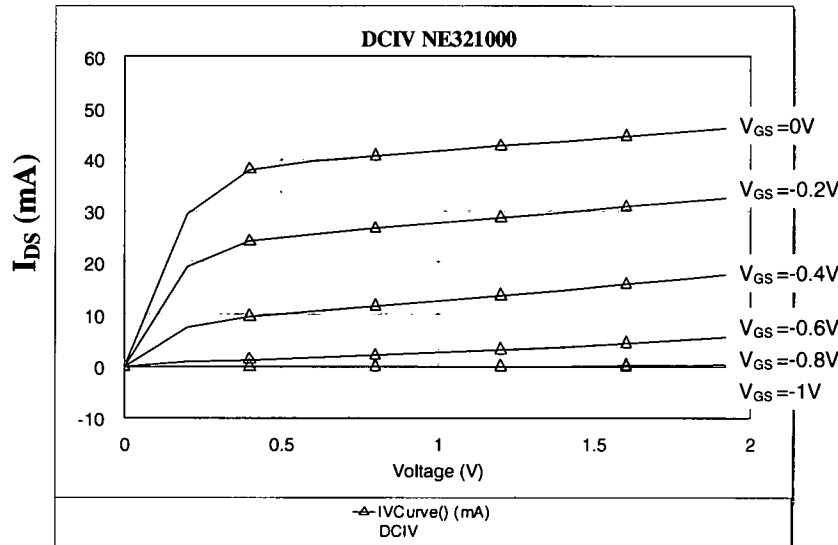
Due to the partial hybrid nature of this LNA design discussed in Chapter 1, the characteristics of the different components play a critical role in the performance of the LNA. This chapter discusses the characteristics of the transistor, the substrate and the surface mount components used in LNA design.

#### **3.1 NEC NE321000 Hetero Junction Fieldeffect Transistor**

The NE32100 super low noise amplifier N-channel hetero junction fieldeffect transistor, HJ-FET, by NEC was selected for the LNA design. This bare die transistor is best utilized between C to Ka-Band frequency and has an operating frequency of 2 – 30 GHz. The combination of the low noise figure in the X-Band frequency range and the associated gain make this HJ-FET ideal for the LNA. At 10 GHz, the minimum noise figure is 0.28 dB and the available gain is 13.4 dB. The manufacturer's recommended operating conditions given for the transistor are the drain to source voltage,  $V_{DS} = 2V$  and the drain current,  $I_D = 10$  mA.

Figure 3.1 shows the I-V curves for the HJ-FET. The curves show the drain current as a function of  $V_{DS}$  as the gate to source voltage,  $V_{GS}$ , is stepped from 0 to -1 V. A  $V_{GS}$  is chosen that yields an  $I_D$  equal to 10 mA. Refer to Appendix A for the transistor's data sheet.





**Figure 3.1: Drain Current versus Drain to Source for HJ-FET**

The S-parameters and noise parameters of a transistor influence the design process for the matching and stability networks. The S-parameters of the transistor were measured using an Agilent 8720ES Vector Network Analyzer. Measurements were taken using two ground-signal-ground (GSG) 125  $\mu\text{m}$  pitch Infinity probes. It was difficult to measure the transistor with the available probes due to the transistor's small footprint. The transistor's bare die overall dimensions are 300  $\mu\text{m}$  by 300  $\mu\text{m}$ . The width of the source is 56  $\mu\text{m}$ . The gate width is 61  $\mu\text{m}$  and the drain width is 58  $\mu\text{m}$ . More accurate measurements can be taken using a probe with a smaller pitch. Therefore the transistors were only tested to verify functionality and for comparison to the provided MWO transistor model from the manufacturer. The MWO transistor model's S-parameter simulation is comparable to the measured data and is used for all simulations discussed from this point forward in this project.

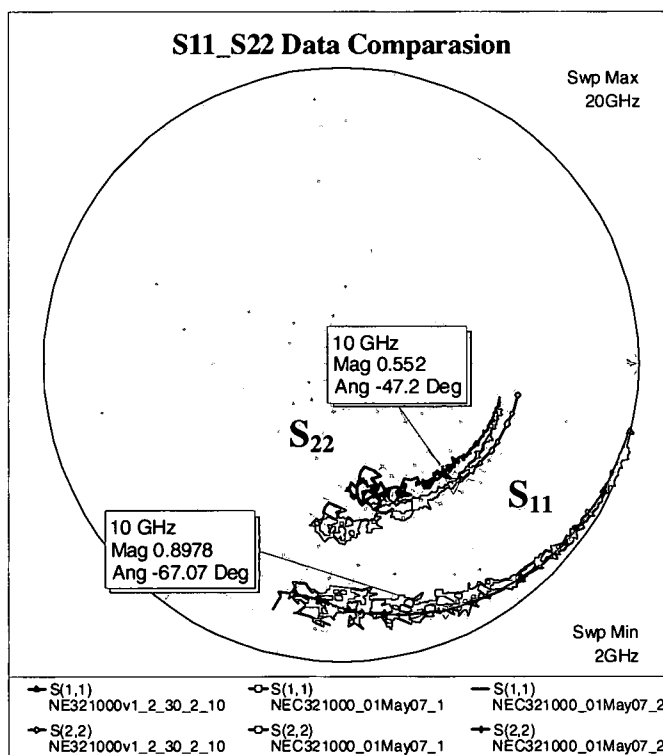
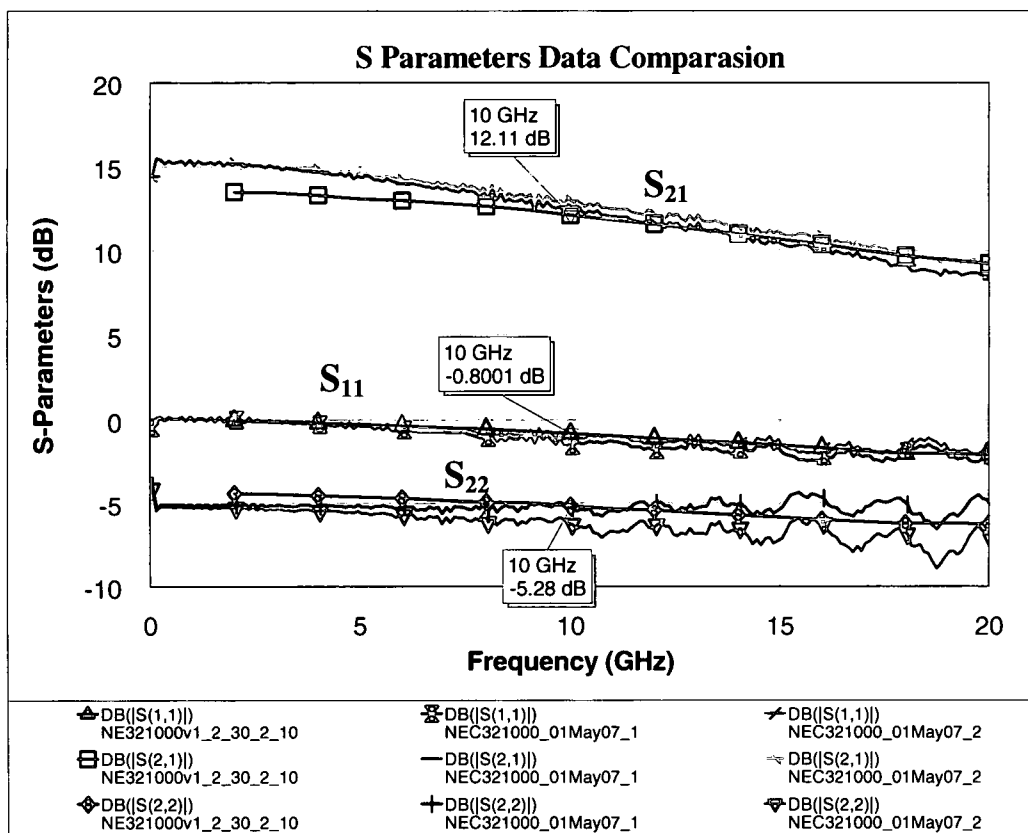


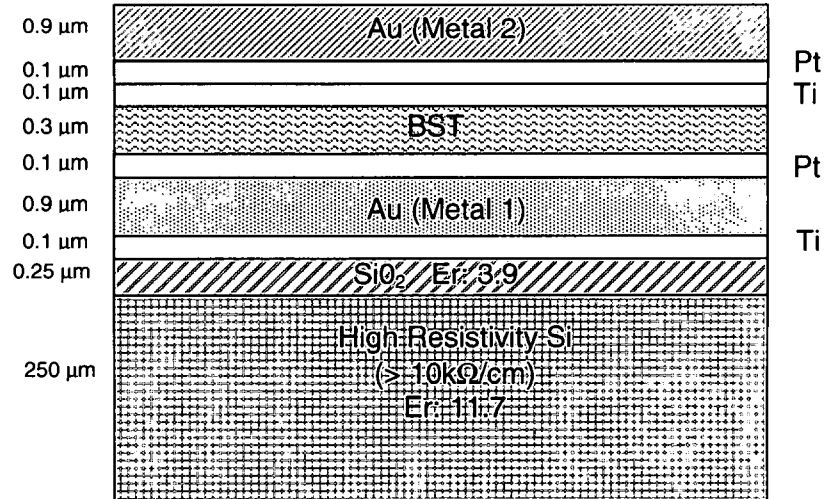
Figure 3.2: S-Parameter Comparison of the Measured Data and MWO Transistor Model

Overall the NE32100 HJ-FET is a good choice for the LNA design. The low noise figure, the available gain and the bare die chip meet the requirements necessary for this project and allow for the transistor to be easily integrated on the final LNA.

### **3.2 Substrate Description**

The selected fabrication process uses high resistivity silicon (Si) with a thin layer of  $\text{SiO}_2$  for the BST thin film substrate. High resistivity silicon is used for the lower loss tangents available with it at microwave frequencies and the interest in future integration with other Si substrates [6]. The bottom metal layer is a stack of Titanium (Ti), which is primarily used as an adhesion layer, a thick gold (Au) layer, followed by a thin Platinum (Pt) for providing a good interface with BST thin film. Gold has good conductive properties and make it a good choice for the RF metal layers. The Titanium (Ti) and Platinum (Pt) are used to aid in the adhesion of the thin film BST material [12]. The top metal layer (metal2) consists of a thin Ti layer, followed by a thin Pt layer, and a thick gold layer, serving as the RF metal. It is critical to use Ti/Pt layers on either side of BST for providing a good interface with BST, as Pt acts as an excellent barrier for oxygen diffusion. The process for depositing the metal layers for this fabrication uses a standard positive photoresist lift-off photolithography. A process-controlled pulse laser deposition system deposits the BST thin film across the entire wafer [11].

The diagram of the substrate in Figure 3.3 shows the different substrate layers and their thicknesses.



**Figure 3.3: Cross Sectional View of the Layers**

With this substrate, the CPW transmission lines are designed for 50  $\Omega$  characteristic impedance with the signal line width of 50  $\mu\text{m}$  and the spacing between the signal and the ground plane being 50  $\mu\text{m}$  as well [12]. This was determined using the transmission line tool in MWO with substrate thickness found in Figure 3.3.

### 3.3 Surface Mount Components

The hybrid nature of the bias and the stability networks of the LNA require surface mount capacitors and inductors. The design requires a 5.2 pF surface mount capacitor for the stability network and one 10 pF surface mount capacitor for each of the bias networks. The ATC 500 series chip capacitors manufactured

by American Technical Ceramics (ATC) were readily available. ATC is recognized as a leading manufacturer of surface mount capacitors operating at microwave frequencies. The selected surface mount capacitors have a 0603 case size (1.00 mm x 1.10 mm).

The design requires a 5 nH inductor for the drain bias network and a 11 nH inductor for the gate bias network. The 0201CS series inductors manufactured by Coilcraft have the smallest footprint available. Coilcraft is recognized as a leading manufacturer of surface mount inductors. The selected inductors have a 0503 case size (0.56 mm x 0.36 mm).

Both components fulfill the needed specification for the design of the bias and stability networks. Data sheets are found in Appendix B and Appendix C.

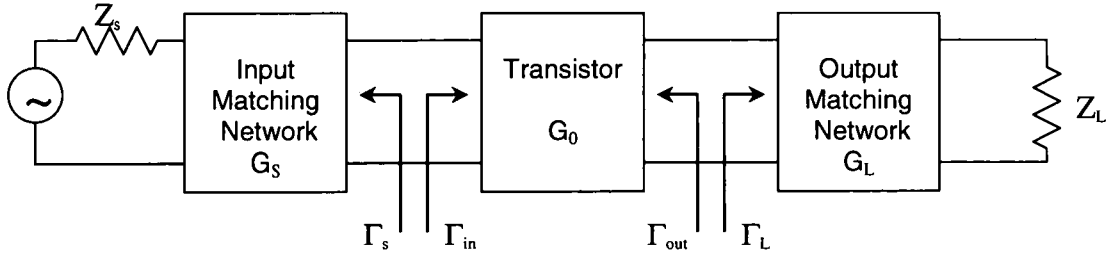
## CHAPTER IV

### LNA: Design and Experimental

This chapter gives a brief background on amplifier design and the process used for this project. The ideal LNA design is simulated along with the BST thin film capacitors using MWO. The simulation schematics for the LNA and the dropout circuits are also discussed in this chapter.

#### 4.1 Design Methodology

The two-port network shown below is a block diagram of an amplifier with matching networks. This diagram shows the reflection coefficients associated with the two-port network. A reflection coefficient,  $\Gamma$ , is defined as a ratio of the impedance or the amplitude of the signal. The source reflection coefficient,  $\Gamma_s$ , is a function of the source impedance with respect to  $Z_0$ , the characteristic impedance. The load reflection coefficient,  $\Gamma_L$ , is a function of the load impedance,  $Z_L$  with respect to  $Z_0$ . The reference characteristic impedance for this project is 50  $\Omega$ . The equations for source reflection coefficient and load reflection coefficient are also shown below [2].



**Figure 4.1: Block Diagram of a Two-Port Network**

$$\Gamma_s = \frac{Z_s - Z_0}{Z_s + Z_0} \quad (4.1)$$

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0} \quad (4.2)$$

The input reflection coefficient,  $\Gamma_{in}$ , and output reflection coefficient,  $\Gamma_{out}$ , are a function of the source and load reflection coefficients and the S-parameters of the transistor. The expressions for them are as follows [2]:

$$\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \quad (4.3)$$

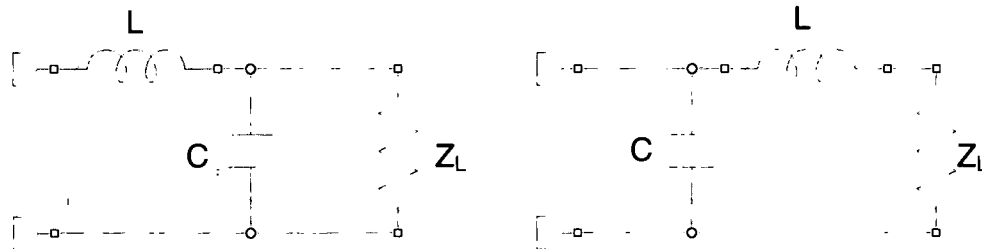
$$\Gamma_{out} = S_{22} + \frac{S_{12}S_{21}\Gamma_s}{1 - S_{11}\Gamma_s} \quad (4.4)$$

When designing an amplifier, the first step is to determine the stability of the transistor at the operational frequencies of the design. Stability is defined as the resistance to oscillation. It is a critical design requirement because certain combinations of source and load impedances can cause the system to be unstable and therefore not functional [1]. The Stern stability factor,  $K$ , can be used to determine the overall stability of the design. The stability factor is defined in the expression below.  $\Delta$  is a function of the S-parameters of the

transistor. When  $K > 1$  and  $\Delta < 1$ , the design is considered unconditionally stable and will not oscillate under different impedances from the source and load [2].

$$K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2 |S_{21}| |S_{12}|} \quad \text{with } \Delta = S_{11}S_{22} - S_{12}S_{21} \quad (4.5)$$

Matching networks are used to optimize the performance of the amplifier by providing proper termination at the input and the output ports of the transistor [30]. Simple matching networks are effectively lowpass and highpass filters. A lowpass filter only allows the lower frequencies to DC pass and rejects the higher frequencies. A shunt capacitor or a series inductor acts as a simple lowpass filter. A combination of these two elements creates a higher-order filter which has a sharper cutoff for the skirt of the filter [2]. Figure 4.2 shows example topologies of the simple lowpass filters used in matching networks.

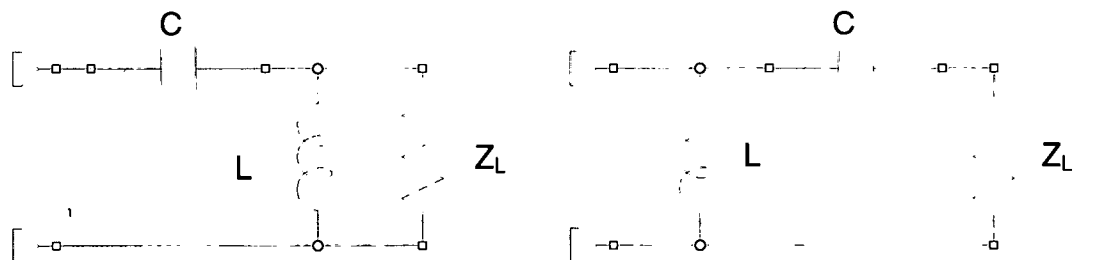


**Figure 4.2: Lowpass Filter Topologies used in Matching Networks**

A highpass filter rejects the lower frequencies while allowing the higher frequencies to pass. A series capacitor or a shunt inductor acts as a simple highpass filter. Like the lowpass filter, a combination of these elements will also create a higher-order filter which will have a sharper cutoff for the filter's skirt [2].

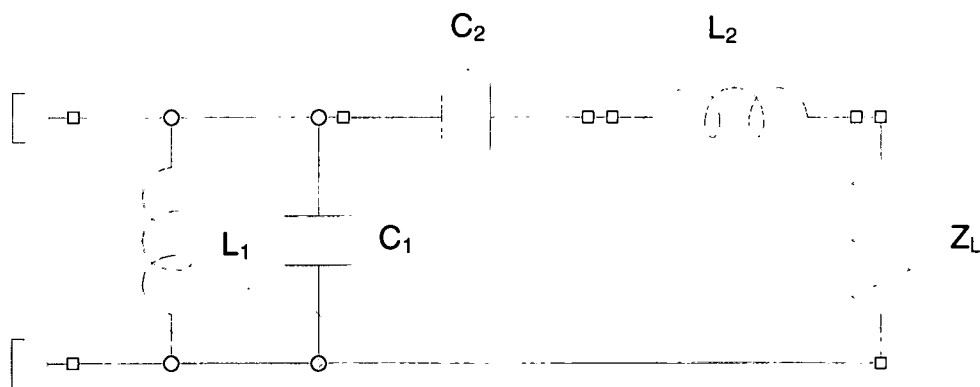


Figure 4.3 shows example topologies of the highpass filters used in matching networks.



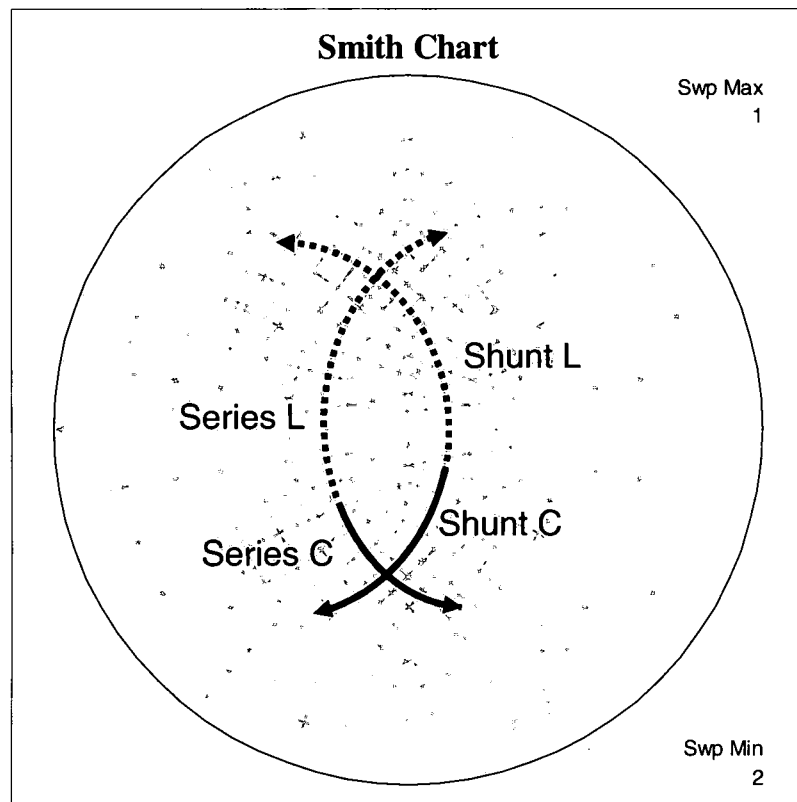
**Figure 4.3: Highpass Filter Topologies used in Matching Networks**

Bandpass filters can also be used in matching networks. A bandpass filter is a combination of a lowpass and a highpass filter. This filter only allows a certain band of frequencies to pass and rejects all other frequencies [2]. Figure 4.4 shows an example topology of the bandpass filters used in matching networks.



**Figure 4.4: Lowpass Filter Topology used in Matching Networks**

When designing the matching networks, a Smith chart can be used to see the effects of the elements added to the matching networks. A shunt capacitor moves clockwise along a constant-conductance circle while a series capacitor moves counter-clockwise along a constant-resistance circle on the Smith chart. Similarly, a shunt inductor moves counter-clockwise along a constant-conductance circle while a series inductor moves clockwise along a constant-resistance circle on the Smith chart [30]. Figure 4.5 shows the effects of adding a series and a shunt element in matching networks on a Smith chart.



**Figure 4.5: Smith Chart Showing Effects of Adding Series and Shunt Elements**

For an amplifier design, it is important to maximize the gain produced by the amplifier to meet the gain requirements. The transducer gain,  $G_T$ , accounts for mismatch in the source and the load. It is easiest to define the separate effective gain factors for each of the three blocks shown in the Figure 4.1 that effect the transducer gain [2]. The effective gain factors for input matching network,  $G_S$ , the transistor,  $G_0$ , and the output matching network,  $G_L$ , are shown in the equations below:

$$G_S = \frac{1 - |\Gamma_S|^2}{|1 - S_{11}\Gamma_S|^2} \quad (4.6)$$

$$G_0 = |S_{21}|^2 \quad (4.7)$$

$$G_L = \frac{1 - |\Gamma_L|^2}{|1 - S_{22}\Gamma_L|^2} \quad (4.8)$$

The overall transducer gain can is shown below in Equation 4.9 as a function of all three effective gain factors [2].

$$G_T = G_S G_0 G_L \quad (4.9)$$

LNA designs often require a compromise between maximum available gain and low noise figure. The noise figure, NF, is a measure of the noise performance in the overall amplifier. The simplest expression for NF is a ratio of the signal-to-noise ratio at the input,  $SNR_{in}$  over the signal-to-noise ratio at the output,  $SNR_{out}$  [2].

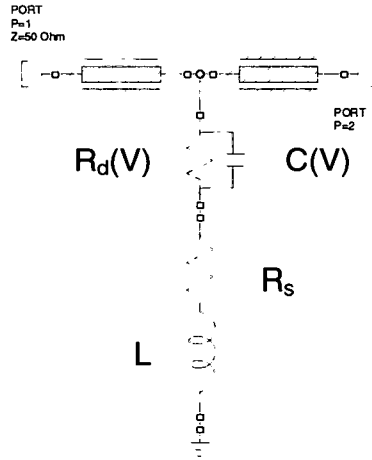
$$NF = \frac{SNR_{in}}{SNR_{out}} \quad (4.10)$$

Another way to calculate the NF is to use an equation that is a function of the transistor noise resistance,  $R_N$ , the optimum source resistance,  $\Gamma_{opt}$ , and the source reflection coefficient,  $\Gamma_S$ . The ideal NF for an amplifier is zero or 1 dB but this is difficult to obtain due to noise inherent in any transistor. Therefore the lowest obtainable NF is when the source reflection coefficient equals the optimum source resistance of the transistor allowing the NF to equal  $F_{min}$  as shown below [2].

$$NF = F_{min} + \frac{4R_N}{Z_0} \frac{|\Gamma_S - \Gamma_{opt}|^2}{(1 - |\Gamma_S|^2)(1 + |\Gamma_{opt}|^2)} \quad (4.11)$$

#### 4.2 BST Thin Film Capacitor Model

The complex model representation of the BST thin film capacitor is shown in Figure 4.6. This model accounts for the parasitic inductance,  $L$ , and resistances,  $R_s$  and  $R_d$ , associated with it. In this model,  $C(V)$  represents the tunable capacitance with respect to the applied bias voltage. The series resistance of the platinum layer,  $R_s$ , is a function of the conductivity of Pt,  $\sigma$ , the width of the conductor,  $w$ , the length of the line shunted to ground,  $l$ , and the thickness of the conductor,  $t$ . The inductance of the line,  $L$ , is a function of the  $Z_0$ , the operation frequency,  $f$ , and the guide wavelength,  $\lambda$ . The shunt resistance,  $R_d(V)$ , is a function of the loss-tangent of the BST thin film,  $\tan\delta$  and the  $C(V)$ . The equations for calculating the different values of resistors and inductance are shown in the expressions below [12].



$$R_s = 1/(\sigma \omega t) \quad (4.12)$$

$$L = (Z_0/(2\pi f)) \sin(2\pi d/\lambda g) \quad (4.13)$$

$$R_d(V) = 1/(\omega C(V) \tan \delta) \quad (4.14)$$

**Figure 4.6: BST Thin Film Capacitor Complex Model**

For this design, a simplified model is used based on an equivalent equation to determine the capacitance. Equation 4.15 was derived from the experimental data shown in Figure 2.2 for the BST thin film capacitor with a 5  $\mu\text{m}$  by 5  $\mu\text{m}$  surface area. This non-linear equation is used for the capacitance value in the MWO closed form capacitor model with a quality factor, Q, of 50. This simplified model allows for easy simulation of the capacitance tuning by varying the bias voltage, V, using the tuning tool in MWO [12].

$$C(V) = -0.0009V^3 + 0.021V^2 - 0.1788V + 0.771 \quad (4.15)$$

### 4.3 Ideal LNA

An ideal schematic for the LNA is designed with MWO using the ideal lumped element models for the different components. This ideal LNA design is used to determine the topologies for the different networks in the design. Also the ideal LNA is optimized to meet all of the design specifications for this project.

#### 4.3.1 Stability for the Ideal LNA

After reviewing the stability factor for the transistor, a stability network is needed to maintain an unconditionally stable state for the amplifier. The first topology for the stability network is an inductor in series with a resistor and capacitor all shunted to ground as seen in Figure 4.6.

After tuning and optimization of the ideal LNA, the network no longer required a resistor and was reduced to only the inductor and capacitor. The stability of the circuit is determined by plotting the stability factor,  $K$ , to verify that  $K$  is greater than 1 for the desired frequency range of the amplifier.

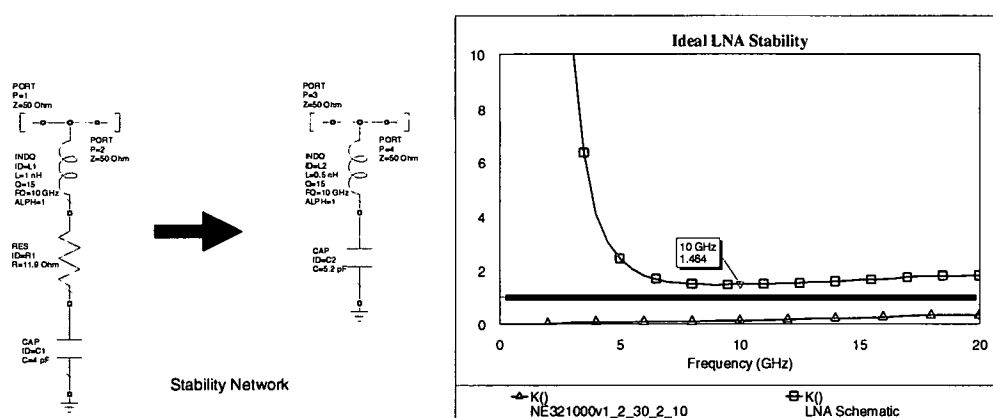


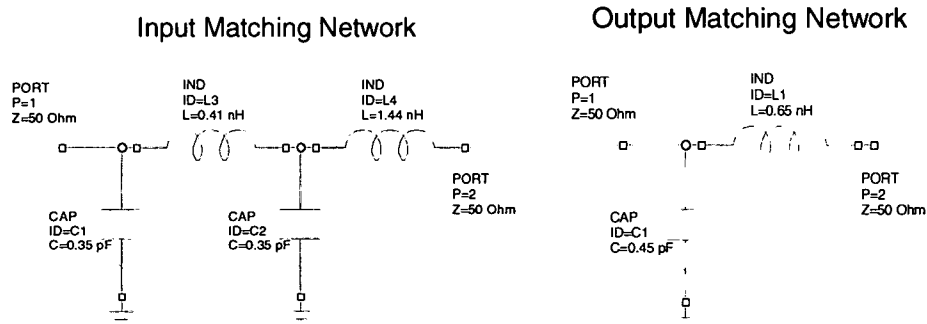
Figure 4.7: Stability Network and Stability Plot for Ideal LNA

### 4.3.2 Ideal LNA Matching Networks

The next step in the process is to design the matching networks for the ideal LNA. The MWO closed-form models are used as the ideal lumped elements in the matching networks. Both highpass filters and lowpass filters were reviewed for the matching network topologies. Due to the lack of vias, the selected fabrication process promotes the use of shunt BST thin film capacitors over series BST thin film capacitors in the matching networks. Since a highpass filter topology required a series capacitor, a lowpass filter topology was selected.

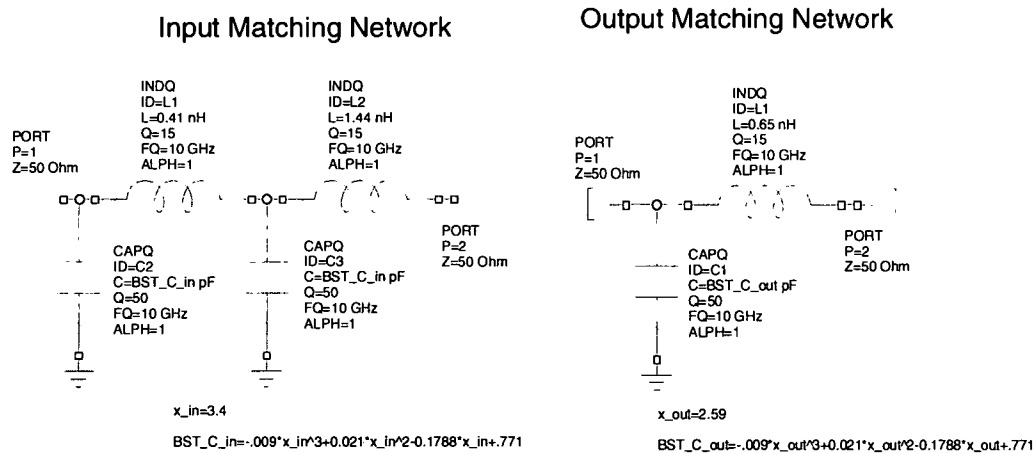
The lowpass filter topology used is a shunt capacitor followed by a series inductor [30]. The input matching network is a two-stage lowpass filter. A single stage lowpass filter did not achieve the necessary return loss for the amplifier design. Adding a second stage to the lowpass filter provided sufficient return loss.

The output matching network is a single stage lowpass filter. It uses the same topology as the input matching network. Only one stage is needed for the output matching network because the stability network is tuned to act as part of the matching network. Figure 4.8 shows both matching networks using the ideal lumped element models.



**Figure 4.8: Input and Output Matching Network for the Ideal LNA**

The ideal shunt capacitors in both matching networks are then replaced with the simplified BST thin film capacitor model discussed in Section 4.2. The tuning tool in MWO is used to adjust the bias voltage in the equation and optimize the capacitance value needed in the matching networks. Figure 4.9 shows both schematics for the input matching network and the output matching network using the simplified BST thin film capacitor model.



**Figure 4.9: Input and Output Matching Network with BST Thin Film Capacitors**



### 4.3.3 Ideal LNA Biasing Networks

As discussed in Chapter 2, a bias voltage is necessary for tuning the BST thin film capacitors. Each capacitor can be biased separately through an individual bias network. This will allow for greater control of the tuning capabilities of the different BST thin film capacitors. Also it would increase the number of bias networks and probe pads needed for the overall LNA design. Another method is to bias the BST thin film capacitors through the RF signal transmission lines. This allows for ease of biasing control of the BST thin film capacitors but reduces the number of overall bias networks and probe pads required for the LNA design. The BST thin film capacitors for this LNA design are biased through the RF signal lines to help minimize the number of bias networks required for the design.

Since the RF signal lines are not available for the biasing, the FET device required additional DC biasing networks. A large inductor, often referred to as an RF choke, is used to block the RF signal from entering the DC source. The value of this inductor is the smallest inductance that is still large enough to block the RF signal without interfering with the matching networks. This design uses an 11 nH inductor for the RF choke in the gate bias network and a 5 nH inductor in the drain bias network. Also a large value capacitor shunted to ground is used as a decoupling capacitor and a pathway to ground for the AC current [1]. A 10 pF capacitor is used for this capacitor for both bias networks. Both the gate and the drain bias networks are the same topology for this design.

Using the RF signal lines for biasing of the BST thin film capacitors creates a biasing conflict with the HJ-FET. This is resolved by using series capacitors to block the BST thin film capacitor biasing voltage from the transistor. These capacitors are referred to as DC blocking capacitors. The initial design used surface mount capacitors for the DC blocking capacitors on the RF transmission line due to the large capacitance required to block bias from the BST thin film capacitors. The large pad structure necessary to attach the surface mount capacitors resulted in a significant degradation in the performance of the LNA. This pad structure caused a 3 dB drop in the gain of the LNA as well as a 100 MHz reduction in the instantaneous bandwidth.

Next BST thin film capacitors were considered for the DC blocking capacitors. A  $20\text{ }\mu\text{m} \times 20\text{ }\mu\text{m}$  BST capacitor is used as the DC blocking capacitor. Surface areas smaller than  $20\text{ }\mu\text{m} \times 20\text{ }\mu\text{m}$  did not provide a large enough capacitance to block the DC voltage. Any larger surface area would have added additional loss to the design. Using the BST capacitors for the DC blocking capacitors keeps the LNA layout as a more integrated design and eliminates additional packaging after fabrication.

#### **4.3.4 Ideal LNA Schematic**

Figure 4.10 shows the completed schematic for the ideal LNA. The rectangle in the center of the schematic is the manufacturer's model for the HJ-FET used in this project. The input matching network on the left and the output matching network on the right use the simplified BST thin film capacitor model for

the shunt capacitors. The bias networks and the stability network are also shown in the schematic below.

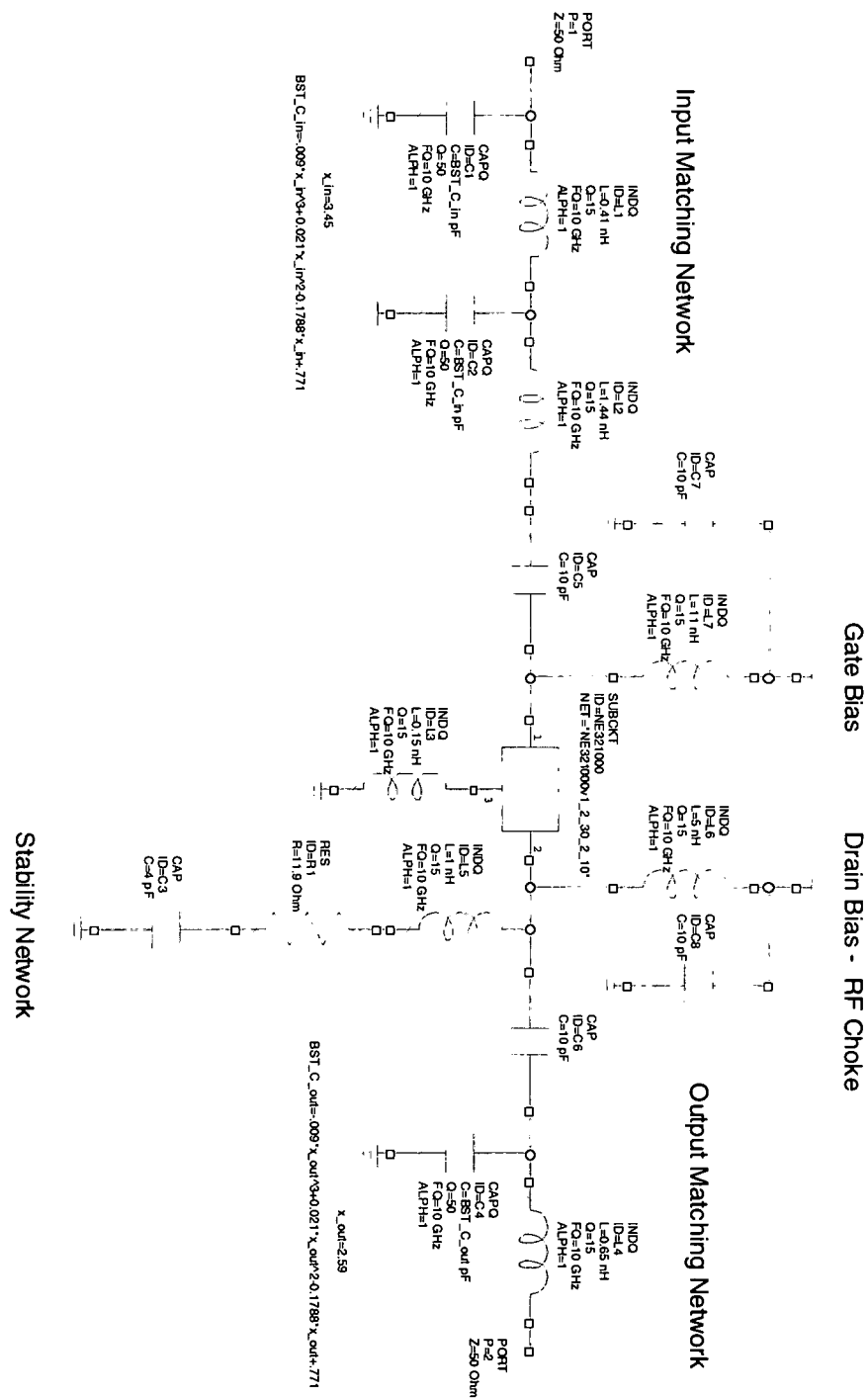


Figure 4.10: Ideal LNA with BST Thin Film Capacitors and Bias Networks

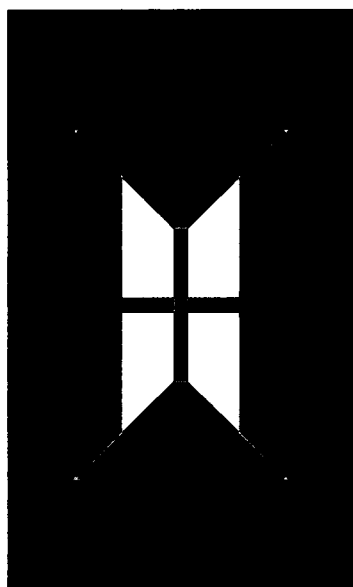
#### **4.4 LNA Simulation**

Once the ideal LNA has been designed using ideal lumped elements, the next step is to convert the design to reflect the actual circuit layout. MWO models are used to capture the interconnects of the amplifier, the surface mount components and the BST thin film capacitors. By adding these models to the schematic, it allows for a closer simulation to the actual fabricated LNA and helps in determining possible issues that might arise in the processing. The CPW substrate model is used in MWO for the CPW transmission lines. MWO's CPW substrate model is populated with the parameters from the BST thin film process substrate definition discussed in Chapter 3. CPW transmission lines are used to simulate the interconnects which is critical to ensure design accuracy. Since the process has no vias between the top and lower metal layers, the CPW transmission line design approach allows for an easily assessable RF ground plane. Also CPW has good isolation properties because of the proximity of this ground plane. Microstrip lines were not used because of the selected fabrication process.

##### **4.4.1 Simulation of BST Thin Film Capacitor Layout**

The BST thin film capacitor uses a CPW transmission line design on the substrate shown in the cross sectional view in Figure 2.3. A parallel plate capacitor layout with the BST thin film as the dielectric layer is ideal for this fabrication process. The shunt capacitor is created by a perpendicular overlay of

two 5  $\mu\text{m}$  width transmission lines. The metal 1 layer transmission line connects with the parallel ground plane to the metal 2 layer. Both metal layers have large parallel ground planes which are effectively shorted through the capacitive coupling [12]. The two large ground planes create a large capacitance that allows the BST capacitor to be shunted to ground without a need for a via connection. Figure 4.11 shows the layout of the capacitor with the orange representing the metal2 layer and green representing the metal1 layer.

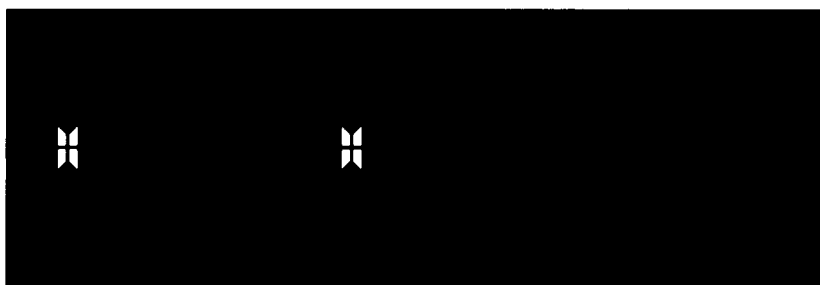
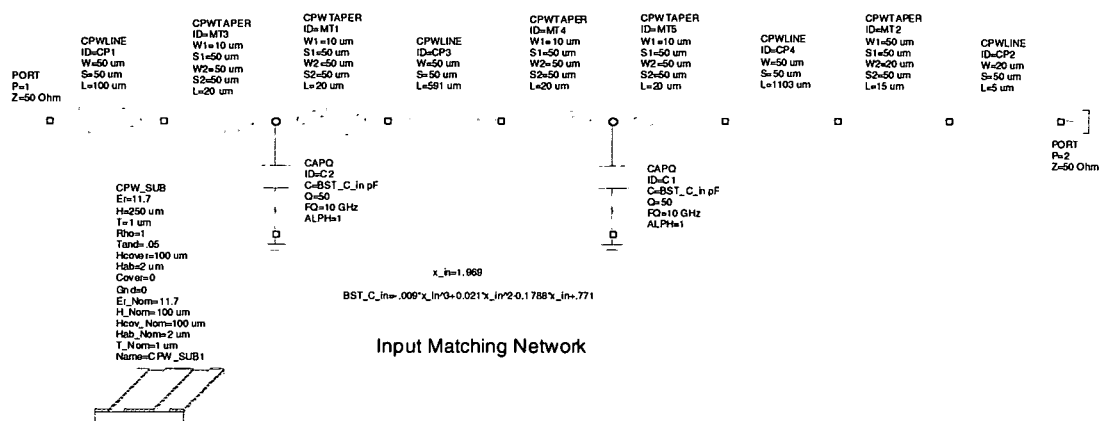


**Figure 4.11: Close-up of BST Capacitor Layout**

#### **4.4.2 Simulation of LNA Matching Networks**

In the input and the output matching networks, the ideal series inductors are replaced with CPW transmission lines. The lack of vias for the BST thin film process makes it difficult to use spiral inductors that provide larger inductance per area compared to the CPW transmission line. The spiral inductors would

require bond pads and a large surface area for wire bonding. This would introduce more losses into the LNA that could degrade the performance. Also the CPW inductive lines were optimized for 50 ohm impedance to meet the specifications for the matching networks. The figures below show the schematics for the simulation input and output matching networks with the CPW transmission lines.



**Figure 4.12: Layout and Schematic Input Matching Network**

### Output Matching Network

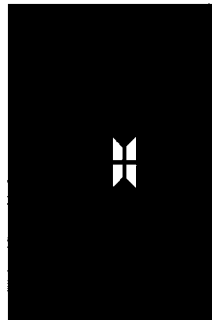
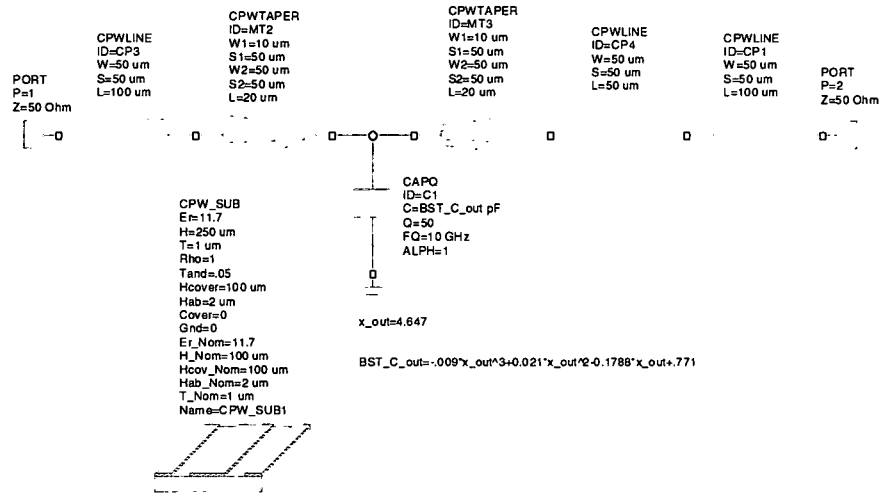
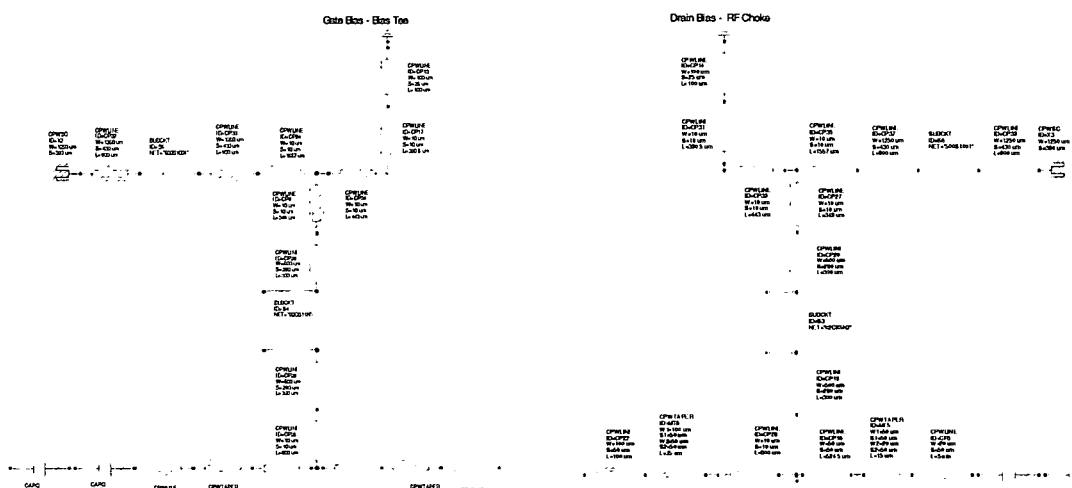


Figure 4.13: Layout and Schematic Output Matching Network

#### 4.4.3 Simulation of LNA Bias and Stability Networks

Due to the large values needed for the inductor and capacitors for the bias network, surface mount components are used in the layout. The RF choke needs an 11 nH surface mount inductor and the shunt capacitor requires a 10 pF valued chip capacitor. Since the bias network is all DC lines, the necessary pad structures for the surface mount components do not add as much loss as they would in the RF signal line. Also the DC lines do not require a 50 ohm line like

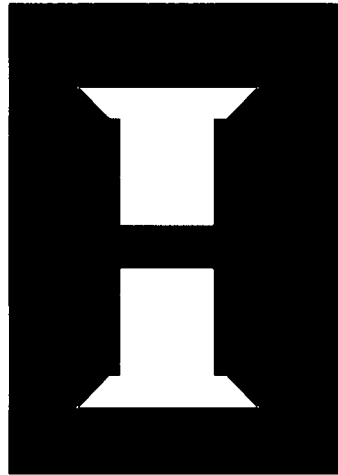
the RF signal line so the CPW transmission line width is 10  $\mu\text{m}$  instead of the 50  $\mu\text{m}$  lines. Both the gate and drain bias networks for the device are similar except they are the mirror image as shown in Figure 4.14.



**Figure 4.14: Schematic for the Gate and Drain Bias Networks**

The BST thin film DC blocking capacitor layout differs from the BST thin film capacitors used in the input and the output matching networks. In order to return to the upper metal layer, two BST thin film capacitors in series are used and act as a single DC blocking capacitor. Even though two capacitors in series equal a smaller capacitance than in parallel, the large area BST thin film capacitors biased through the RF transmission lines have a large enough capacitance for DC blocking. These capacitors also use a CPW transmission line design. Instead of being a shunt to ground, the metal 1 layer continues across under a second CPW transmission line on the metal 2 layer. Figure 4.15 shows the layout for the BST DC blocking capacitors used for the LNA design. The metal1 layer is shown in green along with the metal2 layer shown in orange.





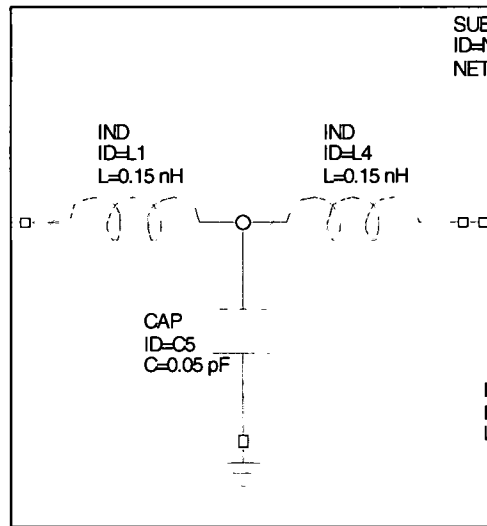
**Figure 4.15: Layout for the BST DC Blocking Capacitors**

The stability network required an inductor and a capacitor in series shunted to ground. An inductive CPW transmission line is used to generate the needed inductance value. Similar to the DC bias networks, a 5.2 pF surface mount capacitor is needed due to the large capacitance value needed for stability. This component also has a large pad structure connected to ground.

#### **4.4.4 Simulation of Transistor Mounting**

The HJ-FET device will be mounted in between the input and the output matching networks on the layout. A ground plane is placed under the mounting opening for the transistor to create a solid ground and make it easier to ground the source through wire bonding. Pads for the wire bonds are at the end of the input RF signal transmission line and at the start of the output RF signal transmission line. The wire bond pads are 100  $\mu\text{m}$  by 100  $\mu\text{m}$ . The gate and the drain of the transistor will be wire bonded to the pads on the RF signal transmission lines. Also the transistor's source will be wire bonded to the

surrounding ground plane. The bond wires used to bond the gate, source, and drain are also modeled as part of the LNA design. The bond wire model shown in Figure 4.16 accounts for approximates for 10 mils length of bond wire for connecting the transistor to the matching networks and ground.



**Figure 4.16: Bond Wiring Model for MWO**

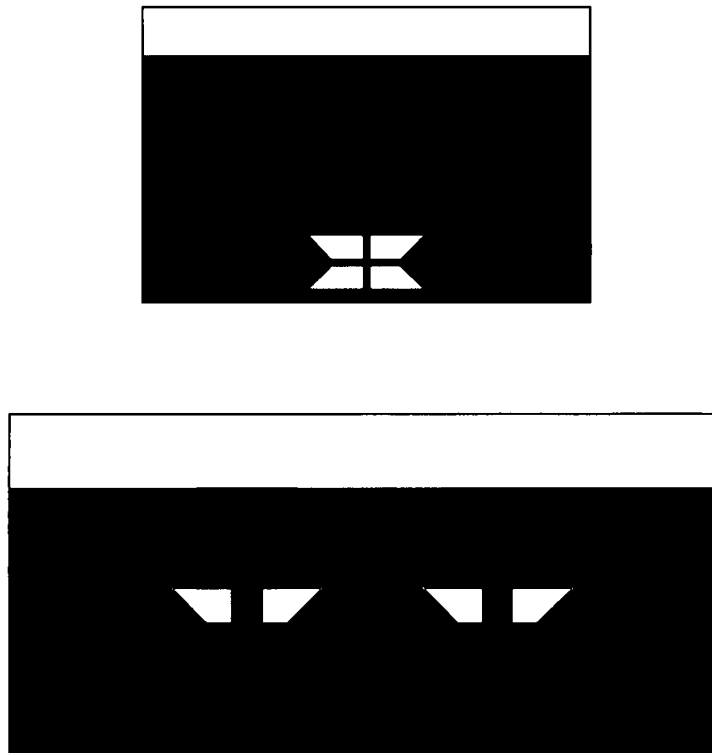
#### 4.4.5 Simulation of Surface Mount Component Mounting

Overall, surface mount components are avoided as much as possible especially for the RF signal lines due to the large pad frame associated with them. The pad structure not only consumes a large real estate area but also adds additional parasitic inductances and capacitances due to the pad structures large size compared to the 50 ohm line. This also introduces more losses and affects the matching networks for the device. However, for the bias and the stability networks, surface mount components are needed for the large values of inductance and capacitance that cannot be produced by using substrate bound elements. The pad structure for these components is modeled using very wide

CPW transmission lines and the MWO model for the components from the manufacturers.

#### **4.4.6 Simulation of Probe Pads**

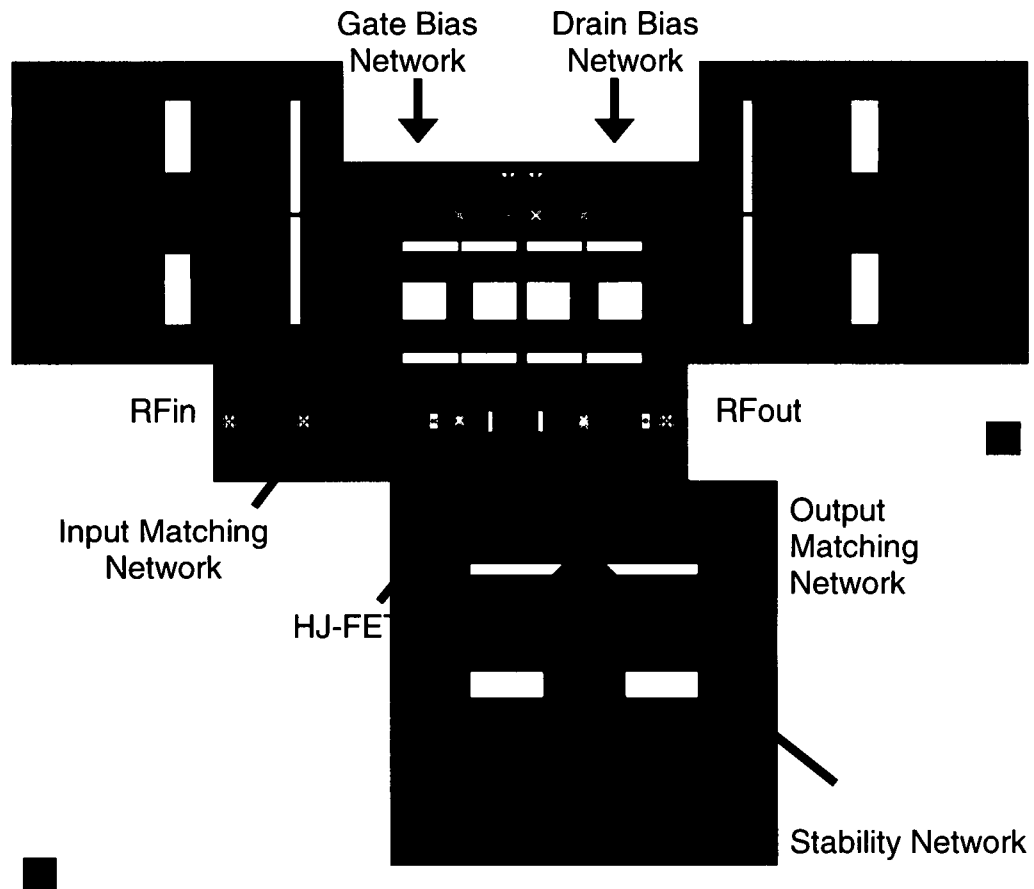
Probe pads are required to measure and bias the LNA on the wafer. The probe pad structures used for the RF signal transmission line are  $50\text{ }\mu\text{m} \times 50\text{ }\mu\text{m}$ . These pads are designed for ground-signal-ground (GSG) probes with a  $100\text{ }\mu\text{m}$  pitch. Larger pitch probes can be used due to the CPW design with the extended ground plane. The DC biasing probe pads are  $100\text{ }\mu\text{m} \times 100\text{ }\mu\text{m}$  and designed for differential ground-signal-ground-signal-ground (GSGSG) probes with a  $125\text{ }\mu\text{m}$  pitch. These pads allow for both bias networks to be probed at the same time with only one probe.



**Figure 4.17: Single-ended Probe Pad and Differential Probe Pad Layouts**

#### **4.4.7 Simulation of the LNA Layout**

Figure 4.18 shows the layout for the simulation of the LNA. The metal 1 layer is depicted in green while the metal 2 layer is depicted in orange. The space in the center is the mounting opening for the transistor. The bias networks probe pads are seen at the top of the layout. The RF signal transmission line probe pads are seen on both sides of the layout with the RF input on the left and the RF output on the right.



**Figure 4.18: LNA Layout in MWO**

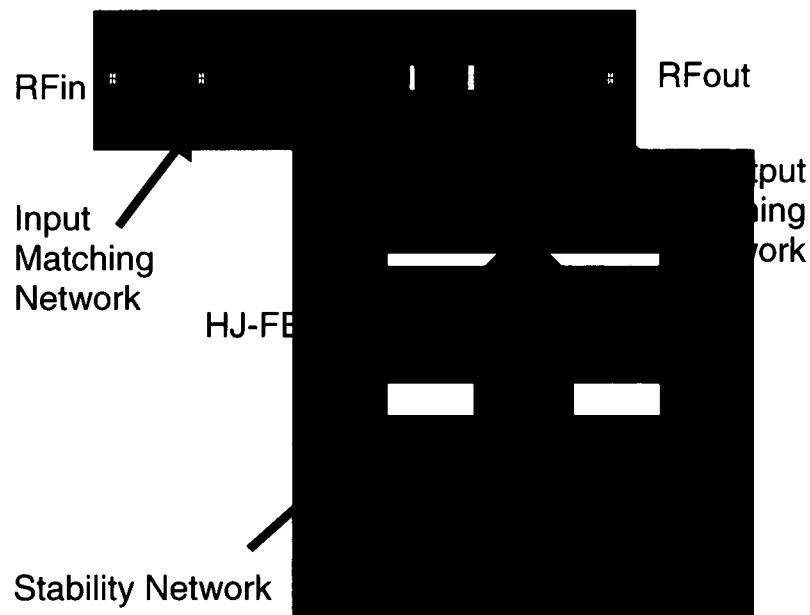
#### **4.5 Dropout Circuits**

Along with the LNA design, multiple dropout circuits are designed for debugging purposes and process verification. A simplified version of the LNA design is created for determining the effects of the bias networks and the DC capacitors on the performance. Also dropout circuits of the BST thin film capacitors are designed for measuring the available capacitances separately. The input and the output matching networks are also designed as dropout circuits to aid in verification of the tuning capabilities of the LNA. Also resonant

circuits are designed to verify the substrate definition used in MWO. These circuits are critical for the development of further iterations of the amplifier design.

#### 4.5.1 Dropout of Simplified LNA

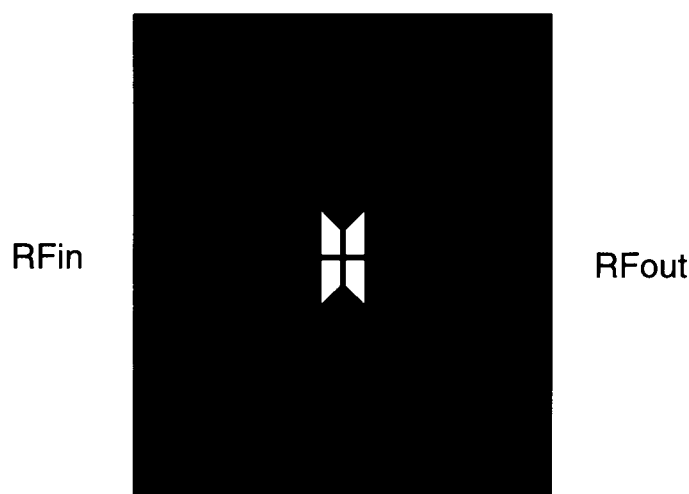
The main dropout circuit is a simplified LNA design without the gate and drain bias networks. Also the DC blocking capacitors are removed for this dropout. The purpose for this test circuit is to evaluate the effects of the bias networks on the LNA and, if necessary, to help de-bug any issues that might arise during testing of the LNA. Also this circuit can be used to test the bias of the device through the RF lines along with biasing the BST capacitors. Figure 4.19 shows the layout of the dropout LNA without bias networks.



**Figure 4.19: Dropout Circuit of the Simplified LNA Design**

### 4.5.2 Dropout of BST Thin Film Capacitors

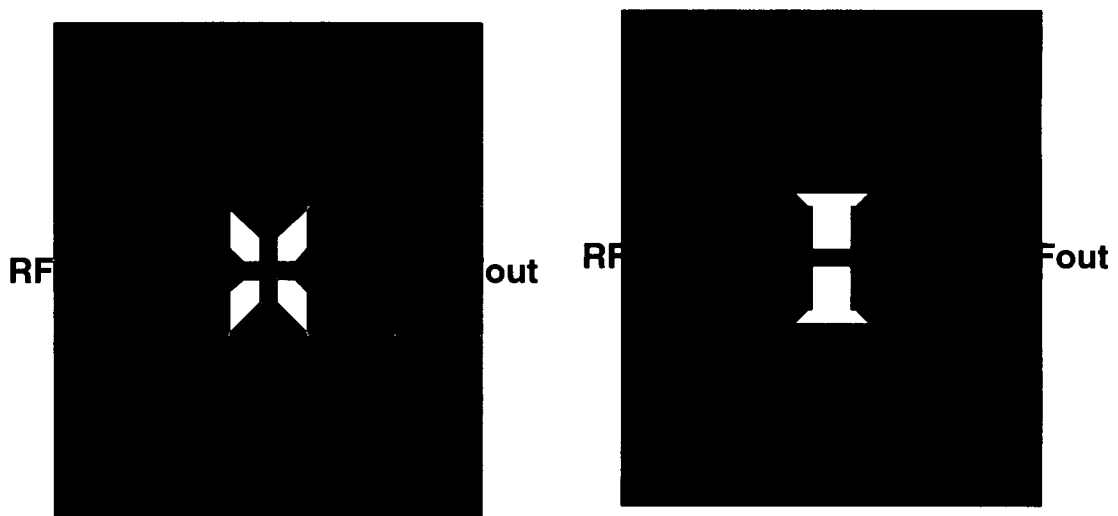
The next set of dropout circuits are the different BST capacitors. The first capacitor is the main BST capacitor used in the matching networks. It is the shunt to ground parallel plate BST capacitor used for tuning the LNA with an area of  $5\text{ }\mu\text{m} \times 5\text{ }\mu\text{m}$ . This dropout will help to verify the functionality of the capacitor layout and its modeled capacitance used in simulation. Figure 4.19 shows the dropout layout for the matching network BST capacitor.



**Figure 4.20: Dropout Circuit of the BST Capacitor**

Another BST capacitor dropout is a parallel plate shunt to ground capacitor with an area of  $20\text{ }\mu\text{m} \times 20\text{ }\mu\text{m}$ . This capacitor dropout will help to characterize the DC blocking capacitor used in the LNA layout. Since it has a larger area than the matching network BST capacitor, this dropout will be tested to verify the capacitance model equation and the loss associated with the larger

area. The last BST capacitor dropout is the actual DC blocking capacitor layout. Since this series capacitor has not been laid out using this process, a dropout is designed to help predict the characteristic of the BST capacitor in this layout and any losses associated with it in the design. As explained in Section 4.3.3, the DC blocking capacitor is comprised of two parallel plate capacitors in series due to the need to return to the upper metal layer for the RF transmission line. Also this dropout will assist in any necessary de-bugging needed for the LNA design.



**Figure 4.21: Dropout Circuit of the 20  $\mu\text{m}$  x 20  $\mu\text{m}$  Shunt and Series Capacitor, Respectively**

#### **4.5.3 Dropout of Matching Networks**

Dropout circuits are also designed for the input and output matching network. Since the matching networks use the BST capacitors and the inductive transmission lines for the series inductors, the dropout circuits aid in comparing to the simulated version of the networks. Also dropouts will be used to verify the tuning abilities of the LNA design and for any necessary debugging of the overall



design. Figure 4.22 shows the layout of the dropout circuits for both the input and output matching networks.

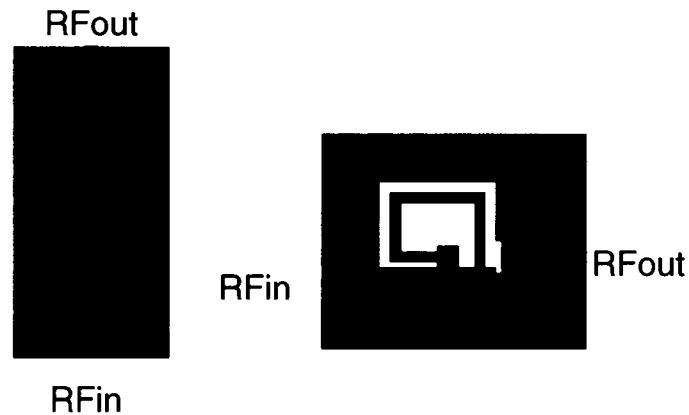


**Figure 4.22: Dropout Circuits for Input and Output Matching Networks**

#### **4.5.4 Dropout of Resonant Circuits**

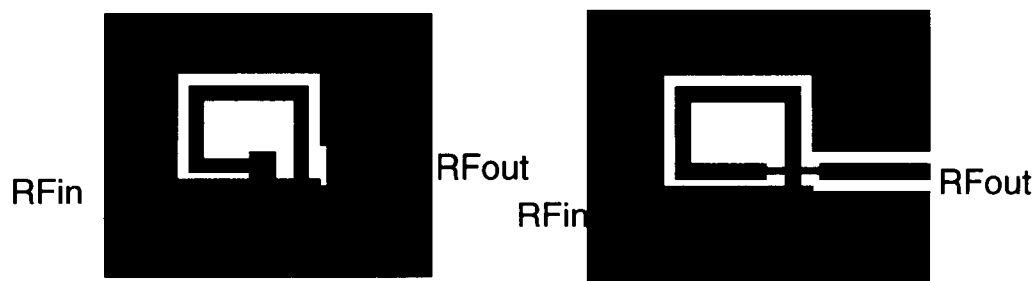
Another set of dropout circuits designed for this fabrication is for verification of the substrate definition and the fabrication process. The first circuit is a 1mm length CPW RF transmission line. This transmission line is designed to 50 ohms, the same as the transmission lines used in the LNA design. This dropout will allow for validation of the substrate definition used in MWO as well as verifying the 50 ohm impedance of the RF lines for future design iterations.

A spiral inductor with pads for wire bonding is also designed as a dropout circuit. Since there are no vias in this fabrication process, the bridge from the spiral inductor will be a wire bond connecting the RF signal lines. This will be done after the fabrication process. This dropout will help to determine if spiral inductors can be used in future design iterations and what the effects will be of the wire bond on the inductor.

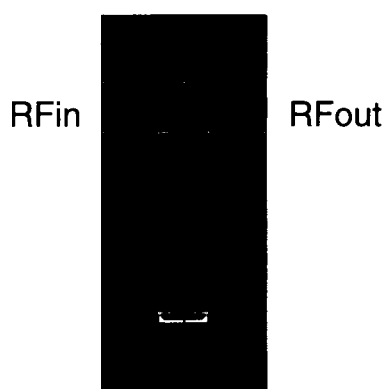


**Figure 4.23: Dropout Circuits for RF Transmission Line and Spiral Inductor**

Series and shunt resonant circuits also assist in the validation process of the substrate definition. The last set of dropout circuits fabricated includes two series resonant circuits using a spiral inductor with the BST thin film capacitor and a shunt circuit with a RF inductive line. The first series resonant circuit uses the spiral inductor with the wire bond pads in series with two series BST thin film capacitors. The bridge for the spiral inductor will be wire bonded after the fabrication process is completed. The  $5\ \mu\text{m} \times 5\ \mu\text{m}$  capacitors have the same layout as described for the parallel plate DC blocking capacitors. The second series circuit also used the spiral inductor but instead of using the wire bond technique, the two series BST thin film capacitors act as the bridge for the inductor. Both circuits can be seen in Figure 4.24 for comparison. The shunt resonant circuit uses a RF inductive line in series with a  $5\ \mu\text{m} \times 5\ \mu\text{m}$  BST capacitor shunted to ground. This circuit will also demonstrate the effects of a T-junction used in a design.



**Figure 4.24: Dropout Circuits for the Series Resonant Circuits**



**Figure 4.25: Dropout Circuit for the Shunt Resonant Circuits**

## 4.6 Experimental

The processing of the designed circuits required two mask layers (Metal1 and Metal2). Standard positive photoresist lift-off photolithography was used for both the metal1 and metal2 layers. For metal1 layer, a Ti adhesion layer (20 nm) was deposited first followed by 800 nm of gold and 200 nm of Pt in an electron-beam evaporation system. The process flow for the metal layers is given in the table below.

**Table 4.1: Lift-off Processing of Metal Layers**

No.	Process Step	Time
1	1:10 BOE:DI H <sub>2</sub> O solution (Surface SiO <sub>2</sub> etch)	30 secs
2	DI rinse wafers (3 or 4 rinses)	
3	Prebake wafers @ 110 C on the hotplate	1 min
4	Degreasing in Acetone and IPA (spin+spray)	30 Secs
5	PMGI SF-11 spin coat @4000 rpm, ramp at 200 (~1 µm thick) Remove edge-bead with nanoEBR	30 secs
6	Bake at 270 C on the hot-plate	2 mins
7	Spin-coat S1813 photoresist @4000 rpm, ramp at 200 (~2 µm) Remove edge-bead with acetone	30 secs
8	Bake at 110 C on the hot-plate	1 min
9	Align and expose in MJB3	11.5 secs
10	Develop in AZ351 developer solution followed by DI spray And blow dry in N <sub>2</sub> (examine pattern)	30 secs
11	Deep UV exposure	200 secs
12	Develop in SAL101 solution followed by DI rinse and N <sub>2</sub> blow Dry (examine pattern)	1 min
13	Plasma ash in O <sub>2</sub> plasma	4 mins
14	Pre-metal etch (BOE solution, 1:10 with DI H <sub>2</sub> O)	30 secs
15	Metallization (e-beam), Ti: 20 nm, Au: 0.8-1 µm, Pt:0.2 um	
16	Lift-off step 1: Soak in acetone for ~ 5 mins. Spin+spray acetone, followed by IPA to remove residue (examine pattern)	
17	Lift-off step 2: Soak in 1165 solution @ 90C	2 mins
18	DI rinse in the rinse station, blow dry in N <sub>2</sub> (examine pattern)	4 cycles
19	Plasma Ash in oxygen plasma	4 mins
20	Examine pattern under the microscope	

After the metal1 layer was defined, the Ba<sub>0.6</sub>Sr<sub>0.4</sub>TiO<sub>3</sub> thin-film was deposited on the entire surface in a process controlled pulsed laser deposition (PLD) system. Neocera PLD system with a capability to deposit on 4" wafers was utilized for the deposition of the BST thin film. BST film was processed at 75 mT oxygen partial pressure at a substrate temperature of approximately 840 C. The fabrication process for the nano-structured BST thin-films is described elsewhere [12]. After the BST deposition, the metal2 layer was defined and

processed using the same lift-off technique as in the table, except for the change in the metal layers to 200Å of Ti, 2000 Å of Pt, and 8000 Å of Au. The devices are ready for testing after the completion of the metal<sub>2</sub> layer. The varactor shunt switches were tested using a HP 8510/8720 Vector Network Analyzer (VNA). First, a Line-Reflect-Reflect-Match (LRRM) calibration was done over a wide frequency range (1 to 20 GHz). The sample was probed using standard GSG probes, with the dc bias applied through the bias tee of the VNA to the probe.

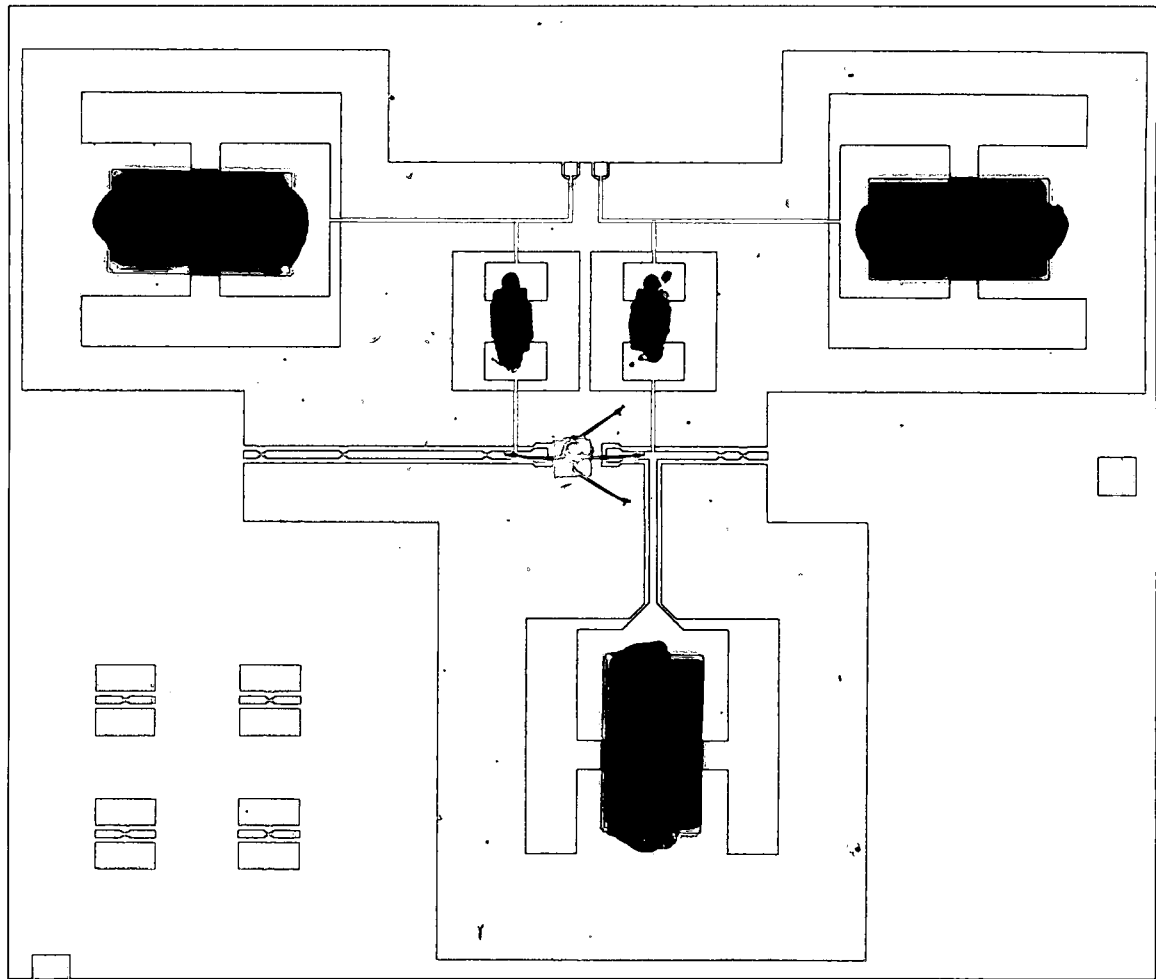
After the LNA is fabricated, the transistor and the surface mount components need to be mounted. The transistor will be attached on the LNA on the mounting opening by a conductive epoxy. Wire bonds will connect the gate and drain to the RF signal transmission lines as well as the source to the surrounding ground plane. The surface mount inductors and capacitors for the bias and the stability networks of the LNA will be mounted with conductive epoxy onto the pad frame for the components.

Additional packaging is also required for some of the dropout components as well. The simplified LNA dropout circuit will have the surface mount capacitor soldered onto its pad frame as well as having the transistor mounted and wire bonded like the LNA design. Also the spiral inductor and the series resonant circuit with the spiral inductor will have the bridge wired bonded at the wire bond pads. After this packaging is completed, the dropout circuits can also be measured.

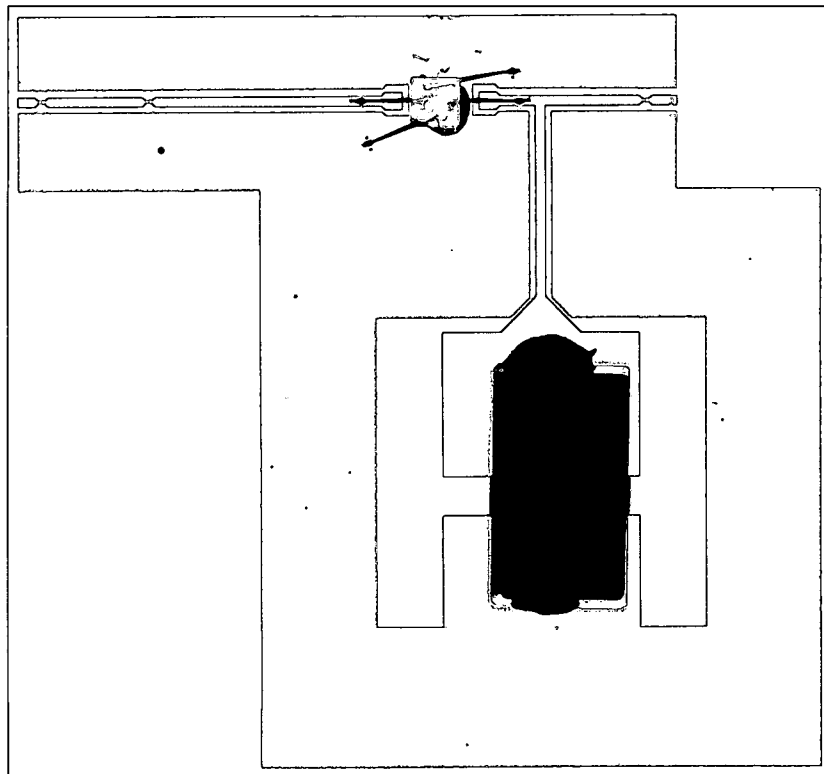
Photographs from processed wafers are shown in the figures below.

Figure 4.26 shows the fabricated LNA and Figure 4.27 shows the simple LNA on

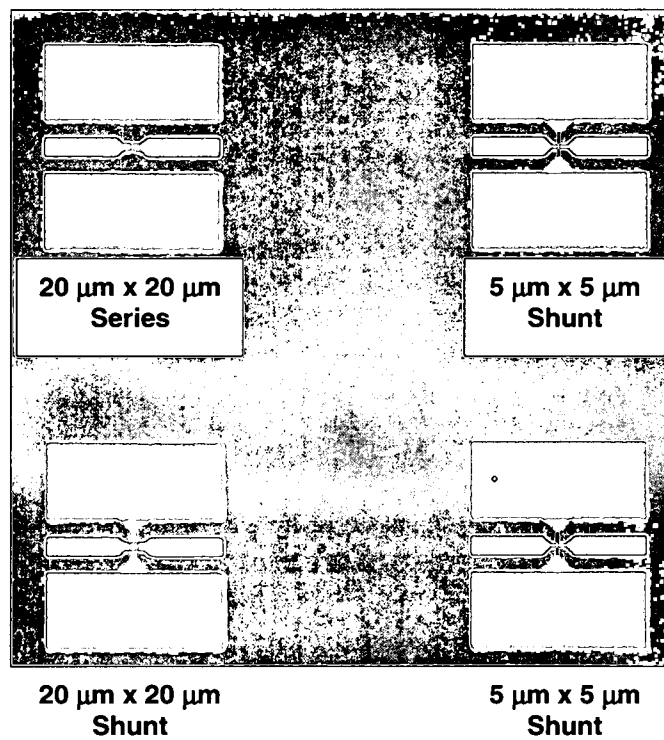
the processed wafer. The dropout circuits of the BST thin film capacitors are shown in Figure 4.28. Figure 4.29 shows the dropout circuits of the input and the output matching network on the wafer. The spiral inductor dropout circuit and the shunt resonant dropout circuit are shown in Figure 4.30 and the series resonant dropout circuits are shown in Figure 4.31.



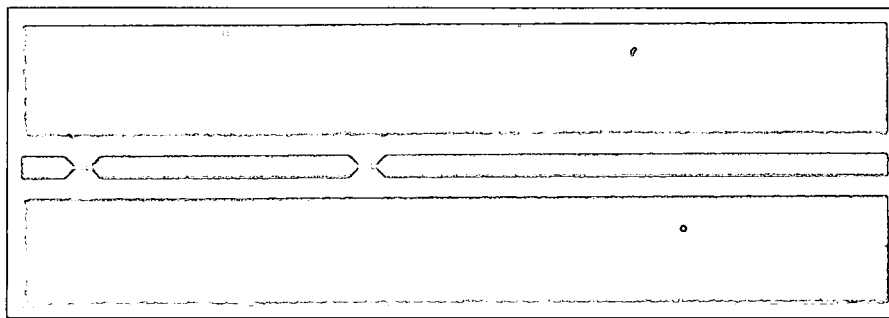
**Figure 4.26: Photograph of the LNA**



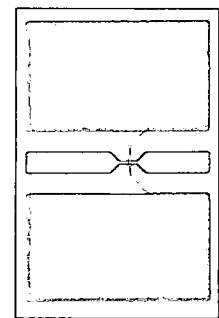
**Figure 4.27: Photograph of the Simple LNA Dropout Circuit**



**Figure 4.28: Photograph of the BST Thin Film Capacitor Dropout Circuits**

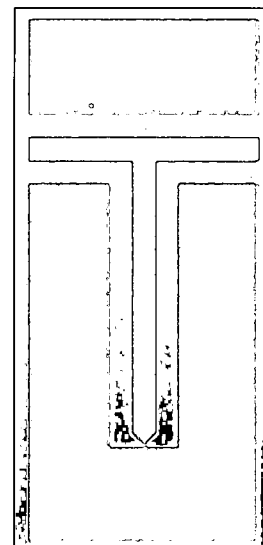
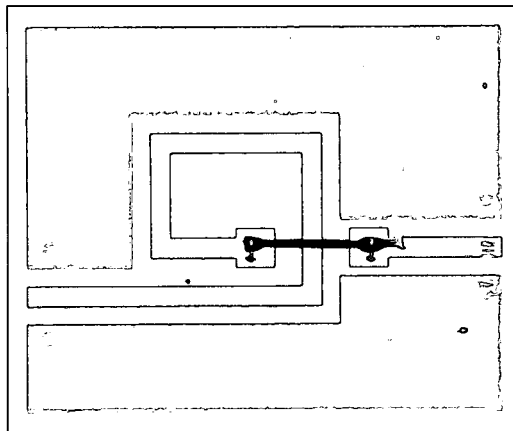


**Input Matching Network**

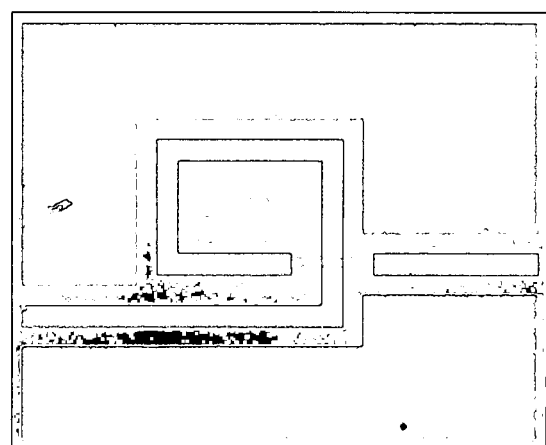
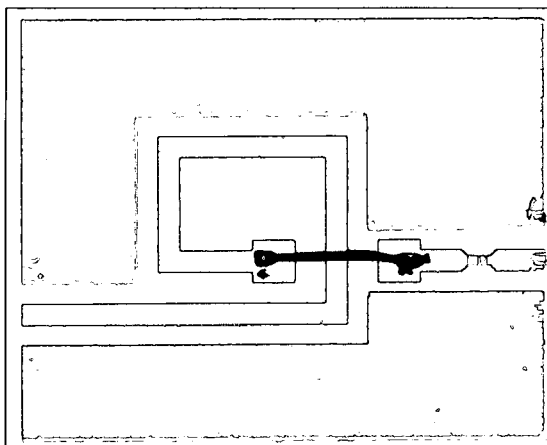


**Output Matching Network**

**Figure 4.29: Photograph of the Matching Network Dropout Circuits**



**Figure 4.30: Photograph of the Spiral Inductor and Shunt Resonant Dropout Circuits**



**Figure 4.31: Photograph of the Series Resonant Dropout Circuits**



To test the functionality of the LNA design, S-parameters for the LNA will be measured from 0 – 20 GHz with a fixed input bias of 1.97 V and a fixed output bias of 4.65 V. Then the S-parameters will be measured from 0 – 20 GHz with a varying input and output bias voltages ranging from 0-5V to test the tuning capabilities of the LNA design. Noise measurements will be taken from 0 – 20 GHz to measure the noise figure of the LNA design. S-parameters of the dropout circuits will be measured from 0 – 20 GHz to assist in the verification and the debugging process of the LNA.

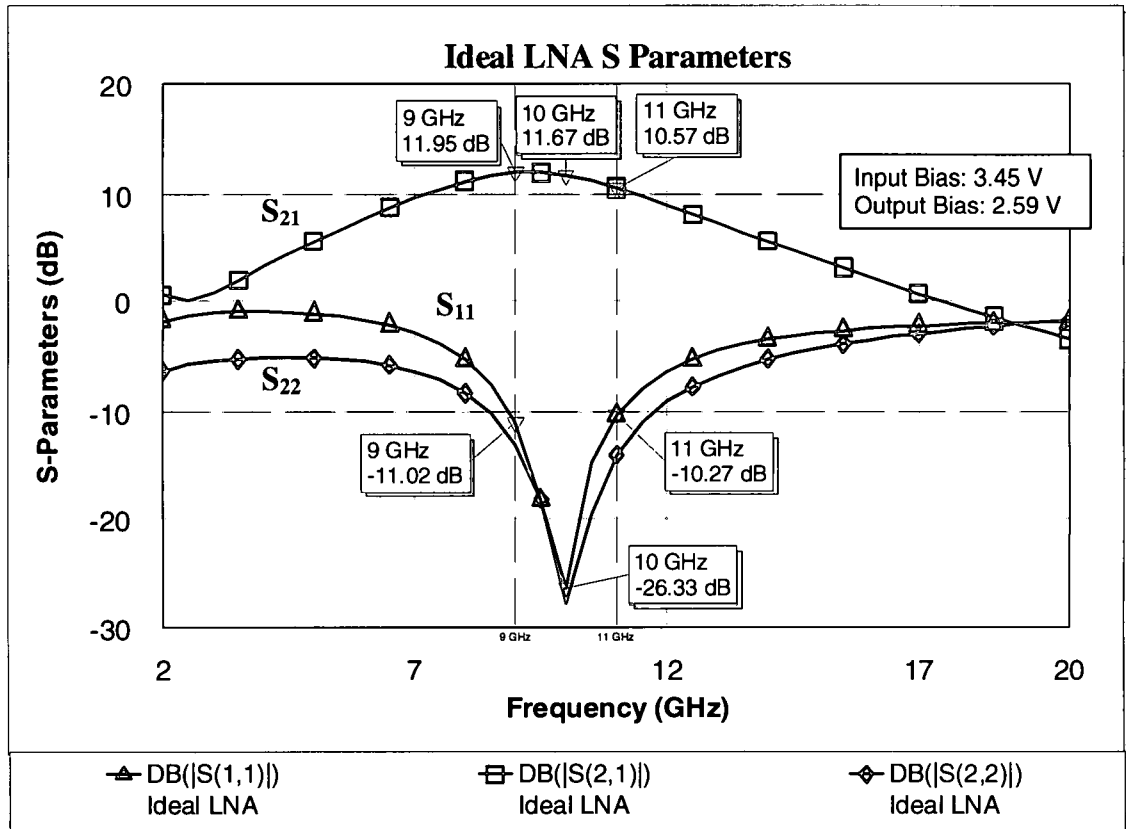
## **CHAPTER V**

### **Results and Discussion**

The simulated results of the ideal and simulated LNA are discussed in this chapter. Also the simulations of the dropout circuits are reviewed. A comparison of the ideal and the simulated LNA is also contained in this chapter. Preliminary experimental results are also presented on the dropout circuits, including the simple LNA circuit.

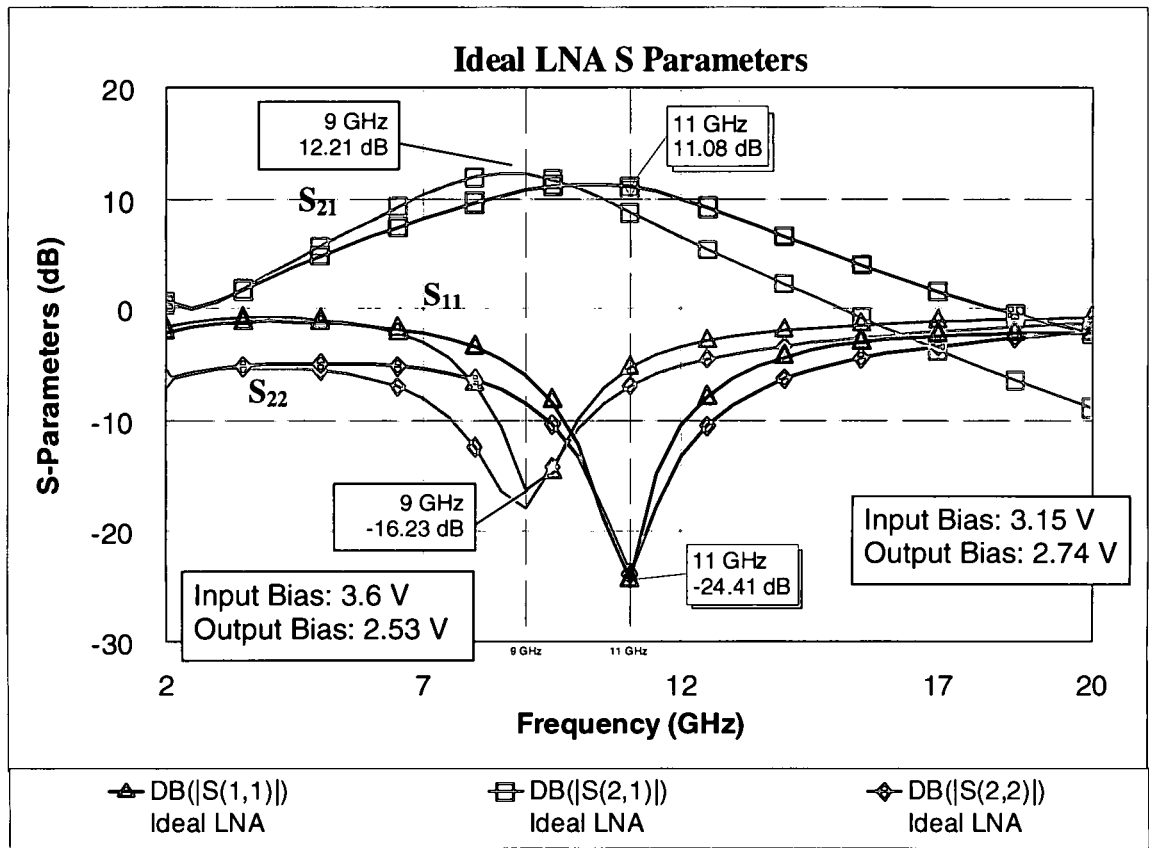
#### **5.1 Ideal Lumped Element LNA Design**

The ideal LNA schematic is optimized to meet the design specifications for this project. At the center frequency 10 GHz, the ideal LNA has a gain of 11.37 dB and an instantaneous bandwidth of 2 GHz. This bandwidth is much greater than the desired 1 GHz bandwidth in the specifications. The input bias for the BST thin film capacitors is 3.45 V and the output bias for the BST thin film capacitor is 2.59 V. Figure 5.1 shows the S-parameter simulation of the ideal LNA design.



**Figure 5.1: Ideal LNA S-Parameter Plot**

The tunability results for the ideal LNA is simulated for the desired frequency range of 9-11 GHz. The tunable LNA must maintain a minimum loss of gain when shifting the frequency and continue to have a noise figure of less than 3 dB. Figure 5.2 shows the tuning range of the ideal LNA with the tunable BST thin film capacitors as well as the necessary bias voltage for the capacitors. The center frequency is tuned from 9 GHz to 11 GHz with the less than 0.5 dB drop in the gain.



**Figure 5.2: Ideal LNA S-Parameter Plot Showing Tuning Range**

The overall noise figure of the ideal LNA is well below the desired valued of 3 dB. The ideal LNA has a simulated noise figure of 1.4 dB at 10 GHz. This is very close to the transistor minimum noise figure value which indicates optimal matching conditions is achieved for low noise performance. Also the ideal LNA is unconditionally stable with a stability factor greater than 1 over the entire simulated frequency range from 0 – 20 GHz. Figure 5.3 shows the noise figure and Figure 5.4 shows the stability simulations for the ideal LNA.

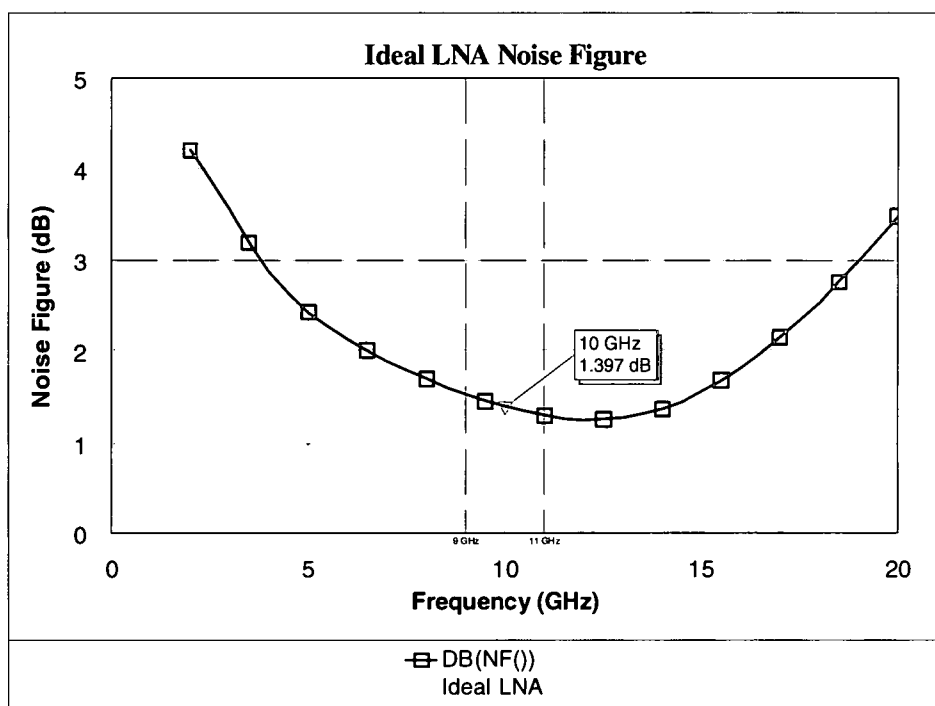


Figure 5.3: Ideal LNA Noise Figure Plot

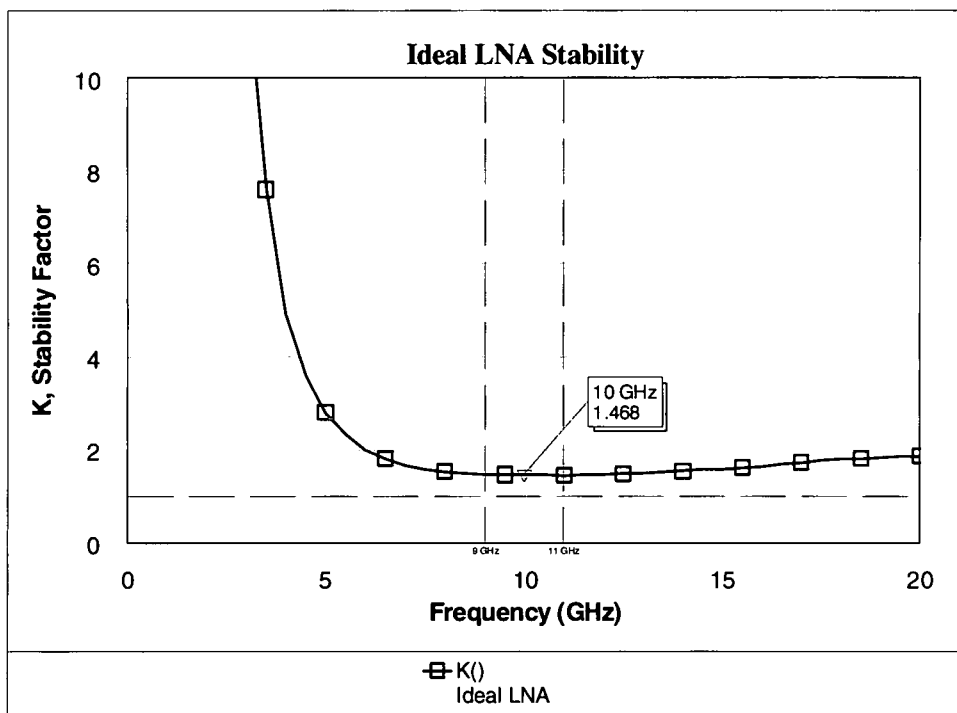
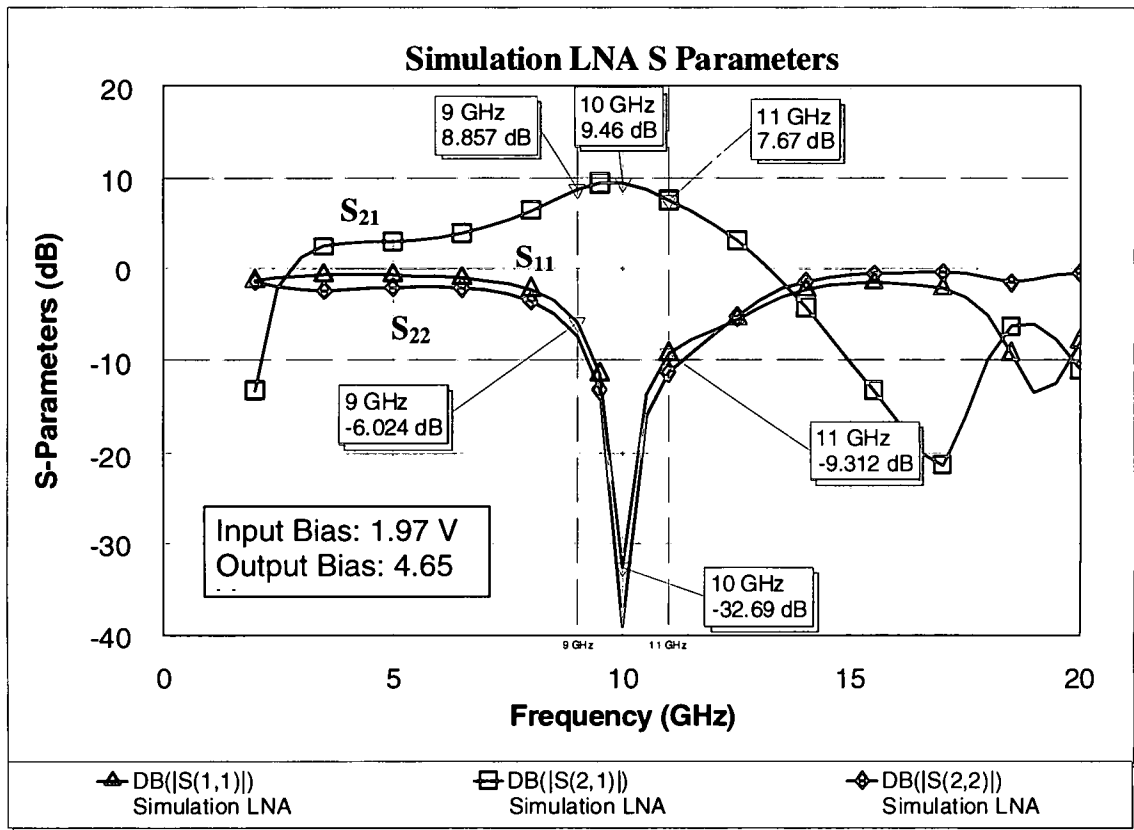


Figure 5.4: Ideal LNA Stability Plot

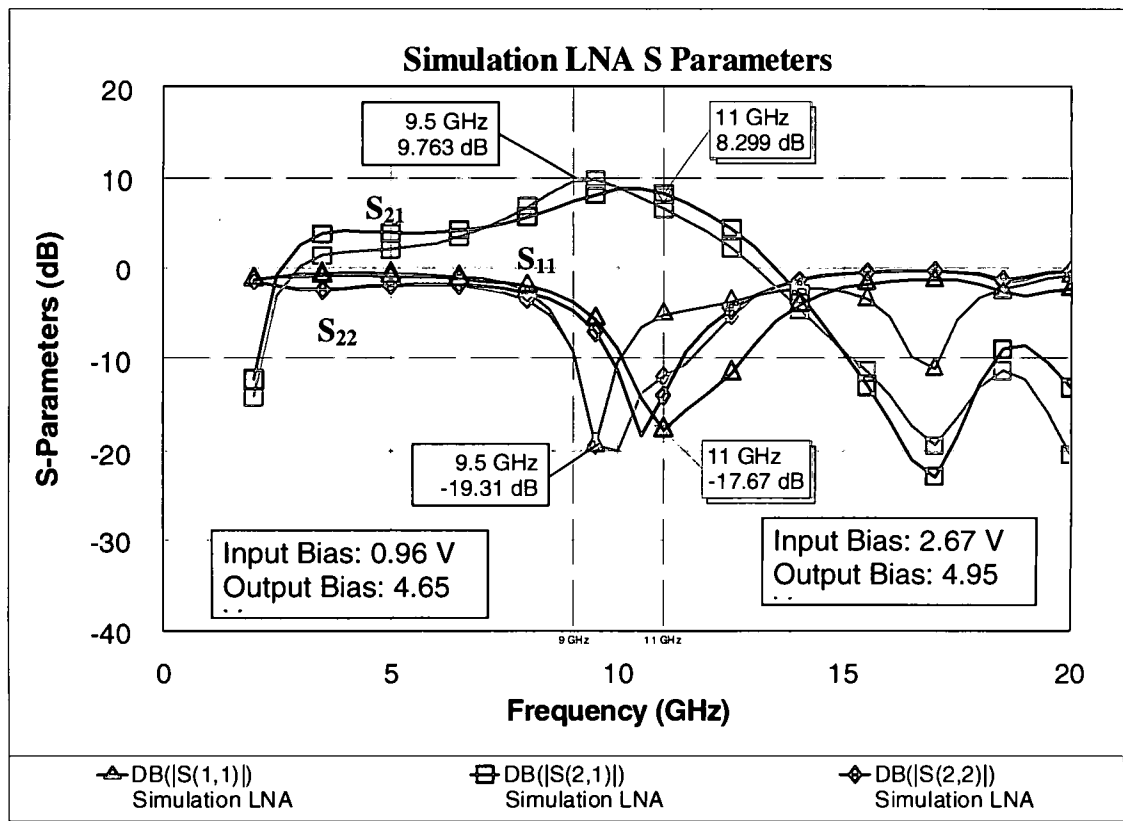
## 5.2 LNA Simulation Results

The simulation of the layout schematic using the models from MWO demonstrates the effects of the real components models compared to the ideal elements. Some re-optimization was needed to re-tune the LNA to meet the requirement specifications. The S-parameters are plotted and show a slight degradation in the gain and bandwidth. The gain at 10 GHz is 9.46 dB and the bandwidth is 1.1 GHz. The gain is still very close to meeting the desired design specifications while the bandwidth is still greater than the design specifications. The input bias for the BST thin film capacitors is 1.97 V and the output bias for the BST thin film capacitor is 4.65 V. Figure 5.5 shows the S-parameter plot of the simulation LNA design.



**Figure 5.5: Simulated LNA S-Parameters Plot**

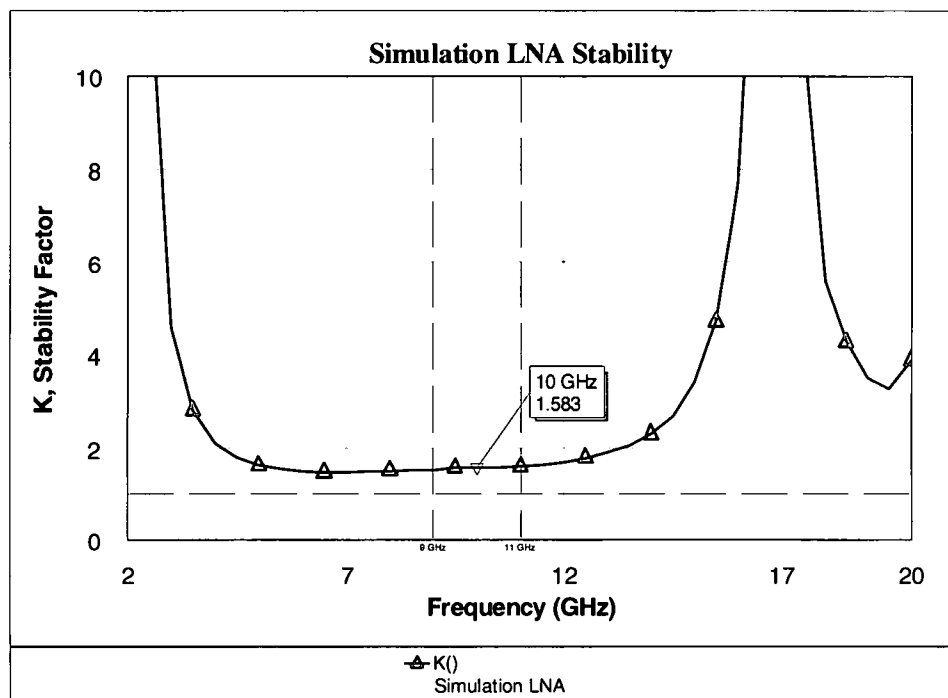
The tuning range for the LNA is maintained between 9.5 GHz and 11 GHz. There is a slight loss in gain and bandwidth during tuning but overall the tuning capability is preserved. The center frequency tuning range is shown in Figure 5.6 below.



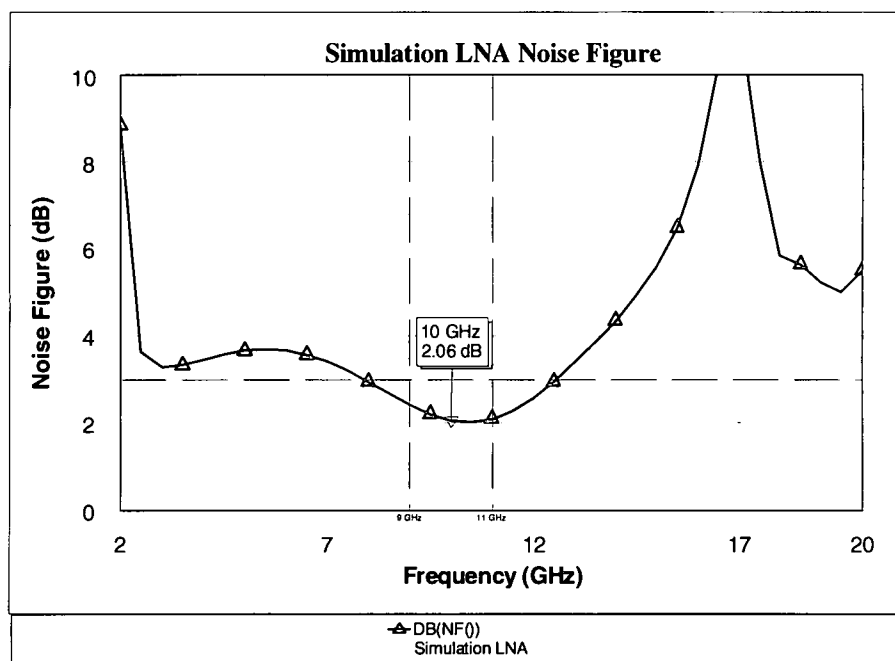
**Figure 5.6: Simulated LNA S-Parameters Plot Showing Tuning Range**

The simulation LNA design is still unconditionally stable like the ideal LNA with a K factor greater than one over the entire frequency range. Also the noise figure increased by 1.34 dB, but still meets the design specifications for the LNA. The noise figure for the simulation LNA is 2.04 dB. Figure 5.7 shows the stability plot and Figure 5.8 shows the noise figure plot for the LNA final design.





**Figure 5.7: Simulated LNA Stability Plot**



**Figure 5.8: Simulated LNA Noise Figure Plot**

Table 5.1 compares the design specifications to the simulation LNA values when tuned to 10 GHz. Overall the LNA's predicted results compare closely to the desired requirements. The bandwidth and the tuning range are maintained along with the noise figure. The gain is only 0.54 dB below the design specification with the fixed bias voltage for the BST thin film capacitors. The simulated results for 9 GHz and 11 GHz

**Table 5.1: Comparison of Design Objectives and Predicted Results**

Requirement	Specification	Simulation (10 GHz)	Units
Input Type	Single-Ended	Single-Ended	-
Input Return Loss	-10	32.69	dB
Output Type	Single-Ended	Single-Ended	-
Output Return Loss	-10	-39.1	dB
Tuning Range	9 - 11	9.4 - 11	GHz
Bandwidth	1	1.1	GHz
Small Signal Gain	10	9.46	dB
Noise Figure	< 3	2.06	dB
Input BST Bias	<10	1.97	V
Output BST Bias	<10	4.65	V

### 5.3 Dropout Circuits Results

The de-bugging process and the verification of the LNA tunability rely on the results of the dropout circuits. These circuits assist in locating any issues or determining where problems occur during testing of the LNA. Also the resonant circuits are needed to verify the substrate definition used in the simulation process as well as characterization of the passive components.

### 5.3.1 Dropout of Simplified LNA Results

A simplified LNA design without the bias networks and without the DC blocking capacitors was measured to determine the effects of the impedance matching networks on the performance of the LNA. Figure 5.9 shows the measured results of the simplified LNA design dropout circuit. The gain for the dropout is 4.65 dB at 10 GHz with  $V_{DS} = 2$  V and  $V_{GS} = -0.5$  V with an  $I_{DS} = 10.6$  mA. The simplified LNA has a drop in the gain because the matching networks are no longer being biased at the optimized voltage for the BST thin film capacitors. Also the  $S_{22}$  shifted away from the resonance at the center frequency of 10 GHz. This circuit will also assist in the de-bugging process for overall LNA if necessary.

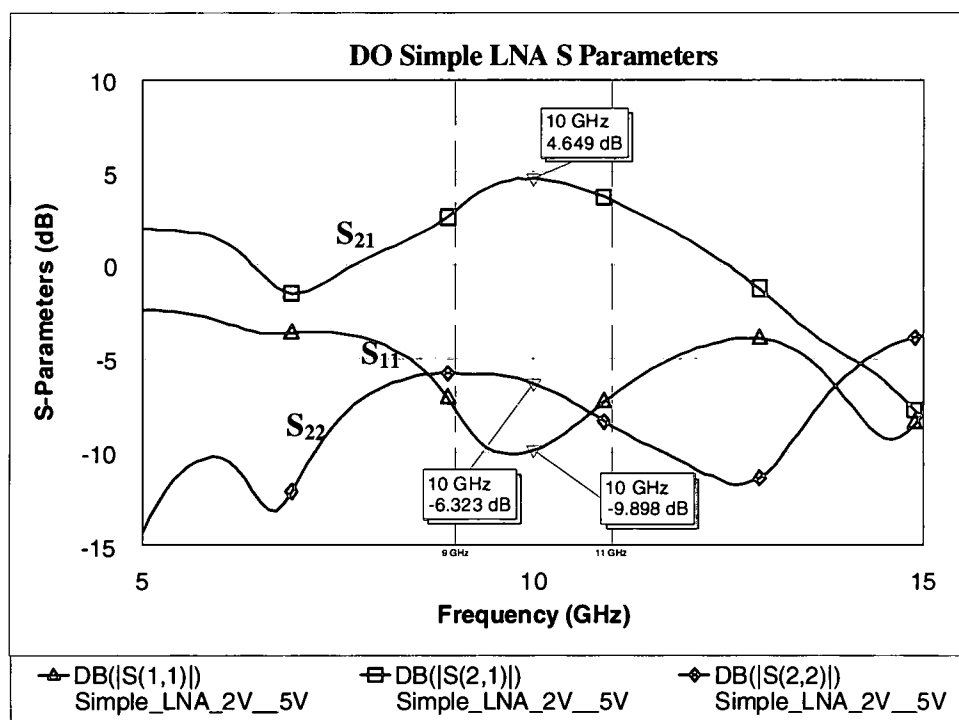
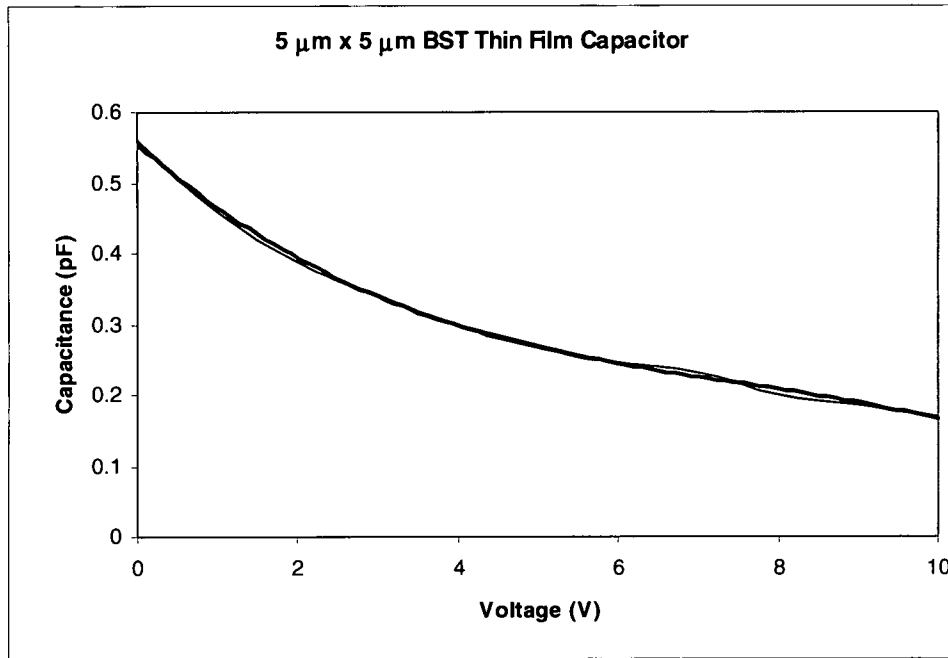


Figure 5.9: Simplified LNA Dropout Circuit S-Parameter Plot

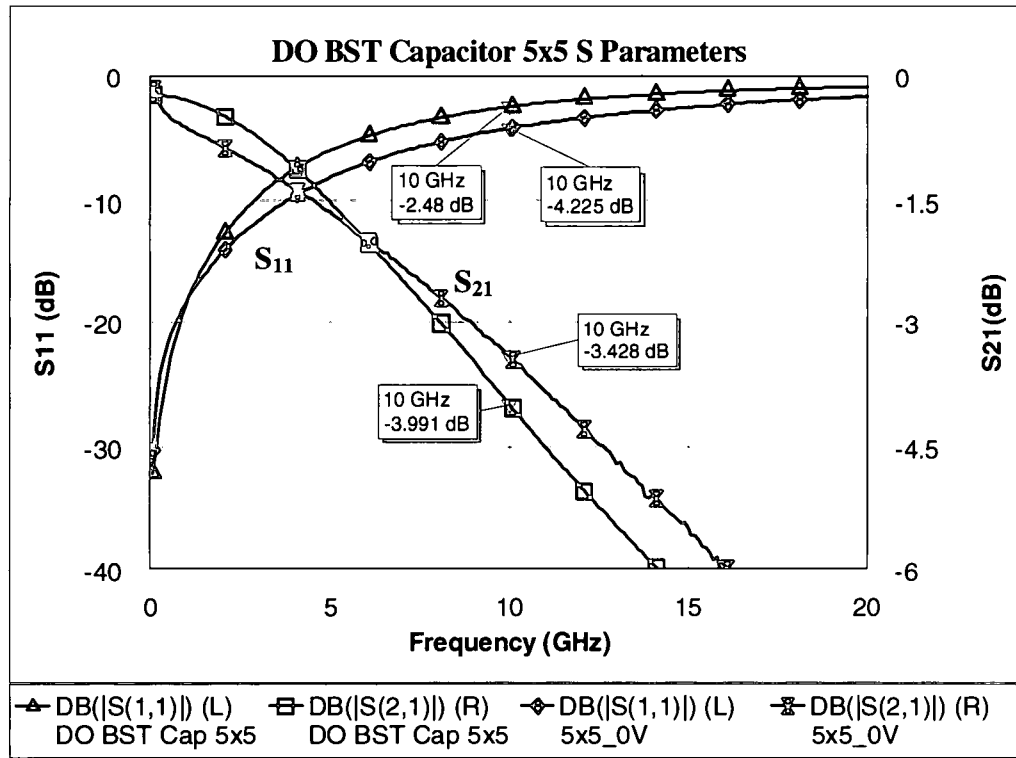
### 5.3.2 Dropouts of BST Thin Film Capacitors Results

The first BST thin film capacitor dropout is a shunt capacitor with a  $5\text{ }\mu\text{m}$  by  $5\text{ }\mu\text{m}$  surface area used for the matching networks. Figure 5.10 shows the capacitance as a function of voltage. The equivalent capacitance equation was derived from a best fit line for the nonlinear capacitance. This capacitance equation is different from the one used for the simulations and can be seen in Equation 5.1. The S-parameters for the simulated BST thin film capacitor are compared to the measured data at a 0 V bias in Figure 5.11. The simulation is reasonably close to matching the measured data for the capacitor.



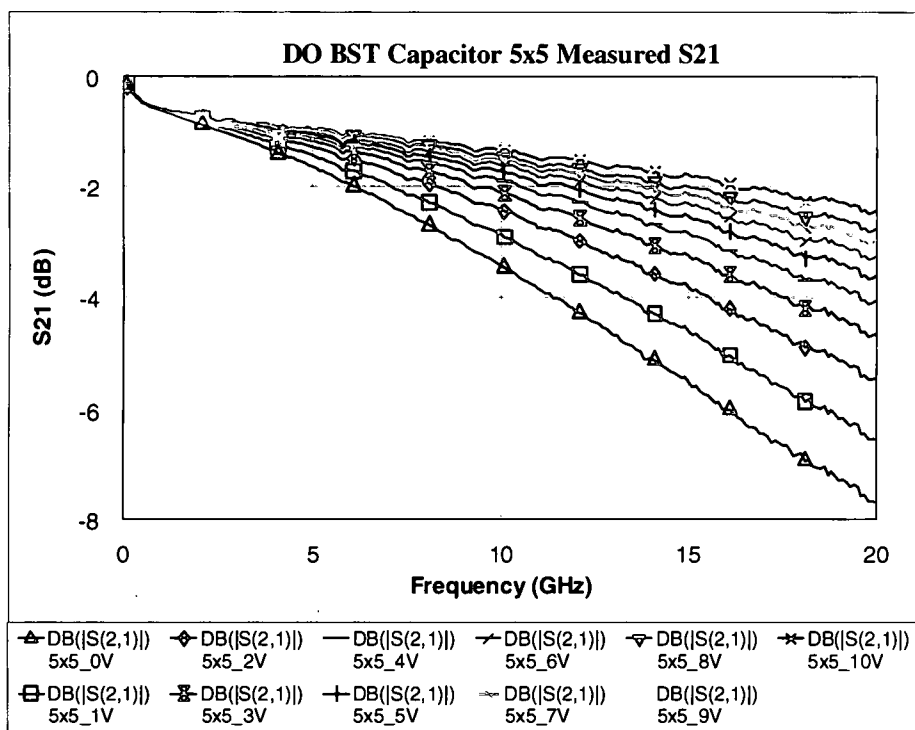
**Figure 5.10: BST Thin Film  $5\text{ }\mu\text{m} \times 5\text{ }\mu\text{m}$  Measured Nonlinear Capacitance**

$$C(V) = -0.0005V^3 + 0.011V^2 - 0.1013V + 0.5556 \quad (5.1)$$

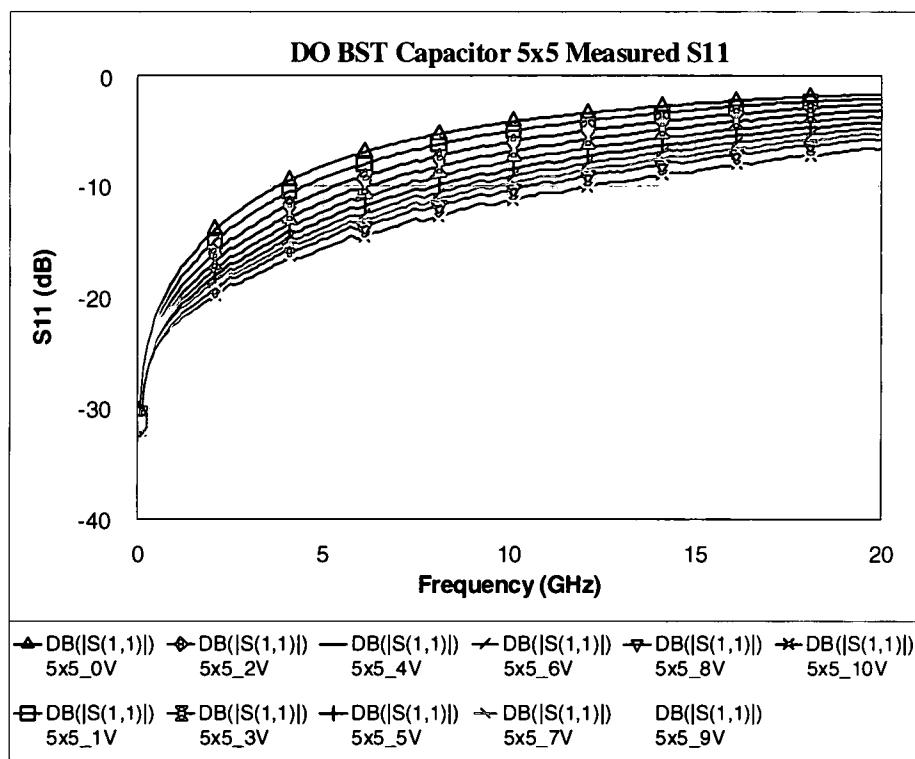


**Figure 5.11: BST Thin Film 5  $\mu$ m x 5  $\mu$ m Capacitor Dropout S-Parameters Comparison**

The shunt capacitor acts as a simple lowpass filter. Figure 5.12 and Figure 5.13 show the measurements of the insertion loss and the return loss for the 5  $\mu$ m x 5  $\mu$ m BST capacitor as the voltage is varied in 1 V steps from 0 V to 10 V. The higher bias voltage lowers the dielectric constant of the BST thin film and therefore has a lower capacitance value. This explains the shifts in the S-parameter plot as the bias voltage is increased.

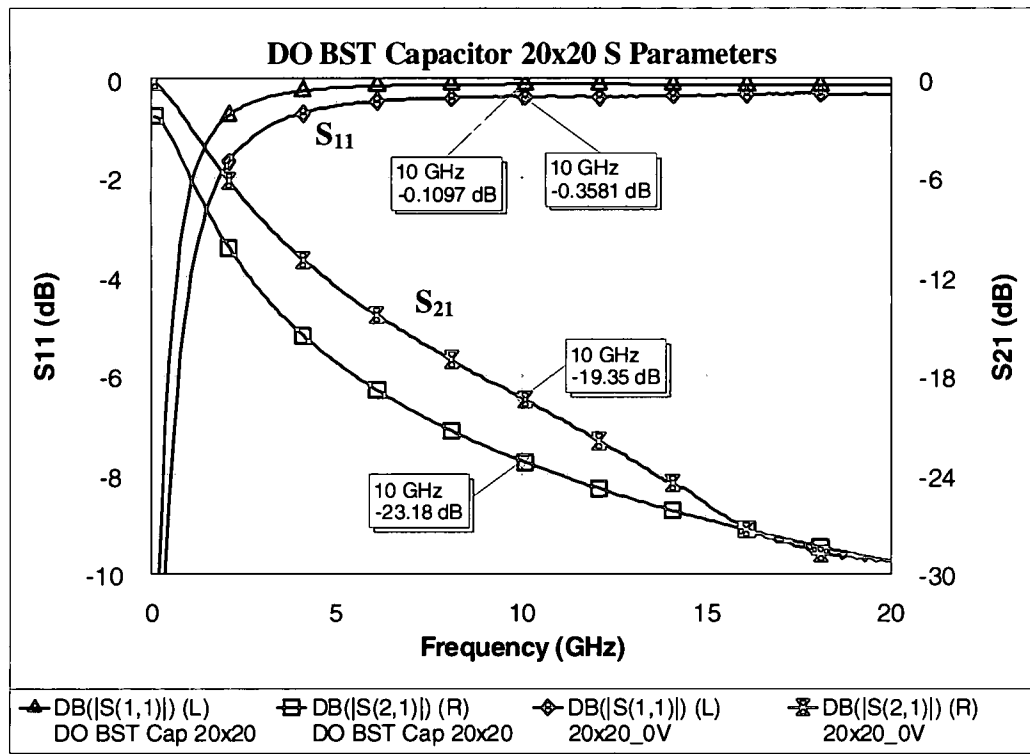


**Figure 5.12: Measured Insertion Loss for the BST Thin Film 5  $\mu\text{m}$  x 5  $\mu\text{m}$  Capacitor**



**Figure 5.13: Measured Return Loss for the BST Thin Film 5  $\mu\text{m}$  x 5  $\mu\text{m}$  Capacitor**

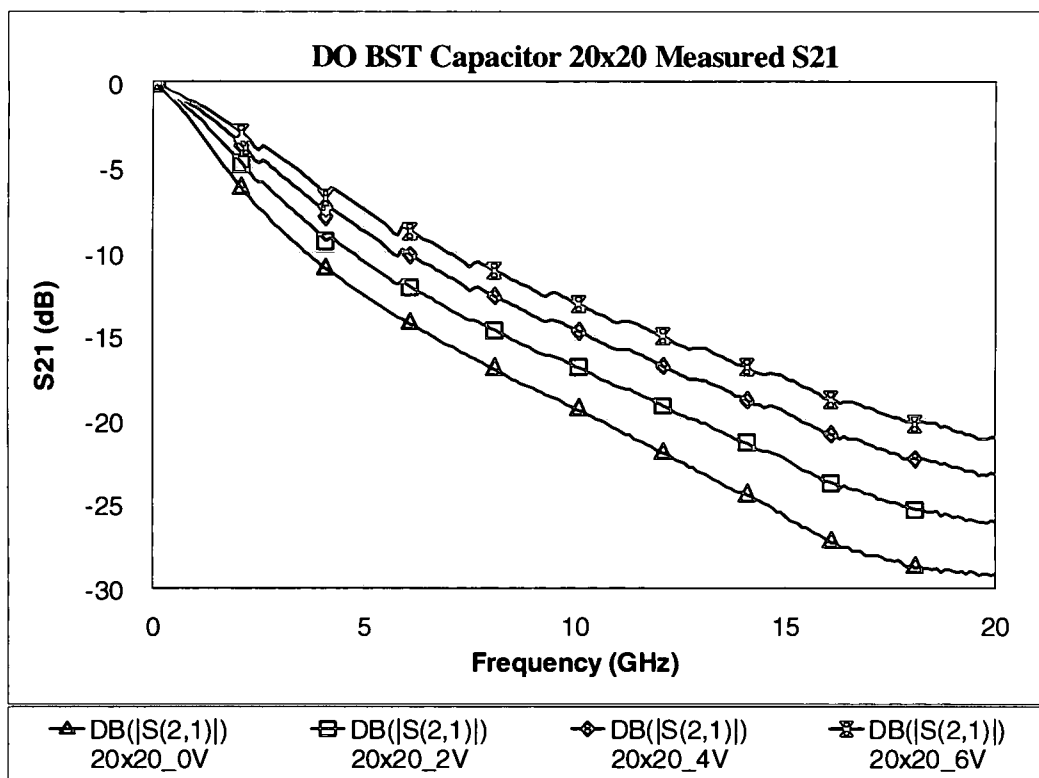
A 20  $\mu\text{m}$  x 20  $\mu\text{m}$  surface area BST thin film capacitor is simulated to assist in characterizing the DC blocking capacitors. Figure 5.14 shows the S-parameter comparison of the measured data to the simulation for this capacitor with the bias voltage equal to 0 V. The measured magnitude of  $S_{11}$  is very close to the simulation with only a 0.2 dB difference. There is a slight magnitude variation in the magnitude of the  $S_{21}$  between the measured and the simulated data.



**Figure 5.14: BST Thin Film 20  $\mu\text{m}$  x 20  $\mu\text{m}$  Capacitor Dropout S-Parameters Comparison**

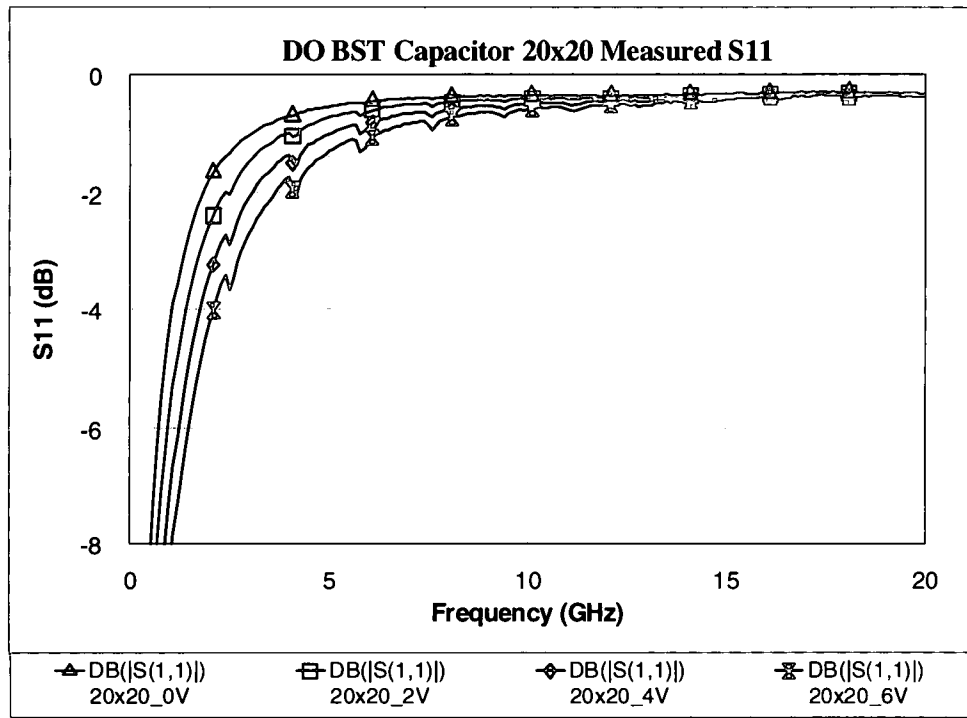
Similar to the smaller area capacitor, the 20  $\mu\text{m}$  x 20  $\mu\text{m}$  BST thin film capacitor also acts like a simple lowpass filter. The larger surface of this capacitor relates to a larger available capacitance value. Figure 5.15 and Figure

5.16 show the measured return loss and the insertion loss as the bias voltage is varied from 0 V to 6 V in 2 V intervals.



**Figure 5.15: Measured Insertion Loss for the BST Thin Film 20  $\mu\text{m}$  x 20  $\mu\text{m}$  Capacitor**





**Figure 5.16: Measured Return Loss for the BST Thin Film 20  $\mu\text{m}$  x 20  $\mu\text{m}$  Capacitor**

The next dropout circuit is the BST thin film DC blocking capacitor. Since this is the first design iteration with series capacitors in this fabrication process, this dropout is critical for characterizing the DC blocking capacitor and verifying the model used for this capacitor. Figure 5.17 shows the comparison of the simulated S-parameters and the measured data for the BST thin film DC blocking capacitor with the bias voltage at 0 V. The magnitude for the measured data is shifted compared to the simulated but the resonance was not affected. This means that the model for the series BST DC blocking capacitor needs to be re-optimized to closer reflect the measured data.

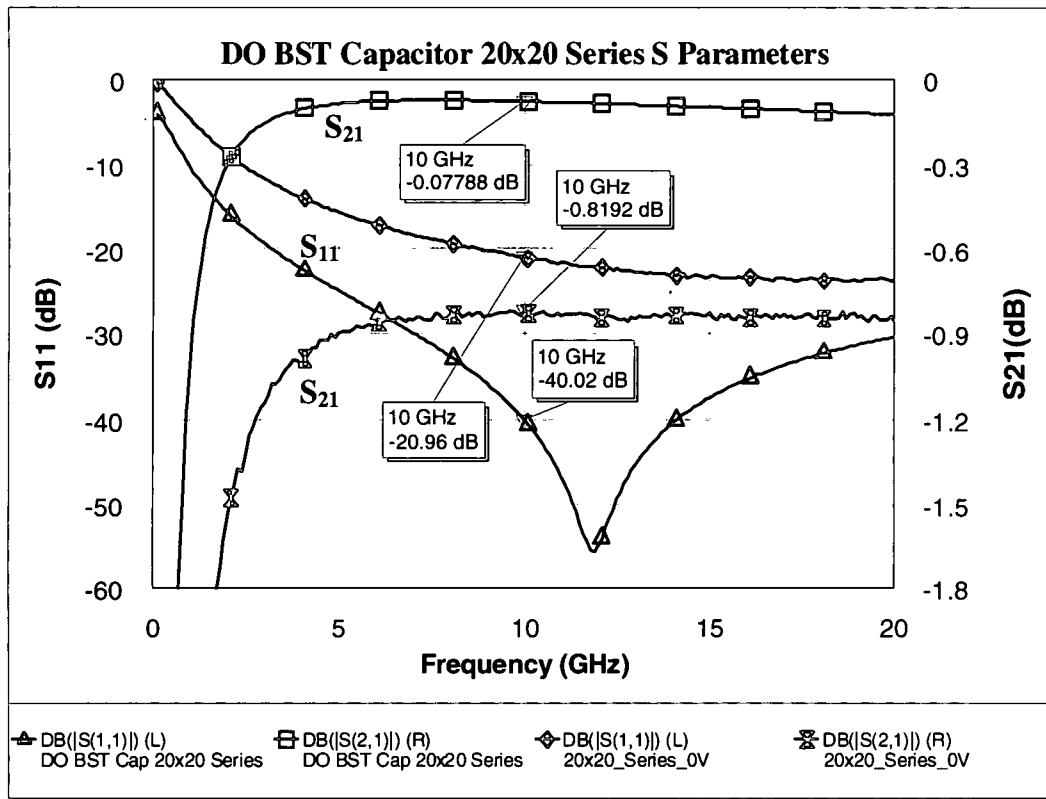
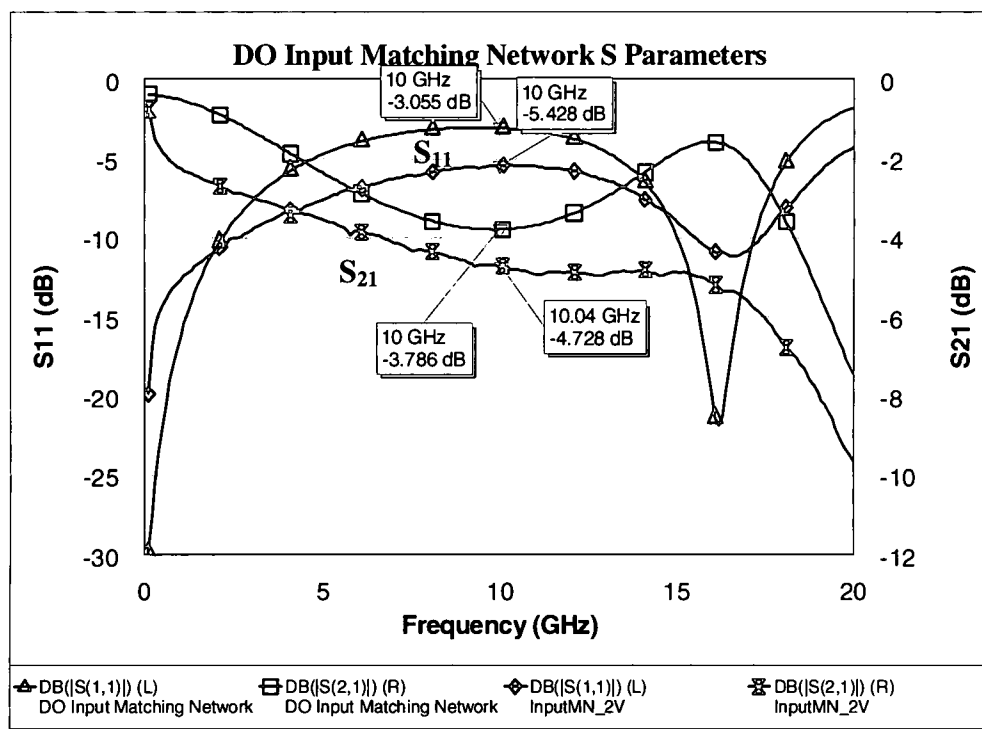


Figure 5.17: BST 20  $\mu\text{m}$  x 20  $\mu\text{m}$  DC Blocking Capacitor S-Parameters Comparison

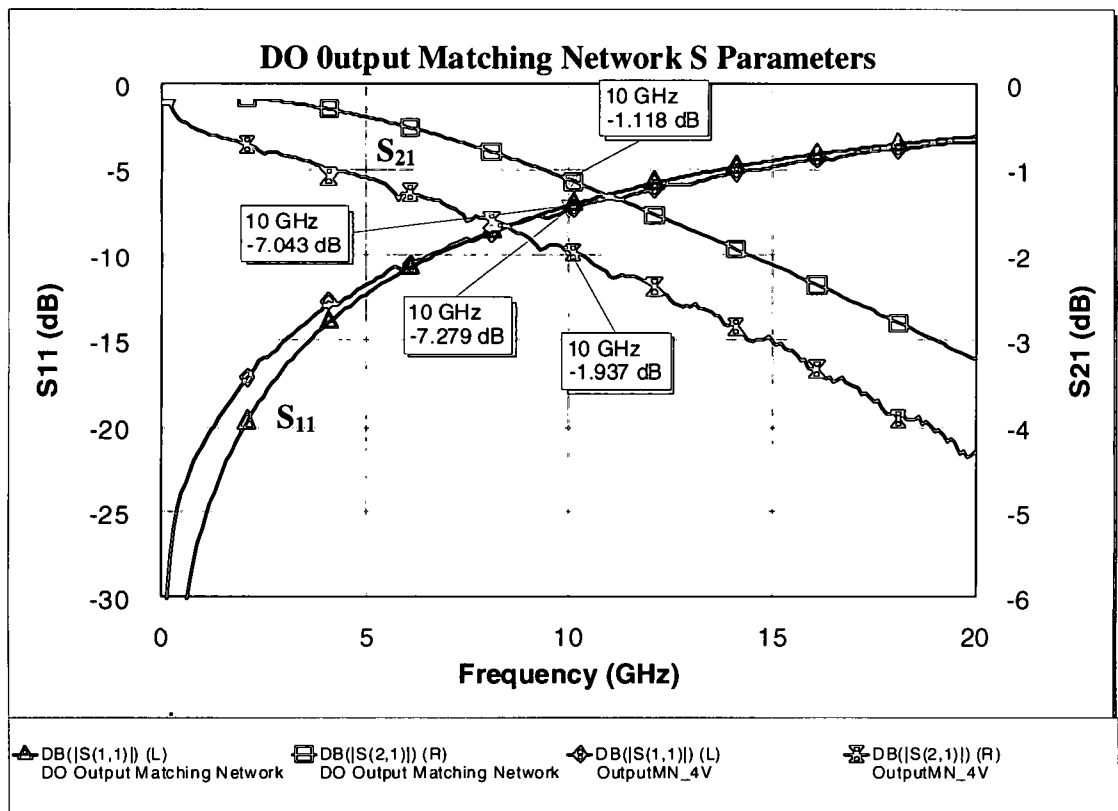
### 5.3.3 Dropouts of Matching Networks Results

The dropout circuits of the matching networks are also critical in the debugging process of the overall LNA. These circuits can help eliminate possible problems that occur in the testing of the LNA. Also the input and the output matching networks verify the tuning capabilities of the BST thin film capacitors. Figure 5.18 shows the comparison of the simulated and the measured S-parameters for the input matching network dropout and Figure 5.19 shows the comparison of the simulated and the measured S-parameters for the output matching network dropout. The simulation results of both matching networks show a simple low pass filter response. The simulation of the output matching

network is very close to matching the measured data because the output matching network has a similar schematic to the model used for the 5  $\mu\text{m}$  by 5  $\mu\text{m}$  BST thin film capacitor. The magnitude for the S-parameters of the input matching network has a 2 dB difference between the measured and the simulated but the resonance is the same in both. The input matching network has longer lengths of CPW transmission lines and it appears that the CPW substrate model for the simulation may not be accurate. The comparison of the S-parameters for the CPW transmission line dropout circuit could help determine the accuracy of the substrate model for the simulations.

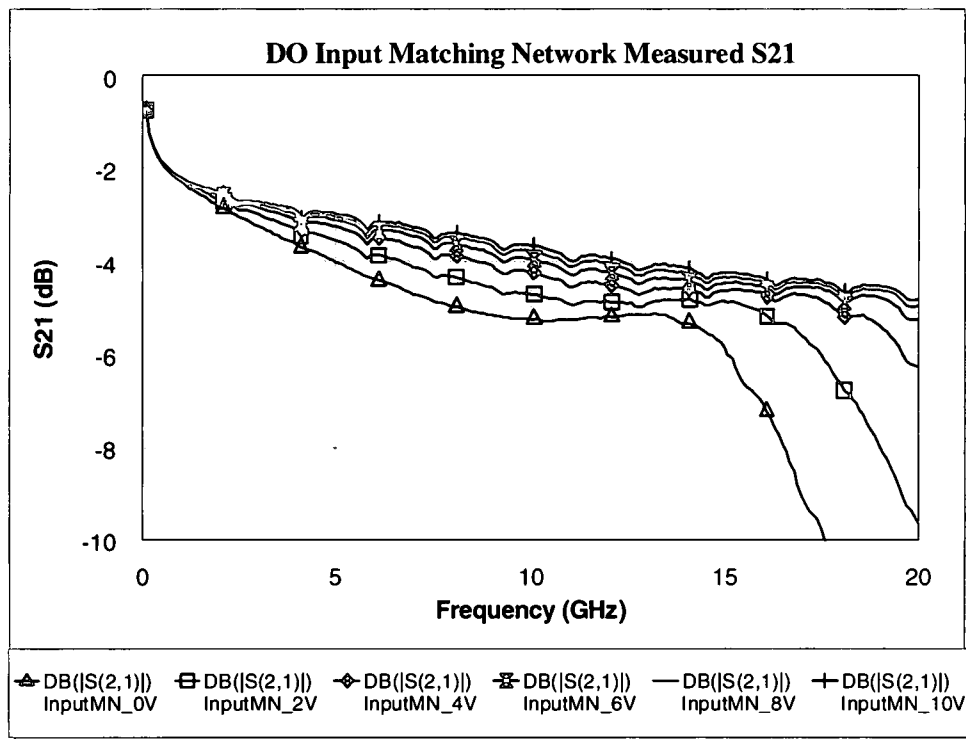


**Figure 5.18: Input Matching Network Dropout S-Parameters Comparison**

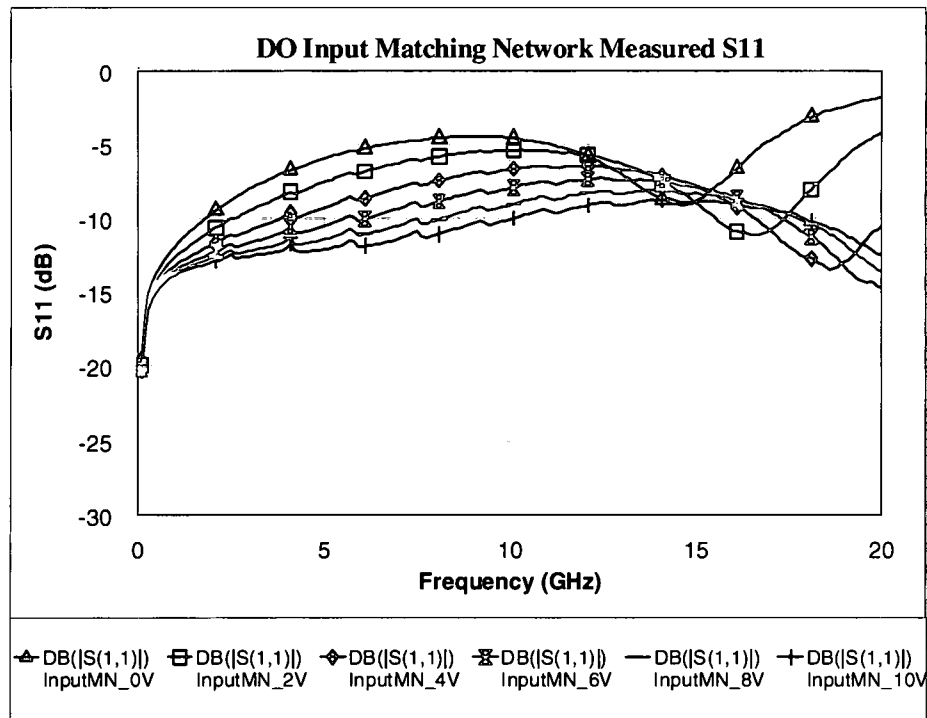


**Figure 5.19: Output Matching Network Dropout S-Parameters Comparison**

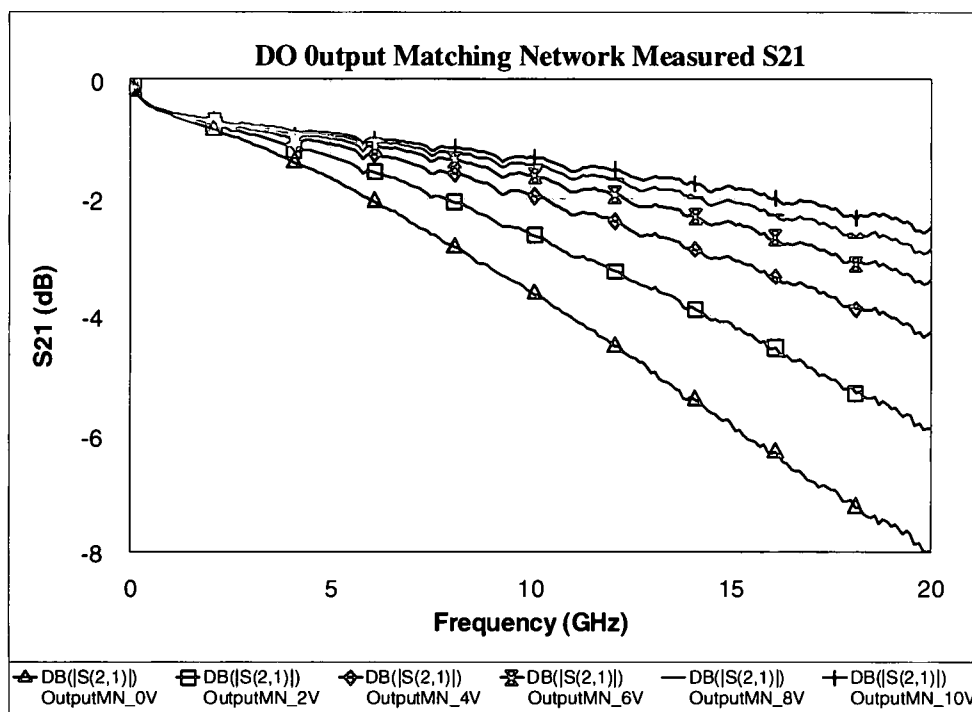
Also the input and the output matching networks dropout circuits are measured to verify their tuning capabilities. Figure 5.20 shows the insertion loss and Figure 5.21 shows the return loss of the input matching network dropout as the bias voltage is varied from 0V to 10V in increments of 2V. Figure 5.22 shows the insertion loss and Figure 5.23 shows the return loss of the output matching network as the bias voltage is varied from 0V to 10V in increments of 2V. It is very clear that the higher dc bias improves the matching network's performance, improves the matching, and lowers the insertion loss.



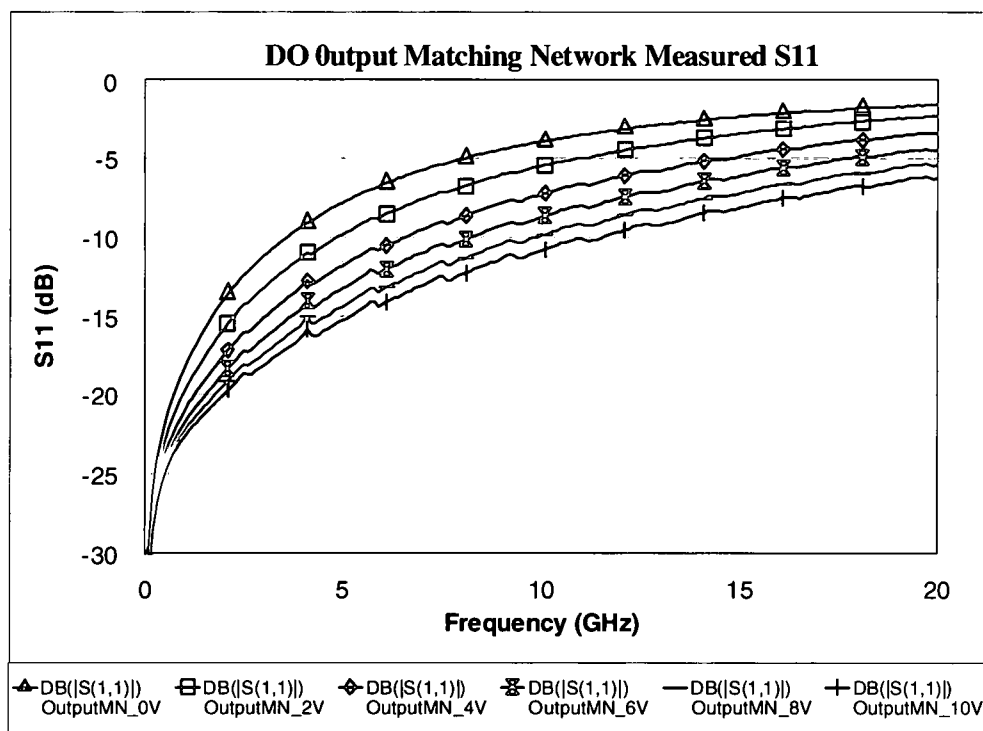
**Figure 5.20: Measured Insertion Loss for the Input Matching Network Dropout**



**Figure 5.21: Measured Return Loss for the Input Matching Network Dropout**



**Figure 5.22: Measured Insertion Loss for the Output Matching Network Dropout**



**Figure 5.23: Measured Return Loss for the Output Matching Network Dropout**

### 5.3.4 Dropouts of Resonant Circuits

The dropouts of the resonant circuits verify the substrate definition used in MWO for all of the LNA simulation. These circuits determine how the fabrication process can alter the resonance of the dropout. The simplest resonant circuit is a 1 mm CPW transmission line. This simulation of this transmission line shows a good 50 ohm match around 10 GHz. The S-parameter comparison of the simulation and the measured data are shown below in Figure 5.24. There is a 2 dB variance between the simulation and the measured data which shows that there is an issue with the substrate definition used in the MWO simulations. The substrate definition needs to be revised to more accurately model the effects of the BST material on the CPW transmission line.

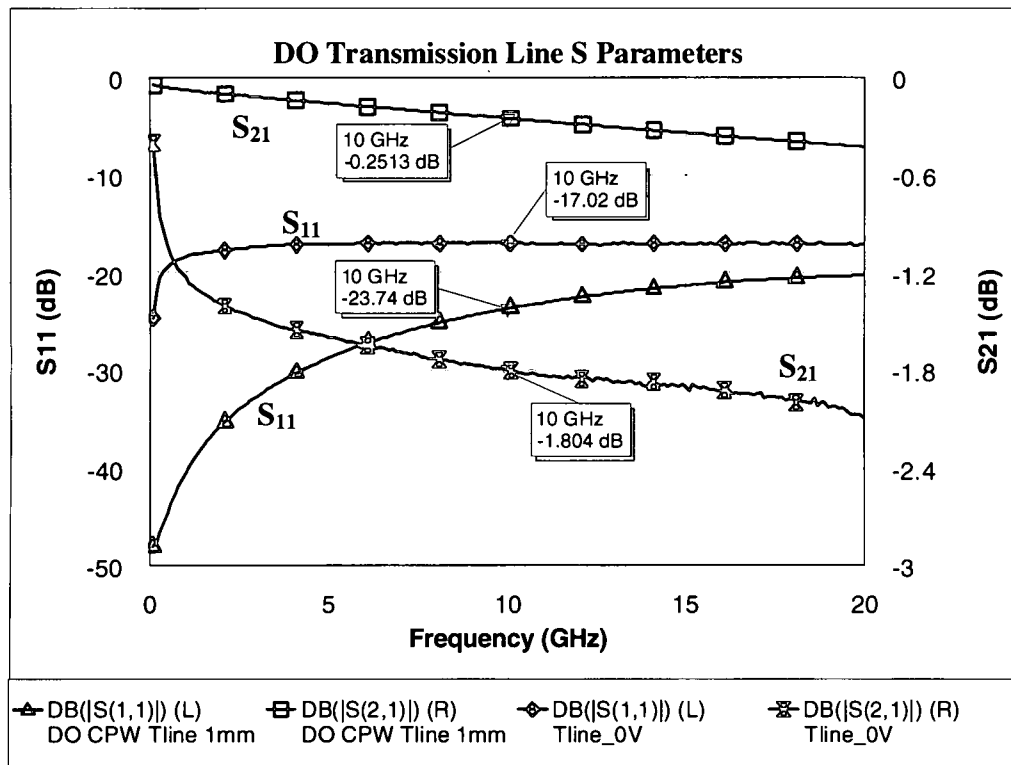
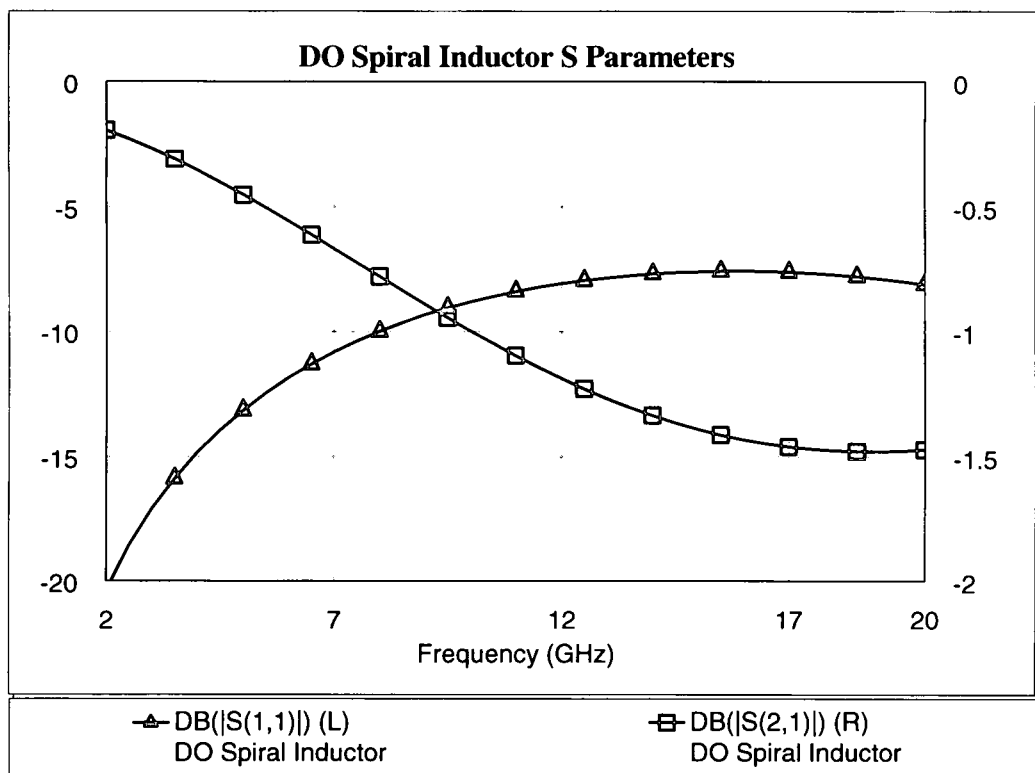


Figure 5.24: Transmission Line Resonant Dropout S-Parameters Comparison

A spiral inductor is designed as a dropout circuit to help determine if higher inductance values are possible through this selected fabrication process. The bridge of the spiral inductor needs to be wire bonded together. Also this dropout circuit can assist in detecting the effects of the wire bond on the inductance value. Figure 5.25 shows the S-parameter simulation of the spiral inductor dropout circuit.

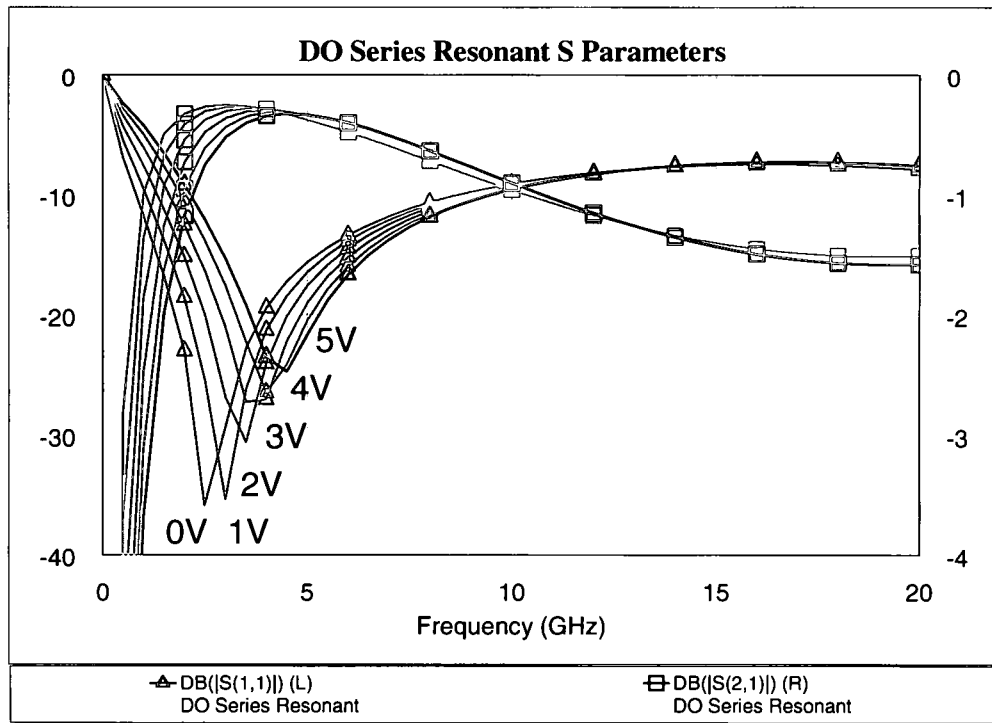


**Figure 5.25: Spiral Inductor Resonant Dropout S-Parameters**

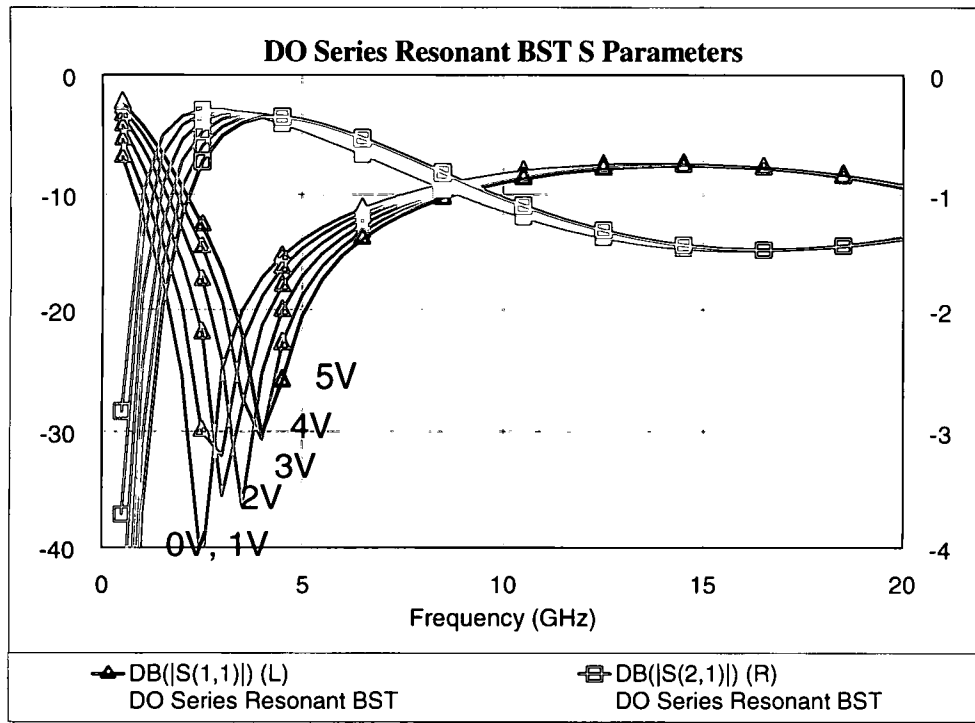
Two series resonant circuits are designed to also assist in the verification of the substrate definition and for characterization of the passive components. The first series resonant circuit includes a spiral inductor with pads for wire bonding the bridge and a series BST thin film capacitor similar to the DC blocking



capacitor. The second series resonant circuit contains a spiral inductor with two BST thin film capacitors in series acting as the bridge of the spiral inductor. These resonant circuits have a bandpass response and can be tuned by applying a voltage on the RF signal line. Figure 5.26 shows the simulation of first series resonant dropout circuit and Figure 5.27 shows the simulation of the series resonant dropout circuit with the BST thin film capacitors.

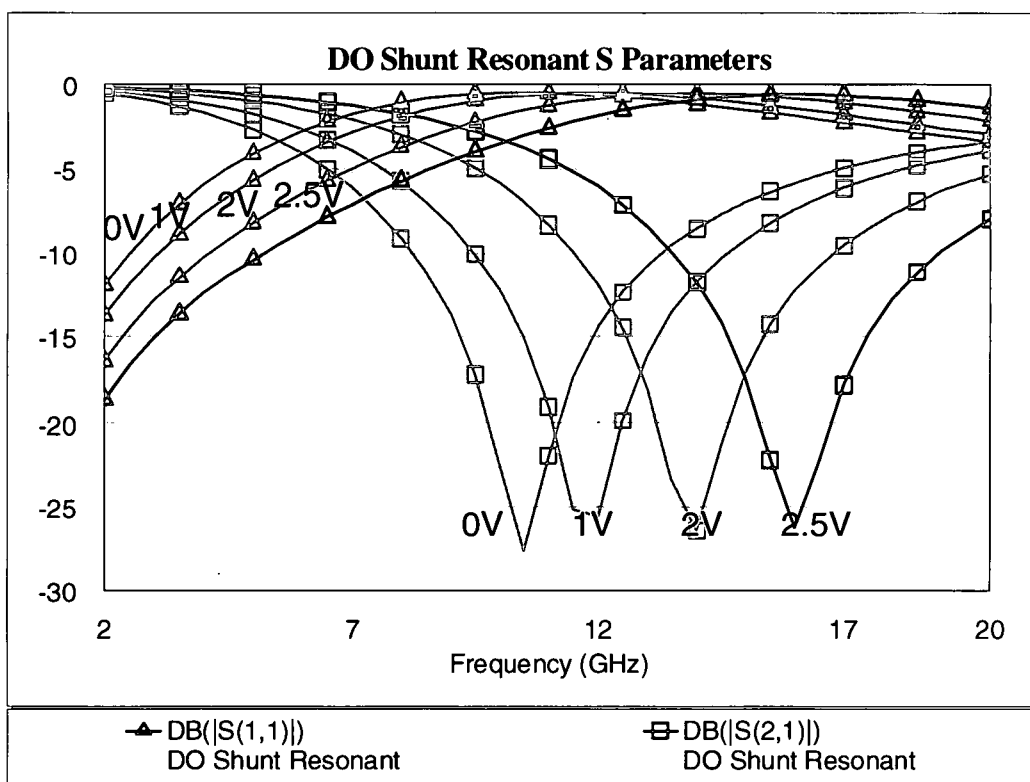


**Figure 5.26: Series Resonant Dropout S-Parameters**



**Figure 5.27: Series Resonant with BST Capacitors Dropout S-Parameters**

The last resonant dropout circuit is a shunt resonant circuit using a RF inductive line in series with a  $5\ \mu\text{m} \times 5\ \mu\text{m}$  BST thin film capacitor shunted to ground. This shunt resonant circuit has a bandstop response. The resonant frequency can be tuned by adjusting the applied voltage for the BST thin film capacitor. Figure 5.28 shows the simulation of the shunt resonant circuit with the bias voltage varied from 0 – 2.5V.



**Figure 5.28: Shunt Resonant Dropout S-Parameters**

## 5.4 Discussion

The simulated LNA is able to meet all of the design requirements except for the gain. The 0.54 dB drop in gain from the ideal LNA is considered an acceptable value for this project. The drop in gain can be associated to the restrictions on the fabrication process and not being able to generate large inductance values. Also the pad frames for the surface mount components added additional losses in the performance of the LNA. It is possible to tune the final LNA to adjust for this loss and hopefully recover the 0.5 dB loss in gain. The noise figure of the simulated LNA is 1 dB lower than the specification that allows for a 1 dB margin for the fabricated LNA. Also the simulated LNA had a

bandwidth of 1.1 GHz that meets the required bandwidth of 1 GHz. Overall the simulated LNA is able to meet the required specifications and demonstrate the tunability of the BST thin film capacitors.

Several of the dropout circuits were measured and the results are compared to the simulations. The BST thin capacitor with an area of  $5\text{ }\mu\text{m} \times 5\text{ }\mu\text{m}$  model is reasonably accurate compared to the simulation. The capacitance had a tuning range of 3.5:1. The CPW transmission line dropout had some variance with the simulation which can be a result from the substrate model used for the MWO simulations. Since the substrate definition was not accurate, the measurements are showing additional loss especially for the input matching network dropout circuit.

## CHAPTER VI

### Summary and Conclusions

The development of reconfigurable electronics offers a single adaptable system for multiple platforms. The benefits of the BST thin film's voltage tunable dielectric properties make it ideal for these tunable applications. The high tuning range, low control voltage and high integration capabilities demonstrate some of the benefits of this material. This project develops a design methodology for a frequency agile X-Band LNA using BST technology. The LNA is designed for a center frequency of 10 GHz and a bandwidth of 1 GHz. The desired tuning range is 9 – 11 GHz and the overall gain is 10 dB with a NF less than 3 dB. This LNA design was fabricated on a high resistivity Si substrate with a BST thin film dielectric sandwiched between two metal layers. In addition to the LNA design, several dropout circuits are designed and fabricated to aid in the material characterization and verification of the LNA performance.

After an ideal lumped element LNA was designed to meet the design requirements, the final LNA is designed as a layout using the models from MWO to simulate the effects of the interconnects, surface mount components and BST thin film capacitors. The predicted LNA performance is very close to meeting design objectives. The S-parameters are plotted and show a slight degradation in the gain and tuning range. The overall gain of the LNA centered at 10 GHz is 0.54 dB below the desired gain value. Also the overall tuning range is reduced to

9.5 -11 GHz. The bandwidth is still within the required specification with 1.1 GHz. The gain remains very close to meeting the desired design specifications while the bandwidth is still greater than the design specifications. The input bias for the BST thin film capacitors is 1.97 V and the output bias for the BST thin film capacitor is 4.65 V.

Initial measurements performed on  $5\text{ }\mu\text{m} \times 5\text{ }\mu\text{m}$  BST capacitors confirmed the large tunability, from 0.56 pF at 0 V to 0.165 pF at 8 V, a tunability of about 3.5: 1. The tunable nature of input and output matching networks were also experimentally verified. A simple LNA was integrated with the BST thin film capacitor based matching networks. The LNA exhibited a reduced gain of 4.65 dB at 10 GHz with a dc bias of 2 V at the drain and -0.5 V at the gate. The small bias voltages however, could not tune the BST thin film sufficiently to observe the frequency tunability of the LNA.

The loss in gain can be due to the necessary use of surface mount components for the bias and stability networks and the large pad frame associated with them. Also, the loss in tuning range can be caused by the CPW RF transmission lines that do not result in the same inductance values as spiral inductors or surface mount inductors.

Overall the design of the frequency agile LNA demonstrates the use of the tunable BST thin film capacitors in a novel design. The restrictions imposed by selected fabrication process limited the available components usable in the design affecting the overall performance. Vias would be a great addition to the fabrication process and allow for the use of such components as spiral inductors.

The frequency tuning of the LNA illustrates the benefits of integrating the BST thin films in the matching networks and indicates that the BST thin films are a viable technology for future tunable circuit applications.

The next step to enhance the scope of this project for the frequency agile LNA is to develop code for an FPGA for use in the control of the BST thin film capacitors. The FPGA can control the bias values for the capacitors and optimize the performance of the amplifier as the frequency is shifted. This will allow for a self-adaptable frequency tunable LNA for future applications and greater tunability control for the BST thin film capacitors.

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## Appendix A

### NEC NE321000 Hetero Junction Fieldeffect Transistor Data Sheet

**NEC**

#### DATA SHEET

#### HETERO JUNCTION FIELDEFFECT TRANSISTOR

**NE321000**

#### C to Ka BAND SUPER LOW NOISE AMPLIFIER N-CHANNEL HJ-FET CHIP

#### DESCRIPTION

The NE321000 is Hetero Junction FET that utilizes the hetero junction to create high mobility electrons. Its excellent low noise and associated gain make it suitable for DBS and another commercial systems, industrial and space applications.

#### FEATURES

- Super Low Noise Figure & High Associated Gain  
NF = 0.35 dB TYP.  $G_s = 13.5$  dB TYP. @  $f = 12$  GHz
- Gate Length:  $L_g \leq 0.20 \mu\text{m}$
- Gate Width :  $W_g = 160 \mu\text{m}$

#### ORDERING INFORMATION (PLAN)

Part Number	Quality Grade
NE321000	Standard (Grade D)

Remark: To order evaluation samples, please contact your local NEC sales office. (Part number for sample order: NE321000)

#### ABSOLUTE MAXIMUM RATINGS ( $T_A = +25^\circ\text{C}$ )

Parameter	Symbol	Ratings	Unit
Drain to Source Voltage	$V_{DS}$	4.0	V
Gate to Source Voltage	$V_{GS}$	-3.0	V
Drain Current	$I_D$	$I_{DSS}$	mA
Gate Current	$I_G$	100	$\mu\text{A}$
Total Power Dissipation	$P_{tot}$	200	mW
Channel Temperature	$T_{ch}$	175	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-65 to +175	$^\circ\text{C}$

Note: Chip mounted on an Alumina heatsink (size:  $3 \times 3 \times 0.6$  t)

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RECOMMENDED OPERATING CONDITIONS ( $T_A = +25^\circ\text{C}$ )

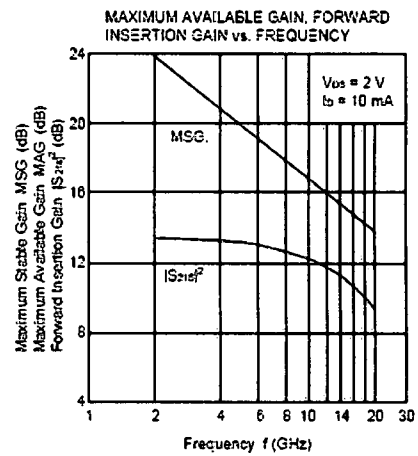
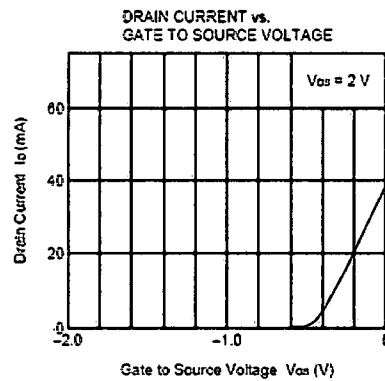
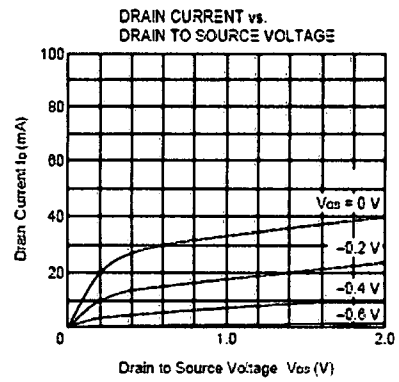
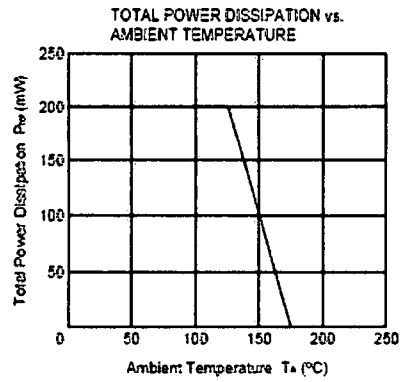
Parameter	Symbol	MIN.	TYP.	MAX.	Unit
★ Drain to Source Voltage	$V_{DS}$	1	2	3	V
★ Drain Current	$I_D$	5	10	15	mA
Input Power	$P_{in}$	—	—	0	dBm

ELECTRICAL CHARACTERISTICS ( $T_A = +25^\circ\text{C}$ )

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Gate to Source Leak Current	$I_{GSS}$	$V_{GS} = -3\text{ V}$	—	0.5	10	$\mu\text{A}$
Saturated Drain Current	$I_{DSS}$	$V_{DS} = 2\text{ V}, V_{GS} = 0\text{ V}$	15	40	70	mA
Gate to Source Cut Off Voltage	$V_{GS(off)}$	$V_{DS} = 2\text{ V}, I_{DSS} = 100\text{ }\mu\text{A}$	-0.2	-0.7	-2.0	V
Transconductance	$g_m$	$V_{DS} = 2\text{ V}, I_{DS} = 10\text{ mA}$	40	55	—	mS
Noise Figure	NF	$V_{DS} = 2\text{ V}, I_{DS} = 10\text{ mA}$	—	0.35	0.45	dB
NF Associated Gain	$G_n$	$f = 12\text{ GHz}$	12.0	13.5	—	dB

Remark RF performance is determined by packaging and testing 10 chips per wafer.  
Wafer rejection criteria for standard devices is 2 rejects per 10 samples.

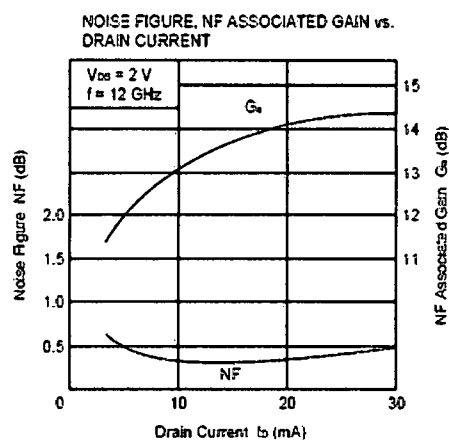
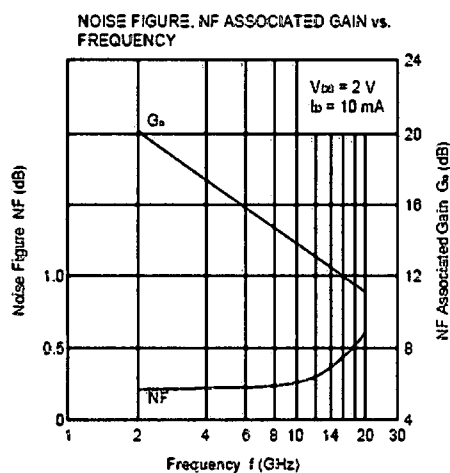
TYPICAL CHARACTERISTICS ( $T_A = +25^\circ\text{C}$ )



# GAIN CALCULATIONS

$$MSG = \left| \frac{S_{21}}{S_{12}} \right| \quad K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2 |S_{12}| |S_{21}|}$$

$$MAG = \left| \frac{S_{21}}{S_{12}} \right| (k \pm \sqrt{k^2 - 1}) \quad \Delta = S_{11} \cdot S_{22} - S_{21} \cdot S_{12}$$



## S-PARAMETERS

MAG. AND ANG.

V<sub>DS</sub> = 2 V, I<sub>b</sub> = 10 mA

FREQUENCY GHz	S <sub>11</sub>		S <sub>21</sub>		S <sub>12</sub>		S <sub>22</sub>	
	MAG.	ANG.	MAG.	ANG.	MAG.	ANG.	MAG.	ANG.
2.0	0.986	-13.2	4.72	170.2	0.020	81.3	0.602	-10.0
3.0	0.957	-19.3	4.70	165.6	0.030	77.3	0.599	-14.8
4.0	0.951	-25.7	4.62	160.5	0.040	73.2	0.593	-19.9
5.0	0.970	-32.7	4.50	155.7	0.050	69.4	0.588	-25.6
6.0	0.962	-38.6	4.45	151.6	0.059	65.3	0.583	-30.1
7.0	0.952	-44.4	4.37	147.4	0.067	62.2	0.574	-34.4
8.0	0.941	-50.1	4.28	143.5	0.074	58.6	0.567	-39.1
9.0	0.927	-55.6	4.17	139.7	0.081	55.2	0.564	-43.1
10.0	0.912	-61.5	4.03	135.6	0.087	51.5	0.552	-47.2
11.0	0.896	-66.9	3.90	131.5	0.094	48.0	0.541	-52.0
12.0	0.882	-71.6	3.79	128.0	0.100	44.9	0.536	-55.5
13.0	0.866	-75.9	3.66	124.9	0.104	42.0	0.526	-55.6
14.0	0.855	-80.2	3.54	121.9	0.108	39.0	0.518	-62.1
15.0	0.843	-84.2	3.42	119.0	0.111	36.2	0.509	-65.0
16.0	0.827	-88.5	3.30	115.8	0.115	33.5	0.501	-65.3
17.0	0.807	-92.6	3.16	112.9	0.116	30.5	0.494	-71.2
18.0	0.796	-95.3	3.05	110.6	0.117	28.5	0.488	-73.2
19.0	0.793	-98.0	2.97	108.7	0.120	27.9	0.489	-75.2
20.0	0.786	-101.2	2.89	106.2	0.123	26.5	0.487	-77.4
21.0	0.782	-103.8	2.79	104.1	0.125	24.9	0.484	-80.9
22.0	0.783	-106.4	2.70	101.9	0.128	23.3	0.486	-82.7
23.0	0.785	-109.9	2.62	99.5	0.132	20.7	0.477	-84.1
24.0	0.778	-113.4	2.53	97.4	0.135	18.8	0.474	-87.9
25.0	0.766	-116.0	2.46	95.8	0.135	16.8	0.481	-85.3
26.0	0.757	-118.1	2.40	93.8	0.135	15.3	0.469	-89.2
27.0	0.753	-119.9	2.33	92.5	0.133	14.3	0.463	-91.6
28.0	0.755	-121.6	2.29	90.6	0.136	14.0	0.484	-93.5
29.0	0.746	-124.2	2.23	88.4	0.135	12.6	0.481	-95.2
30.0	0.743	-126.2	2.16	86.8	0.136	11.3	0.475	-97.5

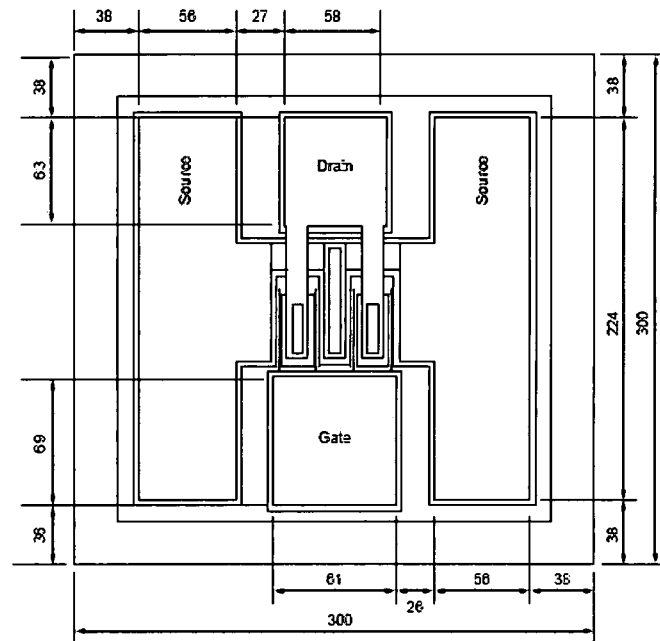



## NOISE PARAMETERS

V<sub>DS</sub> = 2 V, I<sub>D</sub> = 10 mA

Freq. (GHz)	NF <sub>no</sub> (dB)	G <sub>n</sub> (dB)	Γ <sub>opt</sub>		Rn/50
			MAG.	ANG. (deg.)	
2.0	0.21	19.5	0.84	3.7	0.31
4.0	0.22	17.6	0.87	8.2	0.31
6.0	0.24	15.9	0.82	13.3	0.32
8.0	0.26	14.6	0.77	16.8	0.32
10.0	0.28	13.5	0.73	24.8	0.32
12.0	0.31	12.7	0.69	31.4	0.31
14.0	0.36	12.1	0.67	35.4	0.31
16.0	0.45	11.6	0.64	45.9	0.30
18.0	0.52	11.3	0.63	53.9	0.29
20.0	0.59	11.2	0.62	62.4	0.28
22.0	0.66	11.1	0.61	71.4	0.27
24.0	0.72	11.2	0.62	80.8	0.25
26.0	0.79	11.2	0.63	90.8	0.23

CHIP DIMENSIONS (Unit:  $\mu\text{m}$ )



Thickness = 140  $\mu\text{m}$   
 : BONDING AREA

**CHIP HANDLING****DIE ATTACHMENT**

Die attach operation can be accomplished with Au-Sn (within a 300 °C - 10 s) performs in a forming gas environment.

Epoxy die attach is not recommend.

**BONDING**

Bonding wires should be minimum length, semi hard gold wire (3 to 8 % elongation) 20 microns in diameter.

Bonding should be performed with a wedge tip that has a taper of approximately 15 %. Bonding time should be kept to minimum.

As a general rule, the bonding operation should be kept within a 290 °C, 2 minutes for all bonding wires.

If longer periods are required, the temperature should be lowered.

**PRECAUTION**

The user must operate in a clean, dry environment. The chip channel is glassivated for mechanical protection only and does not preclude the necessity of a clean environment.

The bonding equipment should be periodically checked for sources of surge voltage and should be properly grounded at all times. In fact, all test and handling equipment should be grounded to minimize the possibilities of static discharge.

Avoid high static voltage and electric fields, because this device is Hetero Junction field effect transistor with shotky barrier gate.

### CAUTION

The Great Care must be taken in dealing with the devices in this guide.  
The reason is that the material of the devices is GaAs (Gallium Arsenide), which is designated as harmful substance according to the law concerned.  
Keep the law concerned and so on, especially in case of removal.

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    - Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
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M7 95.0

## Appendix B

### ATC 500 S Series Broadband 0603 Capacitors



**AMERICAN TECHNICAL CERAMICS**

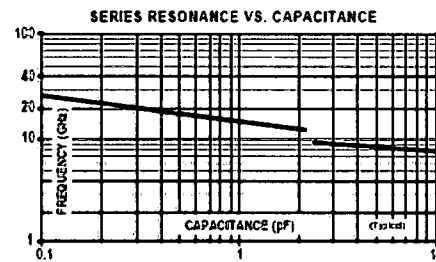
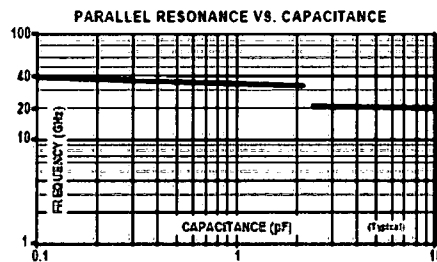
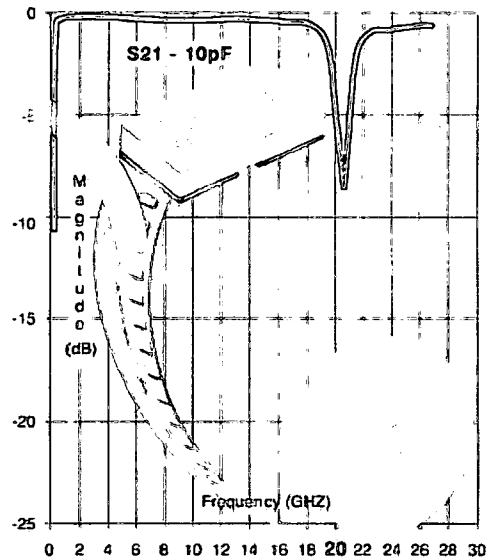
Component and Custom Integrated Packaging Solutions for RF, Microwave and Telecommunications

#### **ATC 500S Series BMC Broadband Microwave Millimeter-wave 0603 NPO SMT Capacitors**

- Low Insertion Loss
- Ultra High Self Resonance
- Surface Mountable
- Rugged Construction

ATC introduces the new 500S Series Broadband Microwave Capacitor (BMC). This unique, patented component greatly exceeds both multilayer and single layer capacitor performance. It delivers extremely low insertion loss with ultra-high self resonance performance, in a rugged, laser-marked package compatible with automatic SMT manufacturing.

Functional applications include Broadband (Bypass, Coupling, Feedback, Impedance Matching, D.C. Blocking) and Tuning.



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## ATC 500 S Series Broadband 0603 NPO Capacitors

### ELECTRICAL AND MECHANICAL SPECIFICATIONS

#### QUALITY FACTOR (Q):

Greater than 1,000 @ 1 MHz

#### TEMPERATURE COEFFICIENT OF CAPACITANCE (T.C.):

0  $\pm$  30 PPM/°C (-55°C to +125°C) (0.1 pF to 2.2 pF)

0  $\pm$  60 PPM/°C (-55°C to +125°C) (2.4 pF to 10 pF)

#### INSULATION RESISTANCE (IR):

0.1 pF to 10 pF:

10<sup>12</sup> Megohms min. @ +25°C @ rated WVDC.

10<sup>10</sup> Megohms min. @ +125°C @ rated WVDC.

#### WORKING VOLTAGE (WVDC):

100 WVDC (0.1 pF to 4.7 pF)

50 WVDC (5.1 pF to 10 pF)

#### DIELECTRIC WITHSTANDING VOLTAGE (DWV):

200% of rated WVDC for 5 secs.

#### OPERATING TEMPERATURE RANGE:

From -55°C to +125°C (No derating of working voltage).

#### TERMINATION: Chip style suitable for surface mounting.

Platinum with gold flash.

Die Shear Strength Test per MIL-STD-883, Method 2019.

### ENVIRONMENTAL TESTS

ATC 500 S Series Broadband Microwave Capacitors are designed and manufactured to meet and exceed the applicable requirements of MIL-C-55681.

#### THERMAL SHOCK:

MIL-STD-202, Method 107, Condition A.

#### MOISTURE RESISTANCE:

MIL-STD-202, Method 108.

#### LOW VOLTAGE HUMIDITY:

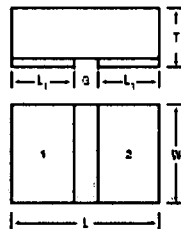
MIL-STD-202, Method 103, Condition A, with 1.5 Volts D.C. applied while subjected to an environment of 85°C with 85% relative humidity for 250  $\pm$  12 hours.

#### LIFE TEST:

MIL-STD-202, Method 108, for 2000 hours, at 125°C.

200% WVDC applied.

## ATC 500 S SERIES BROADBAND 0603 CAPACITORS: MECHANICAL CONFIGURATIONS



MECHANICAL DIMENSIONS - INCHES (mm)				
Length (L)	L <sub>1</sub>	Width (W)	Thickness (T)	Gap (G)
.060 $\pm$ .005 (1.52 $\pm$ .127)	.025 (.635) nom.	.030 $\pm$ .005 (.762 $\pm$ .127)	.024 (.609) max.	.010 (.254) min.



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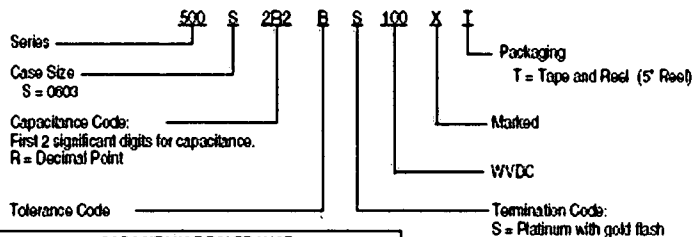
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## ATC 500 S Series Broadband 0603 NPO Capacitors

### CAPACITANCE VALUES

CAP. CODE	CAP. (pF)	TOL.	RATED WVDC	CAP. CODE	CAP. (pF)	TOL.	RATED WVDC	CAP. CODE	CAP. (pF)	TOL.	RATED WVDC	CAP. CODE	CAP. (pF)	TOL.	RATED WVDC
0R1	0.1			1R1	1.1			3R0	3.0			6R8	6.8		
0R2	0.2			1R2	1.2			3R3	3.3			7R5	7.5	C, J, K, M	
0R3	0.3			1R3	1.3			3R6	3.6			8R2	8.2		
0R4	0.4			1R5	1.5			3R9	3.9			9R1	9.1		
0R5	0.5	A, B, C, D	100	1R6	1.6	B, C, D	100	4R3	4.3			100	10	G, J, K, M	
0R6	0.6			1R8	1.8			4R7	4.7						
0R7	0.7			2R0	2.0			5R1	5.1						
0R8	0.8			2R2	2.2			5R6	5.6						
0R9	0.9			2R4	2.4			6R2	6.2						
1R0	1.0			2R7	2.7										

### ATC 500 SERIES BMC PART NUMBER CODE



CAPACITANCE TOLERANCE							
Code	A	B	C	D	G	J	M
Tol.	$\pm 0.5$ pF	$\pm 0.1$ pF	$\pm 0.25$ pF	$\pm 0.5$ pF	$\pm 2\%$	$\pm 5\%$	$\pm 10\%$

The above part number refers to a 500S Series (case size S) 2.2 pF capacitor, B tolerance ( $\pm 0.1$  pF), Termination Code S (Platinum with gold flash), 100 WVDC, with marking and 5" tape and reel packaging.

ATC accepts orders for our parts using designations with or without the "ATC" prefix. Both methods of defining the part number are equivalent, i.e., part numbers referenced with the "ATC" prefix are interchangeable to parts referenced without the "ATC" prefix. Customers are free to use either in specifying or procuring parts from American Technical Ceramics.

For additional information and catalogs contact your ATC representative or call direct at (631) 622-4700. Consult factory for additional performance data.



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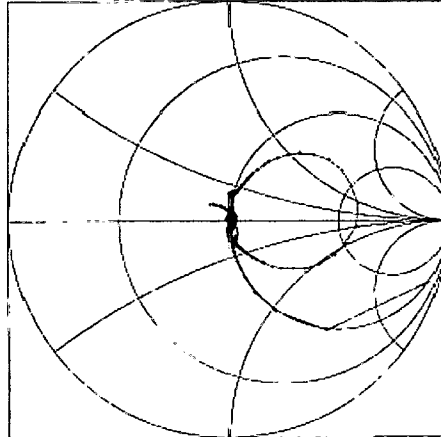


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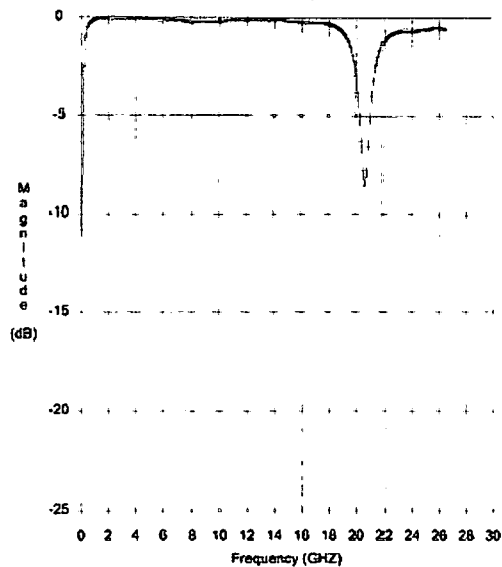
### **ATC 500S Series Broadband 0603 NPO Capacitors**

S11 - 10 pF



Frequency Range: 50 MHz to 26.5 GHz

S21 - 10 pF



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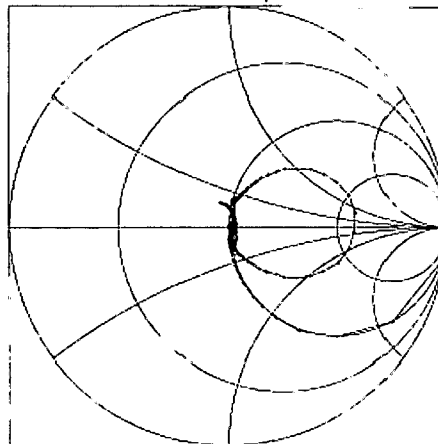




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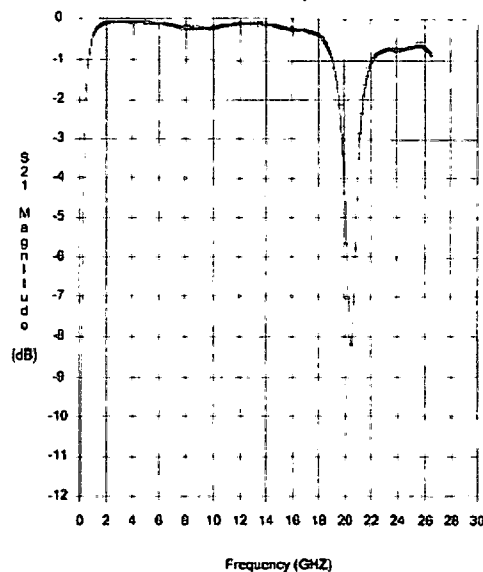
### **ATC 500S Series Broadband 0603 NPO Capacitors**

S11 - 5.1 pF



Frequency Range: 50 MHz to 26.5 GHz

S21 - 5.1 pF



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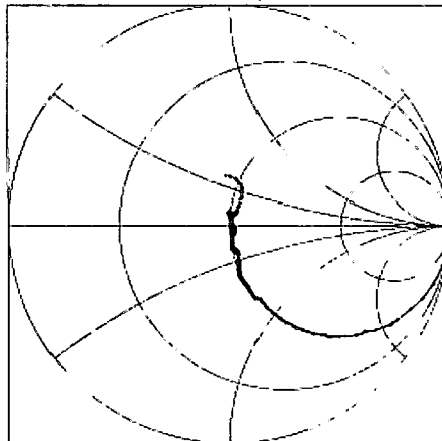


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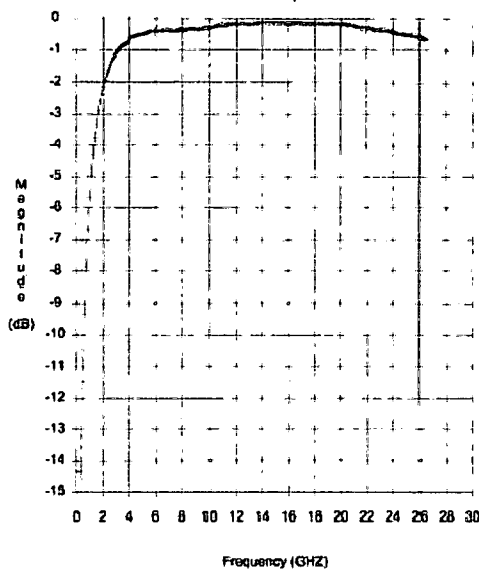
### **ATC 500 S Series Broadband 0603 NPO Capacitors**

**S11 - 1 pf**



Frequency Range: 50 MHz to 26.5 GHz

**S21 - 1 pf**



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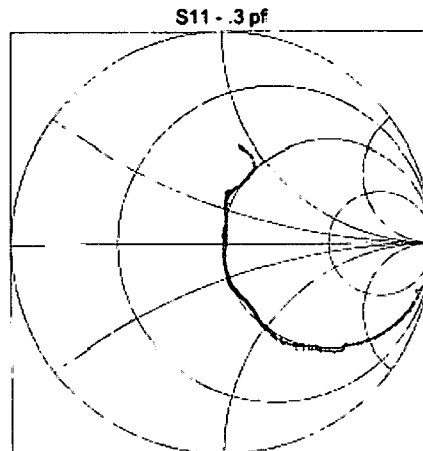
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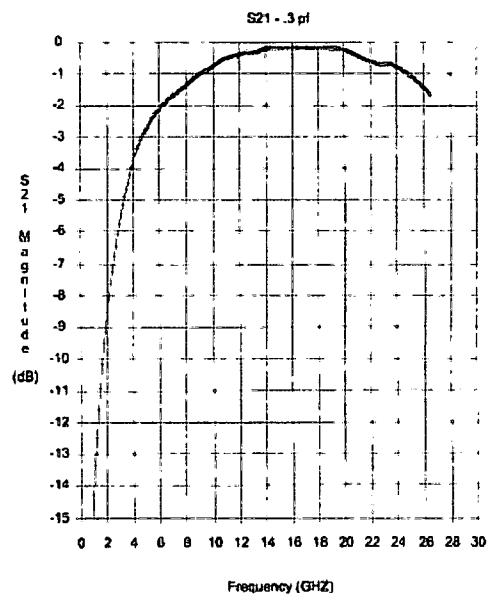


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### **ATC 500 S Series Broadband 0603 NPO Capacitors**



Frequency Range: 50 MHz to 26.5 GHz



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## Appendix C

### Coilcraft 0201CS Series 0503 Chip Inductors

Document 320-1



**NEW!**

## Chip Inductors - 0201CS Series (0503)

Coilcraft has scored another first with the world's smallest wirewound inductor, the 0201CS Series.

Occupying a mere quarter square millimeter of board space, they feature outstanding SRF values (> 26 GHz), low DCR and, despite their small size, excellent current

handling capability. There are 26 inductance values from 0.5 to 14 nH, most available in 5% tolerance.

Coilcraft Designer's Kit C368 contains samples of each of the standard parts shown. To order, contact Coilcraft or visit <http://order.coilcraft.com> to purchase on-line.

Part number <sup>1</sup>	Inductance <sup>2</sup> (nH)	Percent tolerance	800 MHz		1.7 GHz		SRF typ <sup>4</sup> (GHz)	DCR max <sup>5</sup> (Ohms)	I <sub>rms</sub> <sup>6</sup> (mA)
			L typ	Q typ <sup>3</sup>	L typ	Q typ <sup>3</sup>			
0201CS-0N5KKL_	0.5	10	0.50	29	0.49	43	>26	0.015	1400
0201CS-0N6KKL_	0.6	10	0.58	31	0.58	51	>26	0.024	1150
0201CS-1N2XJL_	1.2	5	1.16	42	1.16	60	24.6	0.027	1050
0201CS-1N3XJL_	1.3	5	1.24	38	1.24	57	26.0	0.034	960
0201CS-1N4XJL_	1.4	5	1.35	27	1.34	37	25.8	0.068	680
0201CS-1N5XJL_	1.5	5	1.47	28	1.47	40	25.8	0.086	640
0201CS-2N3XJL_	2.3	5	2.28	45	2.28	64	16.5	0.039	860
0201CS-2N4XJL_	2.4	5	2.36	35	2.36	53	19.1	0.062	730
0201CS-2N5XJL_	2.5	5	2.50	31	2.49	44	19.3	0.124	520
0201CS-3N3XJL_	3.3	5	3.31	42	3.32	62	14.8	0.051	700
0201CS-3N7XJL_	3.7	5	3.65	39	3.66	58	13.0	0.064	680
0201CS-3N8XJL_	3.8	5	3.81	38	3.81	60	13.0	0.102	570
0201CS-3N9XJL_	3.9	5	3.89	35	3.89	50	14.6	0.128	520
0201CS-4N8XJL_	4.8	5	4.83	34	4.83	50	11.2	0.063	730
0201CS-5N2XJL_	5.2	5	5.21	36	5.21	55	12.7	0.126	520
0201CS-5N5XJL_	5.5	5	5.49	35	5.49	50	11.0	0.200	400
0201CS-6N7XJL_	6.7	5	6.71	40	6.72	59	10.1	0.094	590
0201CS-7N0XJL_	7.0	5	6.97	39	6.97	60	10.7	0.149	440
0201CS-7N5XJL_	7.5	5	7.44	36	7.46	50	11.8	0.238	360
0201CS-8N7XJL_	8.7	5	8.68	38	8.74	59	9.4	0.139	500
0201CS-9N0XJL_	9.0	5	9.02	42	9.04	63	9.7	0.173	400
0201CS-9N4XJL_	9.4	5	9.38	36	9.39	51	8.9	0.218	370
0201CS-9N6XJL_	9.6	5	9.62	38	9.64	53	9.1	0.276	320
0201CS-11NXJL_	11.0	5	11.11	40	11.15	62	8.5	0.197	340
0201CS-12NXJL_	12.0	5	12.15	39	12.20	56	7.8	0.248	330
0201CS-14NXJL_	14.0	5	14.13	37	14.37	51	7.2	0.278	320

1. When ordering, please specify termination and packaging codes:

0201CS-14NXJL W

Termination: L = RoHS compliant silver-platinum-glass frit.  
Special order: S = non-RoHS tin-lead (63/37).

Packaging: W = 7" machine-ready reel, EIA-481 punched paper tape (2000 parts per full reel).

U = Less than full reel. In tape, but not machine ready.  
To have a leader and trailer added (\$25 charge), use code letter W instead.

2. Inductance measured at 250 MHz using a Coilcraft SMD-F fixture in an Agilent/HP 4286 impedance analyzer with Coilcraft-provided correlation pieces.

3. Q measured using an Agilent/HP 4291A with an Agilent/HP 16107 test fixture.

4. SRF measured using an Agilent/HP 8722ES network analyzer and a test fixture with a 0.010" air gap.

5. DCR measured on a micro-ohmmeter and a Coilcraft CCF59 test fixture.

6. Current that causes a 15°C temperature rise from 25°C ambient.

7. Ambient temperature range: -40°C to +125°C with I<sub>rms</sub> current.

+125°C to +140°C with derated current.

8. Storage temperature range: Component -65°C to +125°C.

Packaging: -55°C to +60°C.

9. Resistance to soldering heat: Three reflows at >217°C for 90 seconds (+260°C ±5°C for 20 - 40 seconds), allowing parts to cool to room temperature between.

10. Electrical specifications at 25°C.

11. Temperature coefficient of inductance: +25 to +125 ppm/°C.

See Qualification Standards section for environmental and test data.

Refer to Doc 362 "Soldering Surface Mount Components" before soldering.

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Please check our website for latest information. Document 320-1 Revised 04/19/07

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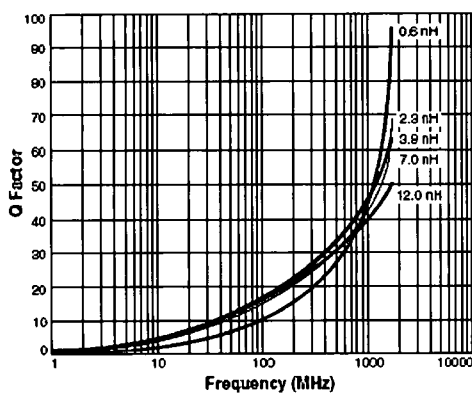
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R002 S93 S98


**NEW!**

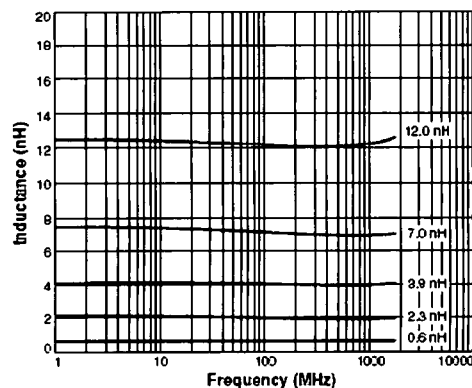
## 0201CS Series (0503)

### Typical Q vs Frequency

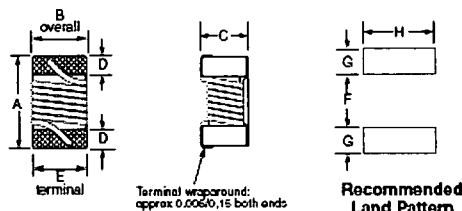
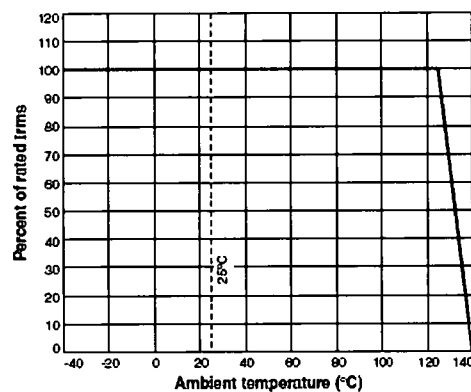


**S-Parameter files**  
ON OUR WEB SITE OR CD  
**SPICE models**  
ON OUR WEB SITE OR CD

### Typical L vs Frequency



### Irms Derating



A max	B max	C max	D	E	F	G	H
0.022	0.014	0.018	0.004	0.010	0.009	0.007	0.013
0.56	0.36	0.46	0.10	0.25	0.23	0.18	0.33

Weight: 0.14 – 0.23 mg  
Tape and reel: 20007" reel 8 mm tape width  
For packaging data see Tape and Reel Specifications section.

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