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MODELING AND EXPERIMENTAL EVALUATION OF
FERROELECTRIC THIN FILMS FOR APPLICATIONS IN
ELECTROMAGNETIC COMPATIBILITY

Dissertation

Submitted to

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In Partial Fulfillment of the Requirements for

The Degree

Doctor of Philosophy in Electrical Engineering

By

Huadong Li

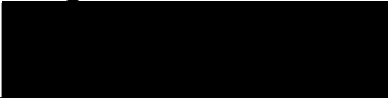
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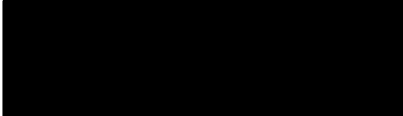
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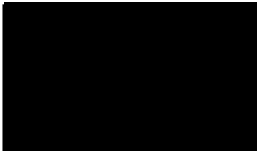
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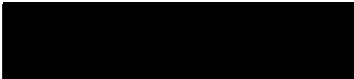
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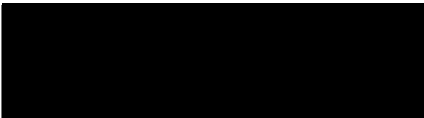
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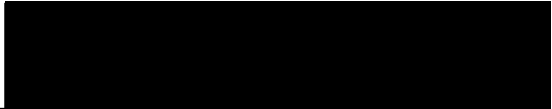
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ABSTRACT

MODELING AND EXPERIMENTAL EVALUATION OF FERROELECTRIC THIN FILMS FOR APPLICATIONS IN ELECTROMAGNETIC COMPATIBILITY

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Ferroelectrics and anti-ferroelectrics have very high dielectric constant and have potential applications in electromagnetic compatibility (EMC) such as decoupling capacitors. This dissertation studied the properties of thin film ferroelectrics and their applications for EMC. A model was developed for the description of ferroelectric thin film's electrical properties. Its polarization is divided into two sections: linear polarization and switching polarization. Simulation shows that the space charge has direct effects on the properties of thin film ferroelectrics. Space charge increases the nonlinearity of the inside field distribution, reduces the peak amplitude of the large signal C-V curve and shrinks its ideal hysteresis loop. Measurements and analyses show that practical hysteresis loop has an initial offset and it is due to the remnant polarization. The hysteresis loop becomes symmetric and it is due to the current leakage in the measurement circuit. Measurements found that the small signal capacitance of thin film ferroelectrics has much smaller peak value on its C-V curves than its large signal capacitance. Analyses show that the difference can not be due to the space charge density change or defect mobility in the films. It is because there exist clearance areas

around coercive voltages when small signals are applied to thin film EF. The effects of the capacitance nonlinearity of a ferroelectrics/anti-ferroelectrics capacitor were analyzed. Simulation indicates that anti-ferroelectrics shows an "increased capacitance" than its nominal value and ferroelectrics shows a "decreased capacitance" than its nominal value in filtering application. Therefore anti-ferroelectric capacitors increase the filtering response, whereas ferroelectric capacitors reduce the filtering response. Due to the "increased capacitance", anti-ferroelectric capacitors also reduce the self-resonance frequency and parallel-resonance frequency. Simulation also shows that anti-ferroelectric capacitors greatly damp parallel resonance. Measurements indicate that a ferroelectric capacitor has much less peak insertion loss than that of a polyester film capacitor with a close capacitance value. Analyses show that there exists a significant series resistance in thin film ferroelectric capacitors and it is the series resistance that reduces the peak insertion loss of thin film ferroelectric capacitors. Measurements and analyses also show that this resistance damps the parallel resonance when local decoupling capacitor and bulk decoupling capacitor are connected in parallel. Further analyses show that this large series resistance does not come from the capacitance nonlinearity. Instead, it is most likely due to the non-switching layer (dead layer) that exists in thin film ferroelectric capacitors. This resistance is not found with BST film and it is thought that it is due to the difference phase: paraelectrics. The study is new and comprehensive. It provides a better understanding of the electric properties of ferroelectrics. This dissertation summarizes the performance analyses of circuits with ferroelectrics and provides valuable guidelines for the EMC applications of ferroelectrics.

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CHAPTER 1

INTRODUCTION

1.1 Ferroelectrics/Antiferroelectrics

1.1.1 Concepts of ferroelectrics

Ferroelectrics (FE) are polar materials that possess at least two equilibrium orientations of the spontaneous polarization vector in the absence of an external electric field, and in which the spontaneous polarization vector may be switched between those orientations by an electric field. The spontaneous polarization in a ferroelectric crystal (or a grain in a ferroelectric film or ceramic) is usually not uniformly aligned throughout the whole crystal along the same direction. A crystal can be divided into many regions and each of them has uniformly oriented spontaneous polarization inside. Those regions are called ferroelectric domains. The region between two domains is called the domain wall (Figure 1.1). The walls which separate domains with oppositely orientated polarization are called 180° walls and those which separate regions with mutually perpendicular polarization are called 90° walls (Figure 1.1). Ferroelectric domains form to minimize the electrostatic energy of depolarizing fields and the elastic energy associated with mechanical constraints to which the ferroelectric material is subjected as it is cooled through paraelectric–ferroelectric phase transition [1, 2-4]. Spontaneous polarization at the crystal surface can lead to the formation of a surface charge. This surface charge produces an electric field, called a depolarizing field E_d , which is oriented oppositely

to P_s (Figure 1.2). The depolarizing field will form whenever there is an inhomogeneous distribution of the spontaneous polarization, for example, due to the fall-off of the polarization near the surface of the ferroelectric (polarization is zero outside the ferroelectric and nonzero inside) or due to a change in the direction of polarization at grain boundaries. The depolarizing field may be very strong (on the order of MV m^{-1}) rendering the single-domain state of the ferroelectric energetically unfavorable [1, 2, 5] and change it into many domains.

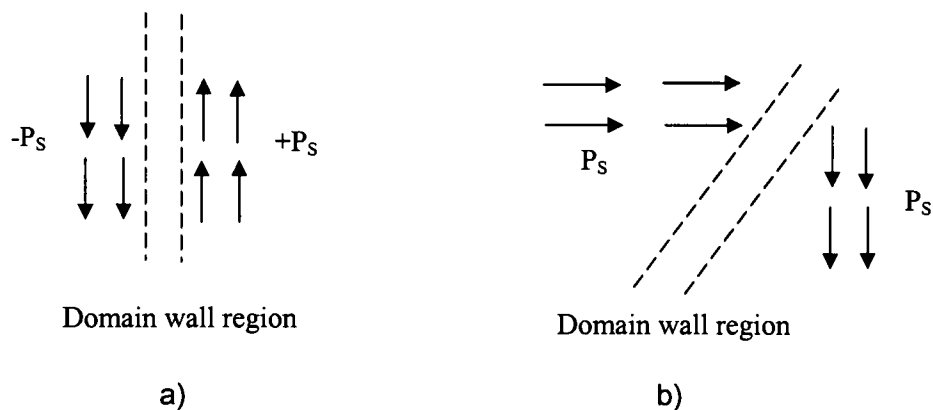


Figure 1.1. Illustration of (a) 180° and (b) 90° ferroelectric domains and domain-wall regions.

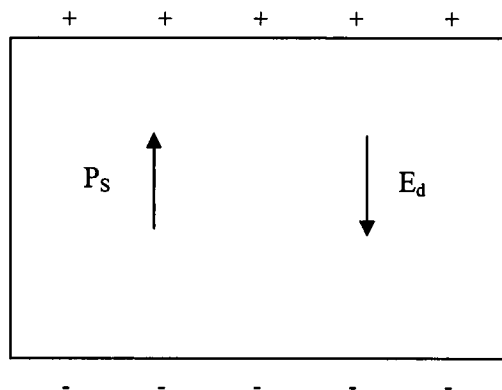


Figure 1.2. Formation of depolarizing field.

1.1.2 Hysteresis loop

The most important characteristic of ferroelectric materials is polarization reversal (or switching) by an electric field. One consequence of the domain-wall switching in ferroelectric materials is the occurrence of the ferroelectric hysteresis loop. The hysteresis loop can be observed experimentally by using a Sawyer–Tower circuit [6]. Figure 1.3 gives a typical FE hysteresis loop. It was simulated by the model given later in the dissertation. At small values of the AC electric field, the polarization increases linearly with the field amplitude. This corresponds to segment AB in Figure 1.3. In this region, the field is not strong enough to switch domains with the unfavorable direction of polarization. As the field is increased the polarization of domains with an unfavorable direction of polarization will start to switch in the direction of the field, rapidly increasing the measured charge density (segment BC). The polarization response in this region is strongly nonlinear. Once all the domains are aligned (point C) the polarization response again behaves linearly (segment CD). If the field strength starts to decrease, some domains will switch-back, but at zero field the polarization is nonzero (point E), resulting in a remnant polarization. To reach a zero polarization state the field must be reversed (point F). Further increase of the field in the negative direction will cause a new alignment of dipoles and saturation (point G) in the opposite direction. The field strength is then reduced to zero and reversed to complete the cycle. The value of polarization at zero field (point E) is called the remnant polarization, P_R . The field necessary to bring the polarization to zero is called the coercive field, E_C . The spontaneous polarization P_S is usually taken as the intercept of the polarization axis with the extrapolated linear segment CD (Strictly speaking, in polycrystalline materials true spontaneous polarization equal to that of a single crystal can never be reached and it is more correct to speak of saturated rather than of spontaneous polarization). It should be

mentioned that the coercive field E_C that is determined from the intercept of the hysteresis loop with the field axis is not an absolute threshold field [2]. If a low electric field is applied over a (very) long time period the polarization will eventually switch.

An ideal hysteresis loop is symmetrical so that $+E_C = -E_C$ and $+P_R = -P_R$. The coercive field, spontaneous and remnant polarization and shape of the loop may be affected by many factors including the thickness of the film, the presence of charged defects, mechanical stresses, preparation conditions, and thermal treatment.

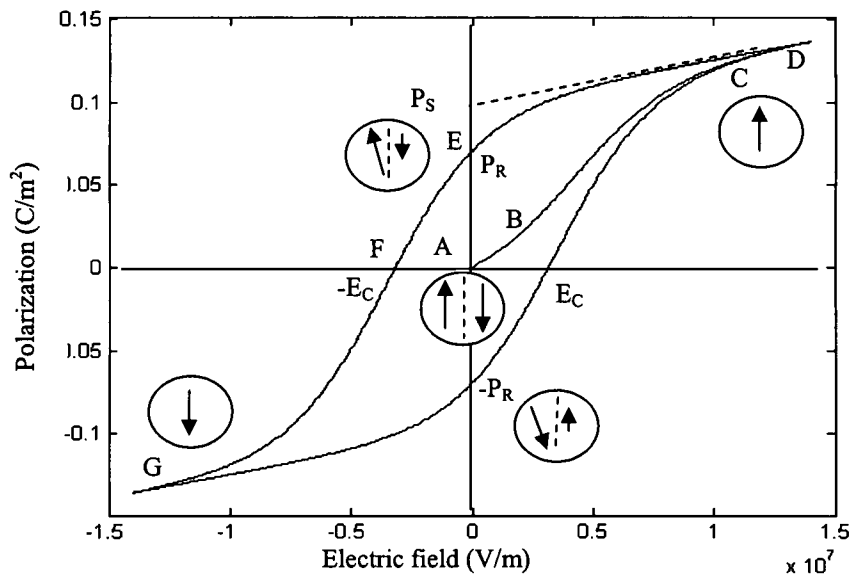


Figure 1.3. Ferroelectric P-E hysteresis loop. Circles with arrows represent the polarization state of the material at the indicated fields.

1.1.3 Polarization switching

Experimentally, the polarization switching of FE is usually studied using pulsed (for example square-wave form) signal. This has two advantages. First, the field is constant during switching. Second, this arrangement is similar to that used for memory applications. Assuming that the initial status of the FE has a remnant polarization of $-P_R$, when a strong field E is applied anti-parallel to the polarization of

the FE, the FE switches polarization from state $-P_R$ to $+P_R$. The measured switching current i is proportional to dP/dt and consists of two parts. One part is due to the fast linear response of the dielectric and the other part is due to polarization switching. The current follows the following expression:

$$\int_0^{t_s} i(t)dt = \epsilon_0 \epsilon E A + 2P_R A \quad (1.1)$$

where A is the area of electrodes and t_s is the switching time. Since the switching current decreases exponentially it is difficult to measure the total switching time, and t_s is usually taken as the value where current falls to $0.1I_{\max}$ [2].

The switching time can be expressed as

$$t_s = t_\infty e^{-\alpha E} \quad (1.2)$$

where α is the so-called activation field. At very high fields this relation changes to a power law of the form $t_\infty \propto E^{-n}$ where n depends on the material.

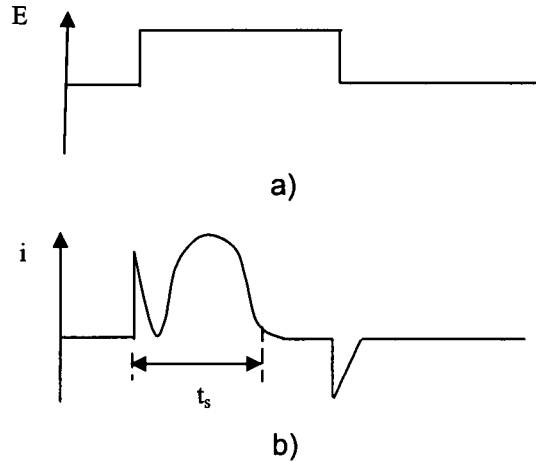


Figure 1.4. Switching and transient current during polarization switching. (a) Electrical field and (b) current as a function of time.

Constants α ; n ; t_∞ and i_∞ are temperature dependent. The switching time decreases as the Curie point is approached. The switching times on the order of tens of

nanoseconds were measured in $\text{Pb}(\text{Zr}, \text{Ti})\text{O}_3$ ferroelectric thin films [7]. Care is needed when experimentally determining the switching time because the electrical time constant of the measuring circuit must be short compared with t_s [4].

1.1.4 Permittivity–electric field (ϵ – E or C – V) loops

Dielectric permittivity versus electric field (or capacitance C versus voltage V) loops are often used in the characterization of ferroelectric materials. Typical behavior is introduced in chapter 5. There are two types of C – V curves related to FE. The first type is measured on a sample PZT capacitor. Measurements of ϵ – E (or C – V) curves are usually made by applying simultaneously on a sample a slowly sweeping DC field which changes as a step-like function and an AC voltage of relatively high frequency (1 kHz or above) and small amplitude. The AC voltage is used to measure the capacitance which is then plotted as a function of the DC bias field, giving a C – V graph. Initial rise in the permittivity with DC field is probably due to increased movement of the domain walls which become ‘free’ from defects which lock them at zero-DC field [8] and due to partial switching of some domains whose coercive field happens to be small enough and which can be switched by the DC +AC field combination. The maximum in the C – V curve appears in the vicinity of the coercive voltage for the P – V hysteresis when most of the domains switch and the material appear to be dielectrically very ‘soft’. At high DC fields, the permittivity decrease reflects two processes: (i) decrease in the number of domains as they become aligned with the field (ideally the sample becomes a single domain and only lattice contributions are present) and (ii) inhibition of the movement of residual domain walls by the DC field [8]. It is possible, however, that small oscillations or bending of residual domain walls under the AC field can still occur even at very large DC fields, contributing to the dielectric permittivity [9]. In any case, the total domain-

wall contribution to the permittivity at high DC bias becomes reduced with respect to the low DC bias fields.

Another way to obtain the C-V curve for FE is to plot the derivative of the P-V hysteresis loop ($\epsilon = \partial p / \partial V$). This hysteresis loop is measured with an alternate current (AC) signal which has a large amplitude and ($> V_C$) with the frequency on the order of 100 Hz. For the second type of C-V curve, the differential capacitance is plotted as a function of the instantaneous value of the AC signal with amplitude $> V_C$. The first type of capacitance is measured with a high-frequency AC field with sub-switching amplitude, applied in addition to the DC field, and plotted as a function of the DC field. The two types of C-V curves have different values, especially around the coercive voltage. They are similar only at saturating voltages, when polarization decreases from saturation towards a remnant value.

In both types of capacitance, there is a linear portion which is independent of the applied signal. The linear portion of FE permittivity is normally above a hundred.

1.1.5 Breakdown field

Breakdown field is an important parameter for device materials. At present day, electronic devices and integrated circuits (IC) are fabricated smaller and smaller. This give rise to the requirement on high breakdown materials since the electric field inside thinner films has higher values under the same applied voltage. It has been reported that the breakdown field strength for PZT is about 7.5×10^7 V/m [10]. A 0.25 μm thick PZT film can stand for about 18 V applied signal. In practice, the breakdown field is typically limited by the quality of the thin film processed, and it can be below 500 kV/cm. This makes FE attractive for device fabrication.

1.1.6 Antiferroelectrics

Antiferroelectrics (AFE) have different hysteresis loop from ferroelectrics. Figure 1.5 conceptually illustrates the typical P-V hysteresis of an AFE. Since the onset of the ferroelectric state and the return of the antiferroelectric state are normally fairly abrupt functions of bias voltage, the result is to give the typical double-loop hysteresis characteristics. This also gives rise to a special C-V curve as described in chapter 5.

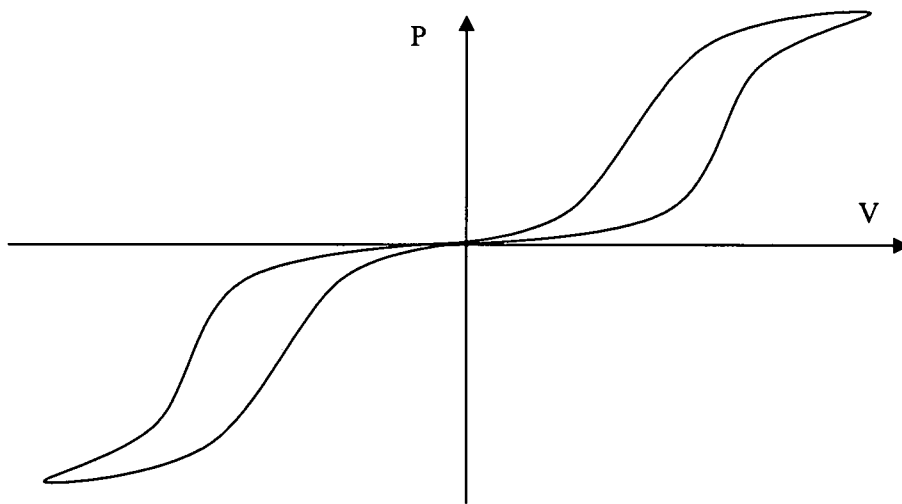


Figure 1.5. A typical hysteresis loop of antiferroelectrics.

1.1.7 Terminology related to FE/AFE

Ferroelectrics: A crystal which belongs to the pyroelectric family (i. e. shows a spontaneous electric polarization) and whose direction of spontaneous polarization can be reversed by an electric field.

Domains: The regions of a FE crystal with uniformly oriented spontaneous polarization.

Domain walls: The region between two domains.

Breakdown field: An electric field when a material starts to fail in electrical insulation.

Antiferroelectrics: A crystal whose structure can be considered as being composed of two sublattices polarized spontaneously in anti-parallel directions and in which a ferroelectric phase can be induced by applying an electric field.

1.2 Electromagnetic compatibility

Electromagnetic compatibility (EMC) is defined as [11] “the ability of a device, unit of equipment or system to function satisfactorily in its electromagnetic environment without introducing intolerable electromagnetic disturbances to anything in that environment”. The term EMC has two complementary aspects:

- It describes the ability of electrical and electronic systems to operate without interfering with other systems;
- It also describes the ability of such system to operate as intended within a specified electromagnetic environment.

Effective EMC requires that the system is designed, manufactured and tested with regard to its predicted operational electromagnetic environment: that is, the totality of electromagnetic phenomena existing at its location. Although the term “electromagnetic” tends to suggest an emphasis on high frequency field-related phenomena, in practice the definition of EMC encompasses all frequencies and coupling paths, from DC through main’s supply frequencies to radio frequencies and microwaves.

There are basically two classes of EMC requirements that are imposed on electronic systems:

1. Those mandated by governmental agencies.
2. Those imposed by the product manufacturer.

The requirements imposed by governmental agencies are legal requirements and generally cannot be waived. These requirements are imposed in order to control the interference produced by the product. However, compliance with these EMC requirements does not guarantee that the product will not cause interference. It only allows the country imposing the requirement to control the amount of "electromagnetic pollution" that the product generates. In order for the product to be marketed (advertised and sold) in a country, the product must comply with these requirements. On the other hand, EMC requirements are intended to result in customer satisfaction. They are imposed for the purpose of insuring a reliable, quality product. Maintaining a good reputation in the market is clearly of critical importance and compliance with both of the above EMC requirements is critical to the success of the product in the marketplace.

With the availability of rapid, global transportation and communication, the marketplace today encompasses the entire world. Consequently, the EMC requirements of all countries are of importance to manufacturers of electronic equipment.

Many EMC regulatory requirements e. g. FCC Part 15 and CISPR Publication 22 [12] have been issued. Each regulation has its own detailed requirements (equipment types, interference types, concerned frequency range, limits, test method, etc) on electronic equipment. Among them radiated emissions and conducted emissions are the interferences commonly considered. In the United States the Federal Communications Commission (FCC) is charged with the regulation of radio and wired communication. A significant part of that responsibility is to control interference from and to wired and radio (wireless) communication. The FCC Rules and Regulations contained in Title 47 of the Code of Federal Regulations have several parts that apply to non-licensed electrical equipment. Part 15 applies to

radio-frequency devices and the range of the radio-frequencies defined by the FCC extends from 9 kHz to 3000 GHz. A radio-frequency device is any device that is capable of emitting radio-frequency energy by radiation, conduction or other means whether intentionally or not. The purpose of Part 15 is to control the interference from these emitters. Under Part 15 the FCC set limits on the radiated and conducted emissions of a digital device. The FCC defines a digital device as

- Any unintentional radiator (device or system) that generates and uses timing pulses at a rate in excess of 9000 pulsed (cycles) per second and uses digital techniques.

Conducted emissions are those currents that are passed out through the unit's ac power cord and placed on the common power net, where they may radiate more efficiently due to the much larger expanse of this "antenna" and thus cause interference with other devices. The frequency range for radiated emissions extend from 450 kHz to 30 MHz. Compliance is verified by inserting a line impedance stabilization network (LISN) into the unit's ac power cord. Although the emission to be controlled is current passing out the AC line cord, the limits are given in volts. This is because the test device (LISN) measures a voltage that is directly related to the interference current. Radiated emissions concern the electric and magnetic fields radiated by the device that may be received by other electronic devices causing interference in those devices. The FCC requires measurement of only the radiated electric field and the regulatory limits are given in dB μ V/m. The frequency range for radiated emissions begins at 30 MHz and extends to 40 GHz. Compliance is verified by measuring the radiated electric fields of the product in either a semi-anechoic chamber or at an open-field test site. The radiated emissions must be measured with the measurement antenna in both the vertical and horizontal

polarizations with respect to the ground plane of the test site, and the product must comply for both polarizations.

Most radiated emissions and conducted emissions originate from current or voltage switching in components or circuits. At present, as the printed circuit board (PCB) manufacturing and assembly technology is developing rapidly, more and more components are assembled on PCBs. A main source of radiated electromagnetic interference (EMI) for many electronic products is the PCB. The design and layout of PCB have been identified as an important factor for EMI reduction [13-15]. Many papers concerning PCB radiation have been reported in the literature [16-20]. In addition to PCB design, integrated circuit (IC) design and package selection are other important factors for EMC. Modern technology has greatly increased the component density inside ICs. ICs' electromagnetic emissions (EME) can seriously degrade the EMC feature of electronic systems. The problem originates from the fact that radio-frequency (RF) signals generated inside an IC are routed out via IC pins to the surrounding PCBs and interconnected cables. The field radiated by these wiring structures, working as emitting antennas, contributes to the EME of the overall system. Steep currents and voltage glitches at the power supply and ground pins of the IC and proper signals at its input/output (I/O) pins are considered IC conducted emissions since they drive EMEs of antennas composed of PCB traces and/or interconnecting cables of the electronic system, which the IC is part of. Furthermore, pulsed currents flowing through IC package leads and circuits routed at silicon level excite IC direct radiations of interfering electromagnetic fields.

Radiated and conducted emissions from ICs heavily influence the EMC features of electronic equipment. Therefore, emission reduction on IC chip level is also very important. Standards regarding IC emission have come out. Measurement procedures for the radiated emissions from ICs can be found in reference 21. The

chapters 4 and 6 of International Electrotechnical Commission (IEC) document [22] describe, respectively, the 1 Ω /150 Ω direct coupling method and magnetic probe measurement method for the measurement of conducted emissions for ICs. Many studies about EMC design, tests and measurement on IC chip level have been carried out in the literature [23-25].

1.3 Introduction to capacitors, PCB and IC chip packaging

One common method for reducing conducted emissions is to insert filters where the power cord or track exits the product. Capacitors are potentially the easiest and cheapest way to solve many EMC problems. One of the best ways to assess if a capacitor is suitable for an application, with respect to frequency, is its impedance plot. This is a graph of the impedance between the terminals as a function of the applied frequency. The ideal capacitor equation would suggest that the impedance (Z_c) continues falling indefinitely and is dependant solely on the capacitance (C) for any applied frequency (f):

$$Z_c = \frac{1}{j2\pi fC} \quad (1.3)$$

The actual plot shows the effect of parasitic inductance (L_p) in that impedance eventually starts rising again. Hence the capacitor exhibits a self-resonance frequency. This is the frequency at which the parasitic inductance and the design capacitance have an equal reactance. Self-resonance frequency (f_0) can be calculated, if not quoted in the data sheet, as:

$$f_0 = \frac{1}{2\pi\sqrt{L_p C}} \quad (1.4)$$

On some capacitors the lowest value of the impedance plot is not limited by this self-resonance effects, but by the equivalent series resistance (ESR). The ESR is a figure for the effective short circuit ability of the dielectric. The ESR value for ceramic

dielectric is typically under 1Ω , often close to 0.1Ω or lower. Tantalum materials exhibit ESR in the $1\text{--}5\Omega$ range, with aluminum oxide dielectrics having higher ESR value up to 10Ω . The equivalent series resistance value limits the lowest value at which the impedance can fall to, and often disguises the actual self-resonance frequency. For best EMC performance it is important to have a low ESR value as this provides a higher attenuation to signal, especially frequencies close to the self-resonant frequency of the capacitor in use.

The equation for the impedance (Z) can be rewritten to include the parasitic inductive impedance (Z_L) and ESR value if a more detailed analysis is required:

$$Z = Z_L + Z_C + \text{ESR} = j2\pi fL_p - \frac{j}{2\pi fC} + \text{ESR} \quad (1.5)$$

It is generally the self-resonant frequency that limits the useful frequency range of a capacitor, hence the need to limit parasitic inductance. It can also be observed that a higher operating frequency range is obtained from lower value capacitors with the same dielectric and package type until limited by the dielectric material's frequency limit. One primary use of capacitors in many circuit designers is to act as a high frequency bypass source for switching demands. The bypass capacitors also tend to be used as supply voltage hold-up capacitors and act as a ripple filter to reduce the transient circuit demands on the power supply unit (PSU) directly from the local reservoir bypass capacitor. Bypass capacitors tend to be in the range of 10 to $470\mu\text{F}$ per PCB and circuit function. However capacitors with these values are not effective at the frequencies that are typically used for switching most digital ICs due to the self-resonance phenomenon. This is due to the fact that the bypass is primarily aimed at preventing the local supply from drooping by more than the allowable noise. The switching frequency noise needs decoupling to ground by a lower value capacitor, specifically employed to eliminate this higher frequency noise

and located as close as possible to the source of the noise (i.e. close to each IC or discrete circuit). Normally the decoupling capacitor has a value of approximately 1/100-1/1000 of the bypass capacitor.

When different values of capacitor, or different dielectric types, are connected in parallel (as with a bypass and supply decoupling capacitor) then another resonant mode can be introduced. Connecting capacitors in parallel is not necessarily a bad idea as it extends the operating frequency range of the capacitive effect (bypass or decoupling) as well as maintaining low impedance to a wide range of frequencies. However, due to phase interaction and multiple parasitic inductances between each capacitor, a third resonance mode called parallel resonance is introduced. These resonant modes will be present regardless of the choice of the capacitor.

The construction of a capacitor is to a certain extent similar for all types, especially there are two plates of metal with a sandwich of dielectric between them. It is the dielectric material used for charge storage that determines the capacitor's characteristics. The simplest and most efficient method of calculate the designed capacitor value is through the parallel plate capacitor equation:

$$C = \epsilon_0 \epsilon_r \frac{A}{d}, \quad (1.6)$$

where ϵ_0 is the dielectric constant of free space (8.854 pF/m), ϵ_r is the relative dielectric constant of the dielectric materials, A is the overlapping plate area and d is the distance between plates.

Design and layout of a PCB for EMC consideration is probably the most cost-effective measure. It is the most cost-effective as it requires no additional components, just the knowledge and experience of EMC layout methods and time spent in applying them. It may also lead to the reduction in filtering requirements, including the number of filters. Therefore, the application of correct PCB layout for

EMC could even reduce the cost of compliance.

A PCB is constructed from a series of laminates, tracking and prepreg layers in a vertical stack. Within the stack is often a series of drilled holes plated forming vias between tracking or plated through holes between surfaces. How these layers are stacked is dependent on the number of layers available for the design. Single-sided (i.e. one layer) boards do appear in very low-cost application. In the majority of modern circuits multi layer PCBs are often used due to the increasing assembly density.

The process of PCB manufacturing has tended to dictate existing common practices for PCB stack structure. The usual advice is to use a balanced stack that is symmetrical with respect to laminate and prepreg spacing. Symmetrical structure from the inner center out is also a common theme using equal thickness of laminates and prepreg with an even number of tracking layers and ground and supply planes. There are economical reasons for the use of even layers. The cost of three and four layers is almost equal; the benefit of an additional layer can be cost against a possible increase in packing density (i.e. reduced total board size), hence reduced cost per PCB in volume. In a stack, as the laminate can be metalized on both sides, the PCB stack consists of an even number of metalized layers.

There are some common guidelines for the structure of PCB layers. The surface layers are almost always tracking layers and rarely contain a plane, this makes sense from a circuit manufacturing viewpoint as it is impossible to test or debug buried tracking. In four-layer boards the outer layers are the tracking and the inner layers are often the power and ground planes. Where a third layer is required for interconnect on a four-layer board the power is sometimes given a routing pattern within the buried layer and signal tracking added to this layer, but the ground plane is retained. Where power planes are present it is common to have these adjacent to a

ground plane and to have tracking on the outside of these, tracking is rarely placed between ground and supply planes.

Since ICs are the primary noise of most emissions, the IC chip package is another important factor in EMC design. A chip package is a holder for the IC. It provides the mechanical, thermal and electrical connections necessary to properly interface the circuits to the system. The physical attributes of a package can typically be separated into three categories: the attachment of the die to the package, the on-package connections and the attachment of the package to the PCB. Two common methods of die attachment are used. One is the wire bond method in which the chip is mounted with the pads on top; the other is the flip chip method in which the chip is mounted with the pads on the bottom. The routing of the signals inside the package typically falls into two categories; controlled impedance and uncontrolled impedance. A controlled-impedance package typically resembles a miniature PCB with different layers and power and ground planes with a centered cavity used for die placement. The chip is usually attached with flip-chip bonding, although short wire bonds are often used. Uncontrolled-impedance package usually has wire bonds that connect the die directly to a lead frame, which is then soldered to the board. There are many ways to attach a package to the PCB. A lead frame is simply a metal frame that is integral to the package, which provides an electrical connection between the wire bonds and the PCB. It is either attached with a through-hole mount or a surface mount. A pin-grid array (PGA) consists of an array of pins that stick out of the bottom part of the package. A ball-grid array (BGA) is used to attach an IC to the PCB with an array of solder balls (a large version of flip-chip) and a land-grid array (LGA) permits direct electrical connection between a module substrate and a PCB.

CHAPTER 2

SCOPE OF THE DISSERTATION

2.1 Review of the literature

2.1.1 Noise reduction on PCBs and ICs

In present day, noise control is very important for the design of electrical/electronic components, PCBs and electrical/electronic systems. Besides EMC regulatory requirements, noise can cause delays or false switching as discussed in [26-32]. There are several kinds of noise, one of which is Delta-I noise. This noise consists of an unwanted voltage on the parasitic inductance of the power plane connections, caused by the transient currents associated with switching. Assuming a current change dI happens in a time interval of dt , it will generate a voltage of $V_N = L_{eff} \bullet dI/dt$ on the parasitic inductance with an equivalent value of L_{eff} . Delta-I noise can reduce the driver bias voltage [33]; in this case, the effect is called the ground bounce. Disturbances of several millivolts to 1 V have been reported. These disturbances may jeopardize the operation of sensitive integrated circuits on the printed circuit boards. As stated in [34], Delta-I noise waveforms typically consist of two components, an initial peak followed by a resonating waveform. The peak component has been studied by numerous authors [31] [35]. When the drive signals switch from one state to another, a transient current flows through the connections between the IC and the power planes. These transients excite a voltage

drop on parasitic inductances of the power/ground connections and results in peak noise, which is typically large and occurs for a short duration in comparison to the resonance component.

The development of modern IC and PCB technology is giving rise to increasing concerns regarding the ground bounce noise. Faster clock speeds and larger number of devices on a PCB (or in an IC) have resulted in increased ground-bounce noise in the power and ground planes. It is a critical and challenging design task to control the amount of delta-I noise that is inserted into the power planes.

Previous research on ground bounce noise can be divided into three types. The first type investigated the phenomena and mechanisms of the problem [36-42]. The second type worked on the estimation and prediction of the delta-I noise [43-46]. The third type concerned about the reduction of the delta-I noise. Many methods have been put forward to suppress power bus noise. Among them the design of the PCB and IC configurations is a method people can resort to [47-50].

Delta-I noise caused by power plane resonances in multilayer boards was described in reference [50]. First, the effect of power plane resonances on the ground bounce of the system was studied by performing finite-difference time-domain (FDTD) simulations. A. Kabbani et al simulated the voltage fluctuations at one point of the PCB due to a current surge between the power planes in a different point. Next, two methods to prevent this ground bounce effect were investigated. The first method consists of adding lumped capacitances to the design. The effect of one large capacitor was compared to the effect of adding a "wall" of smaller capacitors. A second approach was to isolate the chips by etching a slot around the sensitive integrated circuits and connecting both sides by a small inductor. Both methods provided excellent protection against power plane resonances.

Using capacitors is a convenient and efficient way to decouple the power ground noise. It can be divided into two types: discrete capacitor decoupling and embedded capacitor decoupling. In the existing literature, there are two techniques available [40] for the study of ground bounce. In the first method, the noise is attributed to inductive effects. The major sources of this inductance are said to be the leads by which the power planes are connected to the stabilized source, and the integrated circuit leads. The influence of the power planes is neglected as they are assumed to have a small inductance. This assumption is correct when the noise frequency is low. Under this assumption discrete capacitors are effective for the noise decoupling.

Once the noise frequency is high, it is reasonable to consider the power distribution system as a dynamic electromagnetic system in which the propagation effects are important. Thus, the power planes of a PCB or IC must be considered as a parallel plate waveguide system when working frequency is high. Much of the electromagnetic energy associated with the transients remains captured within the planes, which form a resonator. In this case embedded capacitors are effective for the noise decoupling [51-57]. Another advantage of embedded capacitor application is that it saves the assembly space required for the discrete capacitors.

2.1.2 Application of FE/AFE

At present, two properties give rise to the wide application of FE/AFE. The controllability of FE/AFE permittivity by DC bias is being widely used for tunable/reconfigurable circuits such as phase shifters, filters and voltage controlled oscillators [58-59]. The nonlinear dielectric tunability can be controlled by applied DC bias. Dr. Guru Subramanyam and his colleagues have demonstrated a novel ferroelectric varactor shunt switch for microwave applications [60-62]. In their

research, the nanostructured BaSrTiO₃ thin-film varactor shunt switches are controlled by a DC voltage. The normal switch state is OFF when a 0 V dc bias is applied and the switch is turned to ON by the application of a DC bias which reduces the loading varactor capacitance to a minimum. Another FE application is in memory circuit called ferroelectric random access memory (FRAM). A FRAM cell stores data in a capacitor that uses ferroelectric film as the dielectric material. The ferroelectric material is distinguished from other dielectric materials by the polarization-voltage (P-V) hysteresis loops. Although the data-storage element in FRAM is a capacitor, it does not store data as free charge. Instead, the position of atoms within the ferroelectric crystal represents the data [63].

An FE capacitor is characterized by capacitance that decreases with voltage and an AFE capacitor is characterized by the capacitance that increases with voltage and offers significantly-increased energy-density storage capability. AFE ceramic capacitors are receiving attention for application as selective energy storage devices in hybrid integrated power electronics as low-loss small-size passive components with large energy-density storage capability for voltage filtering and clamping protection against transient voltage spikes [64].

Both the capacitance of a discrete capacitor and the capacitance between power ground and planes in PCBs and IC chip packages are directly related to the dielectric constant of the dielectric materials used in the capacitors. Conventional dielectrics used in discrete capacitor and power bus typically have low values of relative dielectric permittivity ϵ_r (e.g. $\epsilon_r < 100$). In contrast, both FE and AFE normally have high (e.g. $\epsilon_r > 200$) values of relative dielectric permittivity and are expected to attain high-values of capacitance. This property makes AFE and FE attractive in the application of EMC decoupling. Although FE and AFE have been widely used in

radio frequency (RF) and memory devices, few articles are available regarding their EMC applications. Study in this dissertation is motivated by the idea and will concentrate on the AFE/FE applications on EMC decoupling.

As mentioned in Chapter 1, FE/AFE have special electrical properties due to their structures. Once these special properties are reflected in dielectric constant, the FE/AFE's dielectric constant depends on the many factors (e.g. frequency, field strength and thickness of the film). To successfully analyze the EMC decoupling effects of FE/AFE, we need to know the relationship between FE/AFE dielectric properties and the controlling factors. FE /AFE have been a research topic for a long time. Some researchers have explored EMC applications of FE/AFE. C. K. Campbell et al [64] studied the modeling of the experimental C–V response of a multilayer ceramic (MLC) antiferroelectric power-electric capacitor. Three conceptual series-connected capacitance regions within each grain and grain-boundary region of the MLC was considered. The equivalent capacitance component for the first region was derived from the voltage-dependent polarizations within a ferroelectric and/or anti-ferroelectric grain. This involved application of different Langevin functions for modeling the ferroelectric and antiferroelectric polarizations. The second region was related to the voltage and frequency dependence of the equivalent p-n junction capacitance at opposite sides of a grain-boundary and compensation-region, with Debye-type relaxation constants relating its frequency dependence. The third capacitance region was associated with the insulator-barrier region itself. Agreement between experimental and theoretical C–V responses was considered to be good, in view of the number of modeling parameters and variables employed.

The low-frequency dielectric relaxation of BaTiO₃ thin-film capacitors was reported by S. J. Lee et al [65]. O. G. Vendik et al [66] studied the dependence of the

dielectric constant of an incipient ferroelectric on temperature and the applied biasing field was modeled correctly by solution of the Ginsburg–Devonshire equation. In [67] the dielectric response of epitaxial BaTiO_3 thin films deposited on MgO was measured through surface electrodes as a function of applied bias, frequency, and temperature. The behavior of the dielectric response is attributed to the presence of residual strain in the epitaxial thin films. Authors used a Green's function technique to investigate the thickness and temperature dependence of the dielectric susceptibility of ferroelectric thin films in [68]. Depending on the interaction constants of the surface and on the bulk, the dielectric susceptibility can increase or decrease with the decrease in film thickness.

Through the use of relations analogous to that of the Rayleigh law, authors in reference [69] demonstrated that the ac electric field dependence of the permittivity of ferroelectric thin films can be described. Both reversible and irreversible components of the permittivity decrease linearly with the logarithm of the frequency of the ac field [69]. The results demonstrated that the models describing the interaction of domain walls and randomly distributed pinning centers in magnetic materials can be extended to the displacement of domain walls in ferroelectric thin films.

The structure of ferroelectric thin film capacitors is in the form of metal ferroelectric metal (MFM). Knowledge of its electrical characterizations is essential to the project. Electric field and relative dielectric constant are generally assumed to be uniform for bulk ferroelectrics. However, numerous experimental results for bulk ferroelectric properties are explainable by the existence of a surface layer of low dielectric constant material at the surface. This phenomenon has been described to be due to the existence of a surface layer of high electric field. It has been pointed out that the since the dielectric constant is highly nonlinear and field dependent, it would thus be

possible for the dielectric constant to vary within the material. In ferroelectric materials, however, the ionic part of the dielectric constant drastically decreases with increasing electric field due to the increasing stiffness of the perovskite lattice [70]. Many authors have adopted an approach which consists of considering ferroelectrics as insulators with two nonswitching dielectric layers, one adjacent to each electrode, each layer having the same thickness and a low relative dielectric constant. A physically based methodology for modeling the behavior of electrical circuits containing non-ideal ferroelectric capacitors was developed in reference [71]. The methodology was illustrated by modeling the discrete ferroelectric capacitor as a stacked dielectric structure, with switching ferroelectric and non-switching dielectric layers. Electrical properties of a modified Sawyer-Tower circuit were predicted by the model. Distortions of hysteresis loops due to resistive losses as a function of input signal frequency were accurately predicted by the model. The effect of signal amplitude variations predicted by the model agreed with the experimental data. The model was used as a diagnostic tool to demonstrate that cycling degradation, at least for the sample investigated, cannot be analyzed by the formation of non-switching dielectric layers or the formation of conductive regions near the electrodes, but is consistent with a spatially uniform reduction in the number of switching dipoles. The ferroelectric properties and fatigue of $\text{PbZr}_{0.51}\text{Ti}_{0.49}\text{O}_3$ (PZT) thin films of varying thickness were investigated using a blocking layer model in reference [72]. Ferroelectric capacitors having Pt bottom and top electrodes and a ferroelectric film of composition PZT were fabricated and investigated. The PZT films of thicknesses varying from 0.12 to 0.69 μm were prepared by organo-metallic chemical-vapor deposition. Annealed capacitors were investigated by capacitance, hysteresis, and pulse switching measurements. It is found that the thickness dependence of the reciprocal capacitance, the coercive voltage, and the polarization measured by pulse

switching can all be explained by a model in which a blocking layer is situated between the PZT film and an electrode.

A model for ferroelectric semiconductors based on the inhomogeneous Landau—Devonshire theory was developed in reference [70], including surface effects. The local electric field was determined by solving Poisson's equation in which a differential permittivity replaces the dielectric constant. The authors found that the hysteresis loops were strongly influenced by the correlation length. Based on their examination of the electric field, polarization, and differential permittivity profile inside the film, it was shown that the differential permittivity strongly decreased with the increasing correlation length. This phenomena leads to high electric fields inside the film and especially close to the surface. As a consequence, an explanation for thin film ferroelectric properties can be given by invoking space charge density many orders of magnitude lower than those usually considered.

2.2 Significance of the dissertation

The power within a printed circuit board (PCB) and some integrated circuit (IC) packages is distributed by means of power planes. These planes extend over the whole board. Two planes can be assumed to be present. One of them serves as the ground plane. The other serves as the power plane, which is at a positive potential with respect to the ground plane. At many points on the PCB, integrated circuits are connected to the power planes. The power and ground planes constitute a parallel plate waveguide. If there is a sudden change in current consumption at some point then one or more modes in this parallel-plate waveguide will be excited causing a voltage wave to propagate radially away from the excitation point. These voltage waves cause changes in the V_{cc} on the board. Four effects can be caused by the excitation. First, the switching can lead to a voltage drop at the switching chip

or die in a chip itself. This change can possibly result in false switching of the chip or die itself. Second, the propagated voltage wave can lead to malfunction of other IC's or dies at some distance from the excitation point, especially when these chips/dies are sensitive such as with clock chips/dies. Third, the excitation propagation on the planes will directly generate radiated emissions. Fourth, the excitation can propagate or be coupled to components and wires around the planes and generate radiated and conducted emissions.

In the frequency domain, these voltage drops are quantified by impedance

$$Z(r|r_0) = \frac{\Delta V(r)}{\Delta I(r_0)} \quad (2.1)$$

where $\Delta V(r)$ is the voltage drop between the planes at a position r due to a current excitation $\Delta I(r_0)$ at the excitation position r_0 . If r coincides with r_0 , then $Z(r|r_0)$ represents the internal impedance of the voltage source at the chip/die due to the power planes. On the other hand, if $r \neq r_0$, then $Z(r|r_0)$ is a transfer impedance. If the board would be of infinite extent, then the wave propagation would be radially symmetric. However, due to the finiteness of the board, the waves will reflect at the sides of the board. In this way, the finite parallel-plate waveguide can be seen as a flat resonating box with two perfectly conducting (PEC) walls (the power planes) and four imperfect walls (the sides of the board). Due to the mode mismatch between the waves inside dielectric mode and the free-space plane waves, the reflection coefficient at the imperfect walls will be considerable for most incidence angles. This means that the quality factor of the resonator will be considerable, which, in turn, means that the switching of a chip can cause oscillations in the voltages V_{cc} on the board. The resonant frequencies of the resonator will become apparent as extremes in the impedance.

From (2.1), it is clear that the power-bus voltage at one location r due to the current drawn by a component at another location r_0 is proportional to the transfer impedance $Z(r|r_0)$. At frequencies where power/ground planes are electrically small, the power-bus transfer impedance is equal to the power-bus input impedance. Since ferroelectric and anti-ferroelectric materials have high dielectric constants, a small size FE/AFE capacitor placed between the power bus is supposed to give small input impedance and therefore, generate lower ΔI noise. At higher frequencies, the transfer impedance depends on the location of the source and measurement ports, however, the ΔI noise measured at a position can still be reduced by placing a FE/AFE capacitor at the position.

Despite the high dielectric constant, FE and AFE have complicated properties. Their electrical performance depends on frequency, field strength, thickness of the film and the connecting circuits [73]. It is very useful to know the properties of FE and AFE and their effects on EMC decoupling.

The special property of FE is its hysteresis loop appearance when a periodic electric field is applied. This gives rise to nonlinear capacitance and makes its circuit application to be difficult to be predicted. Many researches regarding its electric performance have been conducted in the literature. Campbell modeled thick film ferroelectric capacitors in terms of series-capacitors [64, 74, 75]. The ferroelectric capacitance was given by a modified Langevin function, while the grain-boundary capacitances were modeled by back-to-back p-n junction diodes on either side of an insulator boundary. S. Sivasubramanian et al presented the circuit equivalent of the Landau-Khalatnikov dynamical ferroelectric model [76]. The size and shape of the simulated hysteretic loops depend strongly on the frequency and the amplitude of the driving electric field. L. Baudry studied the properties of thin film ferroelectrics based

on the phenomenological Landau-Denkovshire theory [70, 77, 78]. A two-dimensional lattice of dipoles is assumed to describe the film. Many analyses have assumed a uniform field distribution inside FE films [65, 71, 74-76]. However, two factors make dopant-ion charges often exist inside the film: The first is that some FEs has p-type (or n-type) conductivity themselves. It was reported that PZT has p-type conductivity [79]; the second is that intentional and unintentional doping during the processing of FE films often occur. Niobium has been reported to be an n-type dopant for PZT [80]. The metal-semiconductor-metal sandwich structure of capacitor can be considered as a back-to-back Schottky-barrier system and space charge will be generated in the FE thin film due to depletion effect. This charge will interfere with the otherwise uniform field distribution. Moreover, the nonlinearity and hysteretic performance of FE polarization will make the field distribution more complicated. All these effects will be reflected in the capacitor's internal field distribution and capacitance. The investigation of the effect of space charges thin film in FE/AFE on its electrical performance is essential to the application of thin film FE/AFE.

Hysteresis loop is a basic property of FE. Correctly understanding its property is very important to the application of thin film FE. Besides the effect on inside field distribution and FE's' capacitance, the space charges in thin film FE also affect its hysteresis loop. Clearing understanding the effect is importance to the application of thin film FE. Moreover; most researches in the literature have been focusing on the relationship between FE polarization and FE film material properties. The obtained hysteresis loops are for the isolated FE film and has no relationship with the connecting component and the shape is usually symmetric. Actual hysteresis loops are normally obtained by using a Sawyer-Tower circuit [71]. For many applications, FE material is used as thin film varactors in circuits. One potential application of FE

thin film is power-bus noise filtering because of its high dielectric constant. In this case the FE thin film can be used as either discrete or embedded capacitors. To correctly predict the performance of FE thin film in these applications, the interaction between the FE film and the circuit parameters have to be taken into consideration. S. L. Miller electrically modeled the FE thin film by dividing its polarization into linear polarization and switching polarization and analyzed FE thin film performance in ST circuit with different applied signal amplitude, FE leakage resistance and measurement input impedance [71]. These are considered as steady state analysis. In order to completely understand the practical hysteresis loop, FE film must be analyzed in ST circuit and transient analysis needs to be done.

Capacitance of ferroelectric films has been widely studied in literature. Campbell modeled thick film ferroelectric capacitors in terms of series-capacitance contributions from ferroelectric grains and grain boundaries [74-75]. The ferroelectric capacitance was given by a modified Langevin function, while the grain-boundary capacitances are modeled by back-to-back p-n junction diodes on either side of an insulator boundary. Francis K. Chai investigated the influence of doping concentration on the capacitance of thin film ferroelectrics [81, 82]. In all the analyses, the main portion of ferroelectrics capacitance was attributed to the polarization switching of ferroelectric domains, which play an important role on the hysteresis loops of ferroelectrics. One method to obtain the capacitance of FE films is to derive its hysteresis loops. This type of capacitance was widely used in the authors' analyses and it will be called large signal capacitance in this dissertation. In the meanwhile, the authors also did some capacitance measurements to verify their analyses. The measurements were made with small alternate current (AC) signal while slow sweep was made for the bias to get the C-V curves and the obtained capacitance will be called small signal capacitance. In fact this

measurement method has been widely used for the capacitance analysis of ferroelectric films in other places [83-84]. As mentioned in Chapter 1 that the capacitances obtained with these two methods have different values. Thin film FE can be used in many areas. In the application of memory, FE is basically used with large signals. In the application as a tuning device, FE is basically used with a small signal as the functional signal and a large bias as the tuning signal. In the EMC application as decoupling capacitors, FE films will work under a DC bias. The noise being dealt with can be small and can be large too. In order to correctly apply thin FE films, the relationship between the large signal and small signal capacitances needs to be addressed clearly and the mechanisms need to be investigated.

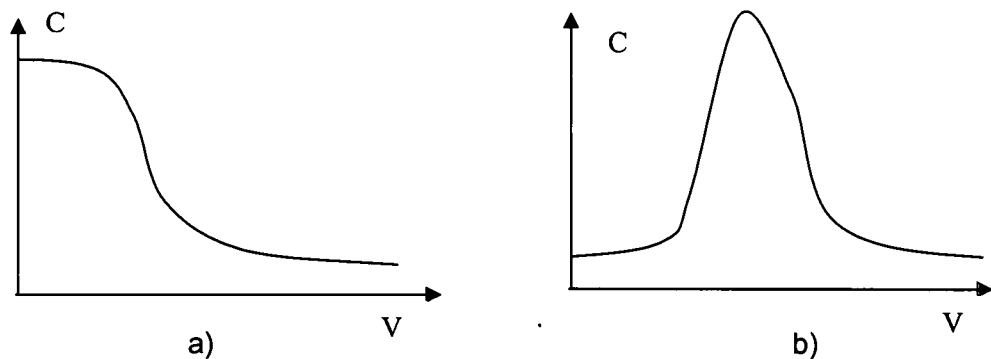


Figure 2.1. Illustrative C-V responses of: (a) ferroelectric and (b) antiferroelectric ceramic capacitors.

Due to high dielectric constant, FE/AFE capacitors are supposed to have much larger capacitance for a fixed size and much smaller size for a fix capacitance. This makes FE very attractive in EMC application as decoupling capacitors both in the discrete and embedded forms. In the application of EMC as decoupling capacitors FE/AFE are used with small signal. So the capacitance related to the application and analyses is small signal capacitance. Due to the material properties, FE and AFE have different C-V relationship. Generally, the capacitance of a ferroelectric

capacitor decreases with the bias voltage V . The capacitance of an AFE increases with voltage V at small values, reaches a maximum at a nonzero bias voltage V and then decreases with the bias voltage V . Figure 2.1 shows the typical C-V curves for FE and AFE capacitors. The special C-V relations will cause some special properties in the circuit application of thin film FE/AFE. In order to make proper use of FE/AFE in EMC application, their nonlinearity effects need to be analyzed.

Besides the capacitance nonlinearity, thin FE films have other special properties like interface layers. These factors also affect their performance in EMC application. A comprehensive study on the decoupling effects of thin film PZT capacitors needs to be conducted. Figure 2.2 gives a basic model of the circuit. It is an RC filter where R is an equivalent resistor and C is a decoupling capacitor. Numeric simulation and measurement based on circuit model will be carried out to compare the decoupling effects of AFE/FE capacitors with regular capacitor. Resonance effect will also be investigated.

The purpose of the study is to find the basic properties related to the hysteresis loop and capacitance of thin film FE/AFE, to compare the performance of FE/AFE capacitance decoupling with that of commercial off-the-shelf capacitors. The results shall provide valuable guidelines for the potential application of FE/AFE in EMC decoupling.

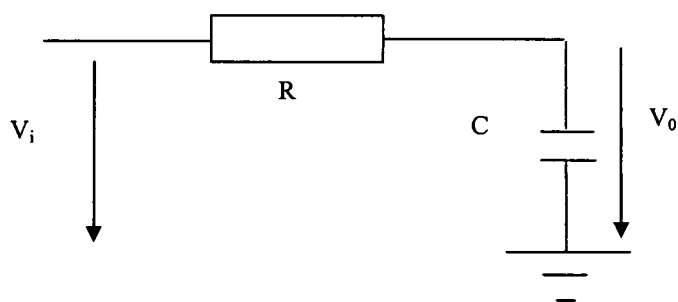


Figure 2.2. A decoupling circuit model.

2.3 The objectives of the study

Through the conduction of the study, the following objectives are going to be achieved:

- a. To Investigate the relationship between the space charge density of thin film FE and its hysteresis loop and capacitance.
- b. To investigate relationship between large signal capacitance and small signal capacitance.
- c. To investigate how the non-linearity of AFE/FE affect capacitors' decoupling effect.
- d. To investigate how the non-linearity of AFE/FE affect capacitors' resonance.
- e. To investigate the decoupling properties of discrete thin film FE capacitors.
- f. To provide better understanding for the application of FE/AFE in EMC.

2.4 The major contributions of the dissertation

The following contributions are made by the the dissertation:

- a. A mathematical model was developed to describe the relationship between the FE polariztion and applied electric field.
- b. The space charge are found to influence the electric field distribution in the FE thin films, its large signal capacitance and ideal hysteresis loop.
- c. The hysteresis loop of a thin film FE obtained with a ST circuit has initial offset due to remnant polarization and finally becomes symmetric due to the leakage effect to the measurement circuit and the FE itself.
- d. FE capacitance was found to be related with the applied signal amplitude. Small signal capacitace is much smaller than large signal capacitance and it is related to the transient domain switching behavior of FE.

- e. FE/AFE capacitance nonlinearity was found to affect the filtering effect, series/parallel resonance frequency and impedance.
- f. Thin film PZT capacitors are found to have a significant series resistance and it has effects on the decoupling effect and parallel resonance in EMC application. This resistance is thought to come from the interface layers between the FE film and the electrodes. This resistance is not found on the embedded BST film in varactors because BST is a paraelectric at room temperature.

The study provides a better understanding of electric properties of FE/AFE. The performance of circuits with FE/AFE can be effectively analyzed and predicted. It provides valuable results which improve the EMC application of FE/AFE.

2.5 Organization of the dissertation

Basic concepts about FE/AFE and EMC are given in Chapter 1. It is followed by a brief review on the research literature in delta noise reduction and FE/AFE application related to EMC. The study significance, objectives and contributions are also explained in Chapter 2. Chapter 3 introduces the models developed and used in this study. Designs and experimental setups are explained in chapter 4 and it is followed by the results and discussions given in chapter 5 and then by the summary and conclusions given in chapter 6. Finally; the scope for future work is given in chapter 7.

CHAPTER 3

MODELING OF THE THIN FILM FERROELECTRICS

3.1 A model for thin film FE with space charges

While the analyses of FE can be targeted at either thick films or thin films, the modeling methods for the two types of films have some difference. As mentioned before, besides the properties of ferroelectric grains itself, effects due to grain boundaries play an important role and need to be taken into consideration for the analysis of thick film FE. This project concentrates on the analyses of electrical properties of thin film FE. The structure is based on the capacitor samples from Radiant Inc and its thickness is typically about 0.25 μm . The samples were prepared by the sol-gel technique. Thin films made by high temperature processing typically have columnar growth which is continuous along the length of the columns. The FE is considered to have uniform physical properties along the thickness direction. The grain boundary effects considered in thick film analysis are ignored in this project.

In Figure 3.1a, the capacitor electrodes are assumed to be perfect conductors at $x=0$ and $x=t$. This structure is considered as a back-to-back Schottky-barrier system. For a thin FE film with a thickness about 0.25 μm it is reasonable to consider it is completely depleted [81] and the charge is uniformly distributed with a space charge density of $\rho = -N_A q$, where N_A is the doping (acceptor) concentration and $q = -1.6 \times 10^{-19}$ C is the elementary negative charge. In [85] the author model

ferroelectrics into lattices of dipoles. The method is suitable for thin film FE. In Figure 3.1b the PZT film is considered to be composed of many dipoles. Each dipole follows the Landau-Devonshire theory and has a P-E relationship [61, 77-78].

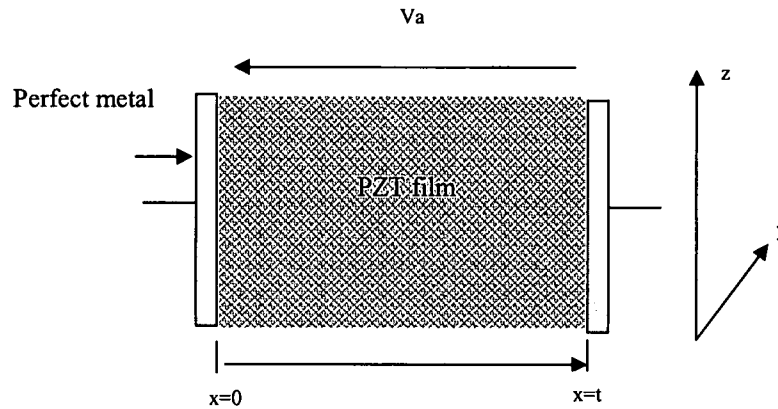


Figure 3.1a. A FE thin film capacitor with structure of metal-FE-metal.

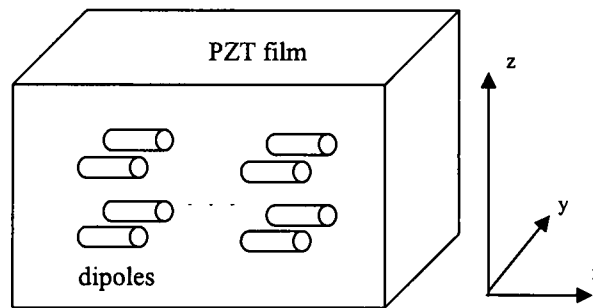


Figure 3.1b. A model of many layers of dipoles in a thin PZT film.

In order to get the hysteresis loop of the PZT film, the coupling between the dipoles, the effect of the space charge on the dipoles, the presence of grain boundaries or stress and the effect of the applied field on the dipoles need to be considered. The accurate results are to be obtained by solving the equations that consider all the effects with a three dimensional numerical method. Unfortunately, this method requires unreasonable computation time. To simplify the problem L. Baudry modeled a thin film metal-FE-metal structure into a two dimensional lattice comprising of many dipoles perpendicular to the electrode interfaces [70, 77-78].

The behavior of each dipole follows the Landau-Devonshire theory. Taking into consideration of the electrical coupling between each dipole, the author predicted the hysteresis loop of thin film FE with a two dimensional numerical method. In his method the two dimensional lattice of dipoles in the y-z plane was reduced to one dimensional lattice of the dipoles, Landau-Devonshire theory could no longer accurately describe the behavior of each dipole in his model. Furthermore, since the analyses was still based on a two dimensional numerical method, it has limitations on the physical explanations of results.

To make the analyses reasonable and easy to understand, a simple method has to be used. The Preisach model has been used to analyze ferromagnetics and ferroelectrics [86-87]. In [86] the author mentioned the mechanisms of the Preisach distribution in ferromagnetic systems which have some similarities to FEs. According to [87], there are two physical interpretations for the Preisach distribution in a thin film FE: (1) it could refer to a coercive field strength distribution of the FE dipoles, (2) or it could refer to the threshold voltage at which the independent domains inside switch. With the Preisach model, the coupling between the dipoles, the effect of space (defect) charge on the dipoles and the presence of grain boundaries or stress are considered by a distribution function of $f(E_{CN}^+, E_{CN}^-)$ in the Preisach plane, where E_{CN}^+ and E_{CN}^- stand for the coercive electric field for positive and negative switches of the dipoles and the function it indicates the ratio of the dipoles that have the values of E_{CN}^+ and E_{CN}^- . This method gives a mathematical description of the FE. But it lacks the function to investigate to physical mechanisms of many FE properties. In this paper a hybrid method is crested. Since the thickness effect of the thin film FE needs to be considered, the FE is modeled into many layers of dipoles in x direction as shown in Figure 3.1b. After using the

Preisach model to consider the different local environments of the dipoles, each layer is treated as an element film FE and has a related local hysteresis loop (P-E), where P and E stands for the local polarization of each layer and local electric field applied to each layer. Since the FE is assumed to have a uniform physical property along x direction, all the layers have the same saturated local hysteresis loops. For simplicity, the only considered local environments for each layer are the coupling between each layer and the effect of the space charges. When the applied signal is strong enough, every layer inside the FE will generate a saturated hysteresis loop and the FE will also generate a saturated hysteresis loop which is the only case considered in this paper. When the applied voltage increases or decreases, it is obvious that the polarizations of all the layers are in the decreasing or increasing process (refer to Figure. 3.1). The local field at each layer may be out of phase and can have different amplitude. But at the peak applied voltage, almost 100% of the dipoles are switched to one direction and each layer is in the linear section of its hysteresis loop.

As a summary, the following assumptions are made for the model development:

- a) The physical properties are uniform along the film thickness direction.
- b) The grain boundary effects are ignored.
- c) The electrodes are perfect conductors.
- d) Only saturated hysteresis loops are considered.
- e) Local environments for each layer the film are the coupling between each layer and the effect of the space charges.

It also needs to be pointed out that this method is a modified Preisach method. Instead of assuming a distribution of E_{CN}^+ and E_{CN}^- for the layers' hysteresis loops, the interactions between the layers are directly considered in the model. The

Preisach distribution of E_{CN}^+ and E_{CN}^- for the layers can be obtained from the simulation results as given in section 3.3.

The local polarization is expressed as the sum of the linear and the switching polarizations.

$$P_{total}(E_x) = P_{linear}(E_x) + P_{switching}(E_x), \quad (3.1)$$

where the linear polarization is expressed in terms of the linear dielectric constant ϵ_f as

$$P_{linear}(E_x) = \epsilon_0(\epsilon_f - 1)E_x \text{ and} \quad (3.2)$$

$$P_{switching}(E_x) = P_d^\pm(E_x). \quad (3.3)$$

In the absence of a fundamental physical theory which predicts dipole switching properties as a function of applied field, the switching polarization $P_{switch}^{+/-}(E)$ can be defined utilizing a convenient mathematical function whose behavior satisfies the physical requirement. A number of candidate functions exist, among them being the error function (an integral of a Gaussian distribution), the Langevin function encountered in magnetism, and the hyperbolic tangent function. The hyperbolic tangent function has convenient mathematical properties and has been shown to be consistent with experimental data. Many authors have used this function for the analysis of ferroelectrics [71, 81]. In this paper the hyperbolic tangent function is selected to describe the polarization and applied field relationship. The following mathematical descriptions come from reference [71].

The relationship between the applied field and the FE switching polarization is expressed for the right-hand half of the hysteresis loop as [71]

$$P_d^+(E) = P_s \tanh[E - E_c]/(2 * \delta), \quad (3.4)$$

where E is the local field in the FE film; E_c is the local coercive field; and δ can be expressed as [71]

$$\delta = E_c \{ \ln[(P_s + P_r)/(P_s - P_r)] \}^{-1}, \quad (3.5)$$

where P_r is the local remnant polarization and P_s is local the saturation polarization.

The left-hand half of the hysteresis loop can be expressed by [71]

$$P_d^-(E_x) = -P_d^+(-E_x). \quad (3.6)$$

The charge density (P) on the electrode at $x=0$ will be quantitatively equal to the displacement at $x=0$ and is given as

$$D(0) = \epsilon_0 \epsilon_f E(0) + P_d(x=0). \quad (3.7)$$

Assuming a uniform charge density ρ in the film, Poisson's equation gives the following expression:

$$D(x) - D(0) = \int_0^x \rho(z) dz, \quad (3.8)$$

where $D(x)$ is the electric displacement at position x and can be expressed as

$$D(x) = \epsilon_0 \epsilon_f E(x) + P_d(x). \quad (3.9)$$

With (3.4) and (3.6), one gets the following equation:

$$\epsilon_0 \epsilon_f [E(x) - E(0)] - P_s \left\{ \tanh\left[\frac{-E(x) - E_c}{2\delta}\right] - \tanh\left[\frac{-E(0) - E_c}{2\delta}\right] \right\} = \int_0^x \rho(z) dz = -qN_A x \quad (3.10)$$

for the increasing side of the hysteresis (E is reducing) loop and

$$\epsilon_0 \epsilon_f [E(x) - E(0)] + P_s \left\{ \tanh\left[\frac{E(x) - E_c}{2\delta}\right] - \tanh\left[\frac{E(0) - E_c}{2\delta}\right] \right\} = -qN_A x \quad (3.11)$$

for the decreasing side (E is rising) of the hysteresis loop. On the other hand, once a voltage V_a is applied over the film as indicated in Figure 3.1, one has the following expression

$$V_a = - \int_0^t E(x) dx. \quad (3.12)$$

The coupling between each layer and the effect of the space charge on each layer are embedded in (3.10)-(3.12). Once a value is given for V_a , (3.10) or (3.11) can be solved together with (3.12) by numerical methods so that field distribution $E(x)$ is obtained. $D(0)$ can be obtained by (3.7). Appendix 1 gives an example code in Matlab. In the code, for each given $E(0)$, a $E(x)$ distribution, a V_a and a large signal capacitance are obtained for the increasing and decreasing sides of the hysteresis loop separately.

3.2 Description for a bulk FE

Once a thin film FE is considered as a bulk, the inside field distribution and polarization are assumed to be uniform. Its hysteresis loop and its local hysteresis local are the same. (3.1)-(3.12) except for (3.8) can be used to express a bulk thin film FE and $E(x)$ can be replaced by V_a/t , where t is the FE film thickness.

3.3 Verification of the models

To verify the correctness of (3.1)-(3.6), measurements were performed on thin film capacitors from Radiant Technologies, Inc. The measured capacitor is made of undoped PZT (20/80) film with a thickness of 255 nm and area of $10000 \mu\text{m}^2$. The hysteresis loop as shown in Figure 3.2 was measured with a precision LC tester from Radiant Technologies, Inc. The parameters related to the thin film FE can be extracted with a curving fitting method. Appendix 2 gives an example code for that. Once the parameters are obtained, a new hysteresis loop can be calculated with (3.1)-(3.6). The FE parameters were extracted from the measurement as $P_r=27.54 \mu\text{C}/\text{cm}^2$, $P_s=27.55 \mu\text{C}/\text{cm}^2$, $\epsilon_r=540$ and $V_c=2.052 \text{ V}$. The hysteresis loop produced with these parameters is also given in Figure 3.2 and results agreed well with the measurement.

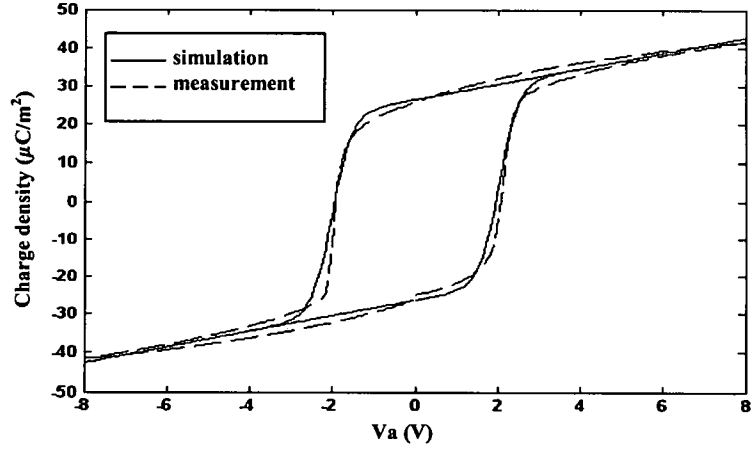


Figure 3.2. Hysteresis loops of a PZT (20/80) film with a thickness of 255 nm and an area of $10000 \mu\text{m}^2$.

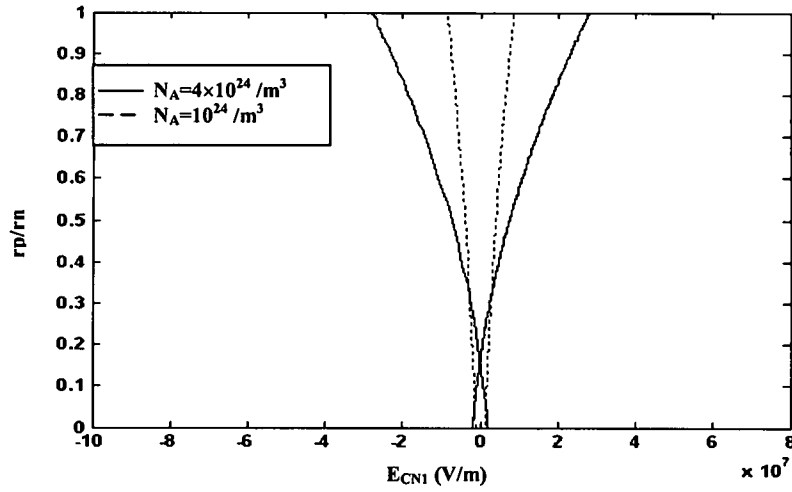


Figure 3.3. Normalized numbers of positively and negatively switched layers. Right curves indicate r_p and left curves indicate r_n .

To explain the relationship between the method presented here with the Preisach model, The distribution of the E_{CN}^+ and E_{CN}^- of the layers inside the thin film FE was investigated. For each decreasing V_a , there is a nominal applied electric field E_{CN1} , which is derived by dividing V_a by the film thickness. If the local field at a layer is stronger than the local coercive field, the layer is considered to be positively

switched. The normalized number of positively switched layers, r_p , is obtained as the ratio of the number of positively switched layers to the total number of the layers in the film. It has a relationship with the Preisach distribution as

$$r_p = \int_{-E_{CN1}}^{E_{CN1}} dE_{CN}^+ \int_{-\infty}^{+\infty} f(E_{CN}^+, E_{CN}^-) dE_{CN}^- .$$

In the same way, the normalized number of negatively switched layers can also be derived and expressed as

$$r_n = \int_{-E_{CN1}}^{+\infty} dE_{CN}^- \int_{-\infty}^{+\infty} f(E_{CN}^+, E_{CN}^-) dE_{CN}^+ .$$

Figure 3.3 gives curves of r_p and r_n for different doping densities. It shows the Preisach distribution changes with the doping density and this is consistent with the result that the doping density affects the field distribution in the FE. It is believed that the method presented in this paper does not have conflicts with the Preisach method. Instead, it is thought that the Preisach method is a statistic method used to simplify a problem when the problem is difficult to be modeled or the affecting parameters are difficult to be predicted.

3.4 The Landau-Khalatnikov circuit model

According to [78], a ferroelectric film can be assumed as an ensemble of dipoles. Each dipole can be described by the p^4 model in which the thermodynamic potential of one dipole is written as [78]

$$V_p = \frac{\alpha}{2} p^2 + \frac{\beta}{4} p^4 \quad (3.13)$$

Where p is the dipole's polarization, $\alpha = a(T - T_C)$, $a > 0$, $\beta > 0$, T is the temperature and T_C is the Curie temperature.

When an electric field e is applied to the dipole, its free energy F becomes [78]

$$F = V_p(p) - pe. \quad (3.14)$$

Assuming that the dipoles are embedded in a material that has viscosity, the motion of individual dipole moments will be delayed by the viscosity. The response of the

dipole to the applied field has a delay and can be described by using the Landau-Khalatnikov kinetic equation as [78]

$$\gamma \frac{dp}{dt} = - \frac{\partial F}{\partial p}, \quad (3.15)$$

where the γ is the viscosity coefficient and it determined the material's hysteresis loop response to frequency as shown in chapter 5.

In this study we are dealing with thin film FE. All the dipoles are assumed to have the same properties and the applied electric field in the film is assumed to be uniform. Therefore; the whole film can be considered to be one dipole. The above equations are still applicable to it.

Besides the contribution of the dipoles, the polarization of a thin FE film capacitor is also attributed to linear polarization of the material in the previous model for thin film FE with space charges and the permittivity related to the linear polarization is assumed to be ionic effect. In the Landau-Khalatnikov model the dipoles' polarization still has some response to high applied field. The significant portion of the linear polarization is actually not from ionic effect. It is still contributed by the dipoles. As to a thin film FE capacitor, it can be modeled into the circuit in Figure 3.4 [76]. C_0 represents the linear capacitance which is the geometry capacitance of the capacitor without the FE thin film and relates the charge to voltage ratio of the vacuum.

$$Q_0 = C_0 V. \quad (3.16)$$

C_F comes from its dipole polarization. R_S reflects the dipole viscosity of the film.

Assuming C_0 is very small, the FE film has an area of S and thickness of L , the Landau-Khalatnikov dynamical equation of the circuit in Figure 3.4 can be written as

$$-L \left[\alpha \left(\frac{Q}{S} \right) + \beta \left(\frac{Q}{S} \right)^3 \right] + V = R_S \frac{dQ}{dt}, \quad (3.17)$$

where Q is the charge on the capacitor.

Assuming the applied signal is periodic and is expressed as $V=V_0\sin(2\pi ft)$, where f is the signal frequency and V_0 is the signal amplitude, the equation can be changed into

$$\frac{dQ}{dt} = \frac{V_0 \sin(2\pi ft)}{R_S} - \frac{\alpha L}{R_S S} Q - \frac{\beta L}{R_S S^3} Q^3. \quad (3.18)$$

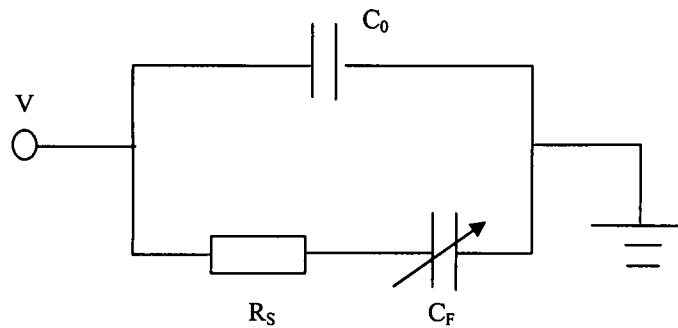


Figure 3.4. The equivalent circuit of a thin film FE capacitor.

CHAPTER 4

DESIGNS AND EXPERIMENTAL SETUPS

4.1 Designs

Measurements were conducted on two types of components. The first type is FE capacitors provided by Radiant Technologies, Inc. These capacitors were composed of 20/80 PZT film ($\text{Pb}(\text{Zr}_{0.2}\text{Ti}_{0.8})\text{O}_3$). Two types of capacitors were used in this project. The film in type AA is 0.27 nm thick and 4% niobium doped. The film in type AB was 0.255 nm thick and undoped. The capacitors in each type have different areas. Figure 4.1 shows the package of the capacitors. Each die is packaged in a four-lead TO-18 header. One lead connects to the case and is labeled as GND. The common lead is connected to Pin 1. The two independent leads from the two capacitors are connected to Pins 2 and 4.

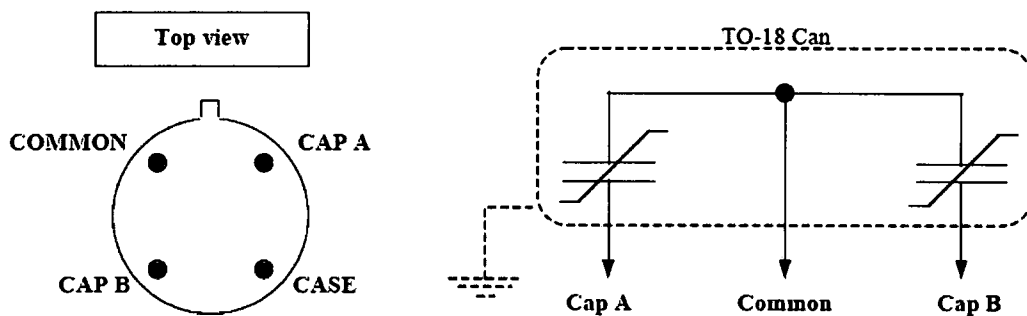


Figure 4.1. Package of thin film FE capacitors

The second type is the capacitive shunt switches shown in Figure 4.2. They are designed using coplanar waveguide (CPW) transmission lines on a high resistivity Si

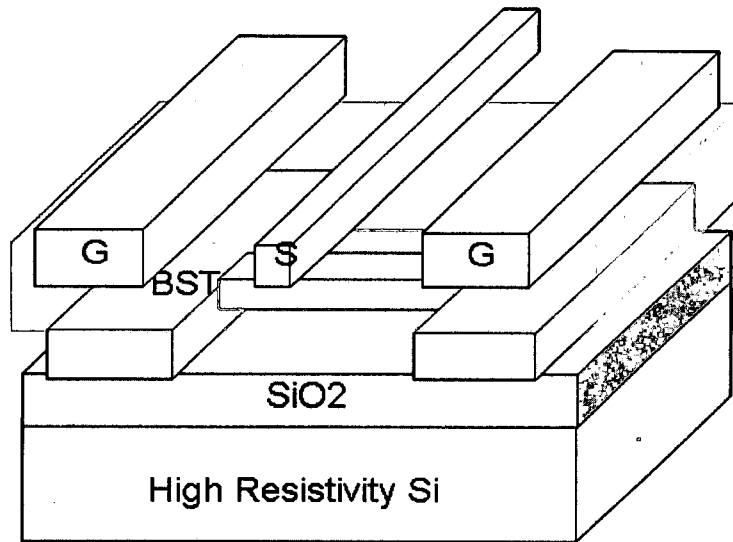


Figure 4.2. Three-dimensional view of the varactor shunt switch showing the varactor and the large ground-pad capacitance.

substrate ($>6 \text{ k}\Omega$) with a thin SiO_2 isolation layer. The thickness of the $\text{Ba}_{0.6}\text{Sr}_{0.4}\text{TiO}_3$ (BST) layer, substrate and SiO_2 layer are $20 \text{ }\mu\text{m}$, $20 \text{ }\mu\text{m}$ and $0.25 \text{ }\mu\text{m}$ respectively. In this study, we designed and fabricated devices with different varactor areas: $5 \times 5 \text{ }\mu\text{m}^2$ and $20 \times 20 \text{ }\mu\text{m}^2$. The CPW ground-signal-ground dimensions were $200 \text{ }\mu\text{m}/50 \text{ }\mu\text{m}/200 \text{ }\mu\text{m}$ on the high-resistivity silicon substrate so as to obtain characteristic impedance close to $50 \text{ }\Omega$ over the range of dielectric tunability. The overall length of each switch is $500 \text{ }\mu\text{m}$ and the overall width is $550 \text{ }\mu\text{m}$. The device requires two metal-layer processes, with the BST layer between the metal1 and metal2 layers. The metal2 layer contains the probeable CPW line for on-wafer probe measurements. Both metal1 and metal2 layers contain the ground lines, resulting in large ground-pad capacitors due to the sandwiched BST layer. In addition, the metal1 layer contains a shunt line connecting the two ground lines. As shown in Figure 4.2, a parallel-plate varactor is created between the shunt line in the metal1 layer and the center conductor in the metal2 layer. The varactor capacitance is

essentially in series with the larger ground-pad capacitance, thus resulting in an effective capacitance of the varactor. The shunt conductances of the large ground-pad capacitors, as well as the varactor, eliminate any need for via holes, hence resulting in a simple process. The important device parameters are (i) the varactor area (overlap area of the metal1 and metal2 layers), (ii) CPW transmission line parameters, (iii) parasitic inductance and resistance of the thin-line shunting to ground in metal1, and (iv) the dielectric properties of the nanostructured BST thin-film.

4.2 Measurement setups

Measurements about the thin film FE capacitors were conducted on the following parameters: small signal capacitance, hysteresis loop, insertion loss and impedance. The measurement setup for each parameter is addressed in this chapter.

4.2.1 Small signal capacitance measurement setup

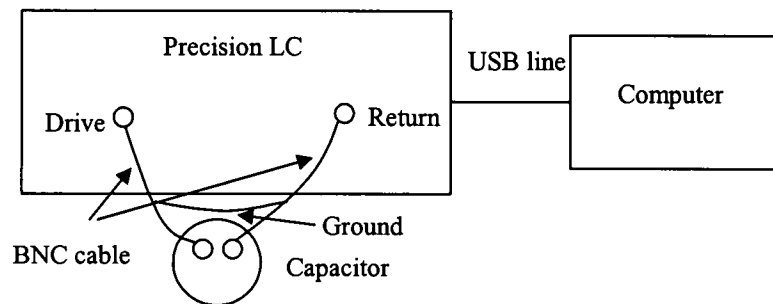


Figure 4.3. Setup for small signal capacitance and hysteresis loop measurement with a precision LC tester.

Three methods were used in this project to measure the capacitance of a thin film FE capacitor. Figure 4.3 gives the block diagram for capacitance measurement with a precision LC tester from Radiant Technologies. One pin of the measured capacitor

is connected to the Drive port and another pin is connected to the Return port. The

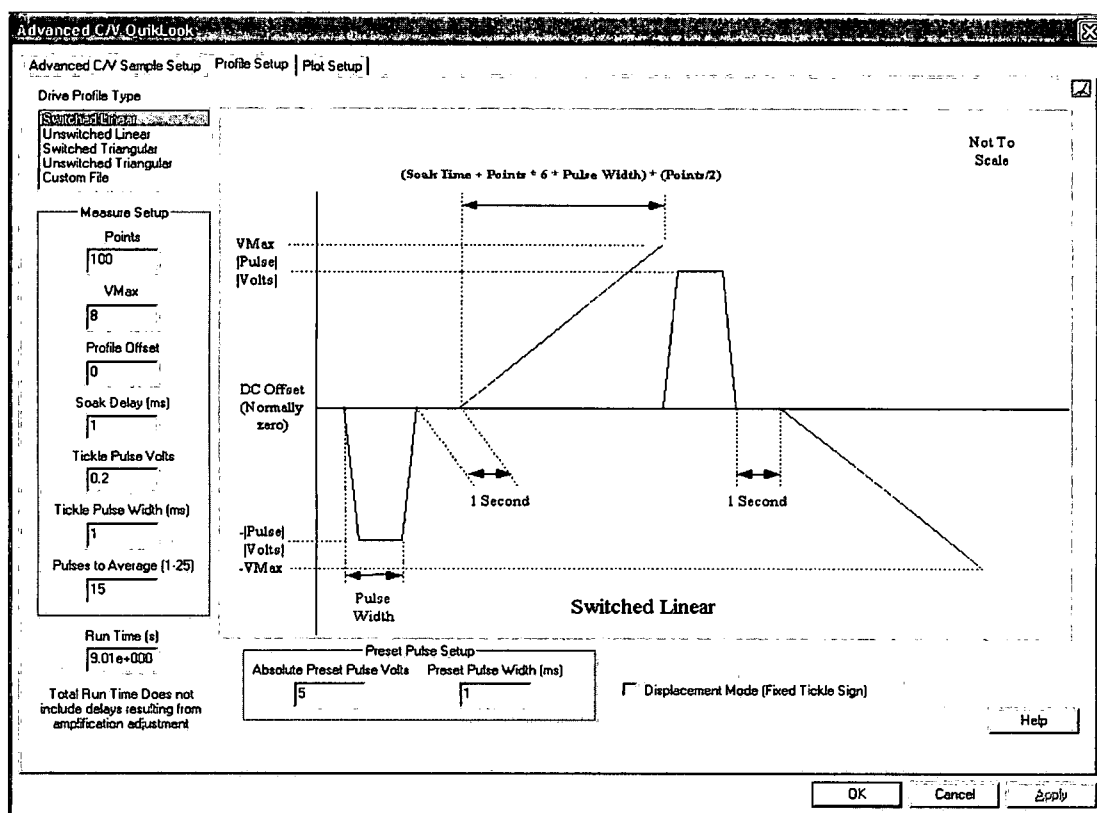


Figure 4.4. C/V measurement profile setup.

ground of the two BNC connection cables can be connected together. The RADIANT precision LC tester is a compact and effective tester for non-linear capacitors. It is versatile and capable of executing a variety of tasks including hysteresis loop measurement, small signal CV, IV, leakage current, remanent hysteresis, fatigue, imprint, retention, voltage breakdown, piezoelectric displacement, and others. The basic hysteresis measurements are conducted by changing the voltage on the sample. It uses a virtual ground input for the charge measurement. A hardware integrator behind the virtual ground is used to collect the charge generated by the test waveform. This integrator is an electrical circuit that counts the number of electrons that enter or exit its input. It outputs a voltage proportional to the total count of electrons for measurement. At every measurement, the charge on the

integrator and the voltage across the sample are measured at the same time. From them the C-V can be calculated. The tester is connected to a computer through a USB cable and measurements were controlled by the computer software Vision. The DC bias voltage profile, the measuring pulse amplitude/width, measuring points and number of measuring pulses at each point can be set as show in Figure 4.4. Results can be collected in both graph and test forms.

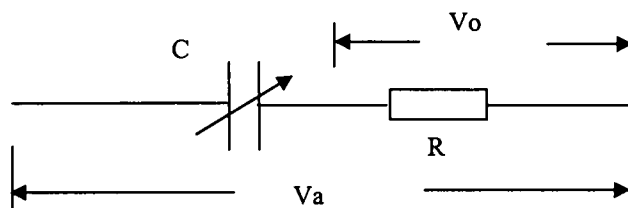


Figure 4.5. RC Circuit used for small capacitance measurement.

Figure 4.5 shows another method for small signal capacitance measurement. A 100 Ω resistor R was connected in series with the measured thin film FE capacitor C. Once the resistance of R is much smaller than the impedance of C, the voltage V_o , in proportion to the circuit current, directly reflects the capacitance of C. The capacitance C can be expressed as

$$C = \frac{V_o}{\frac{dV_a}{dt} R} \quad (4.1)$$

The input signal V_a was triangle wave and was provided by a Tektronix arbitrary function generator AFG310. Both V_a and V_o were measured with Tektronix oscilloscope TDS7254B.

Small signal capacitance was also measured by a Hewlett Packard precision LCR meter 4284A. The Hewlett Packard Kelvin clip leads was used and the measured capacitor's pins were clamped to it. The AC measured signal frequency amplitude and DC bias can be set on the panel.

4.2.2 Hysteresis loop measurement setup

Two methods were used in this project to measure the hysteresis loop of thin film FE capacitor. The first method is by a precision LC tester from Radiant Technologies. The setup is given in Figure 4.3 and is the same as for small capacitance measurement. During measurement, the Vision software shall be correctly set for hysteresis loop measurement. The measurement signal amplitude and frequency can be set as shown in Figure 4.6. Results can be obtained in both graph and text forms.

Hysteresis QuikLook Measurement Setup | QuikLook Plot Setup

Hysteresis Task Name: Hyst-1

VMax: 1

Hyst Offset: 0

Hysteresis Period (ms): 10

Pre-Loop Delay (ms): 1000

Voltage Range: Internal Amplifier ±100.0 Volts

External Amplifier: ± 500 Volts

Drive Profile Type: Standard Bipolar

Area (cm2): 0.0001

Thickness (μm): 0.3

Sample Name (24 Characters Max.):

Lot ID (12 Characters Max.):

Wafer ID (12 Characters Max.):

Die Row: 0

Die Column: 0

Capacitor Number: 0

Multi-Channel Options:

Sensor Enable: ☒ Sensor Scale: 1 Sensor Offset: 0 Sensor Label: 50 Sensor Impedance: 50

Sensor Data = Sensed Voltage * ((Input Impedance + Sensor Impedance) / Input Impedance) * Scale + Offset

Preset Loop: ☒ Start with Last Amp Value: ☒ Auto Amplification: ☒

Amp. Level: 100.0

Drive Channel: 0 Return Channel: 0

Drive Port: 0 Return Port: 0

Enable Ref. Cap: 1nF ±0.1% (Max = 30 Volts) Enable Ref. Resistor: 2.5 M-Ohm ±0.1% (Max = 100 Volts)

Drive Closed: ☒ Return Closed: ☒

Help

RADIANT TECHNOLOGIES, INC. FERROELECTRIC TEST SYSTEMS

Hysteresis Version: 3.1.1 - Radiant Technologies, Inc., 2000 - 12/12/05

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Figure 4.6. Parameter setup for hysteresis loop measurement.

Another method for hysteresis loop measurement is by a ST circuit [6]. Figure 4.7 show the diagram for the setup. The input signal V_i was provided by a Tektronix arbitrary function generator AFG310. Both V_i and V_o were measured by a Tektronix

oscilloscope TDS7254B. Its nominal input impedance is $1\text{M}\Omega$. Once the normal capacitor has a much smaller capacitance than the measured FE capacitor, the measured V_o directly reflects the charge on the FE capacitor as $Q=V_o \cdot C_n$. The resistor value can be changed for leakage current investigation. All the components were mounted on a breadboard. The AFG 310 generator can be set to generate either a continuous or short time signal. The amplitude, frequency and waveform can be configured. If the hysteresis loop wants to be displayed on the oscilloscope, the two input channels need be set in X-Y mode. The results can also be saved into a text file.

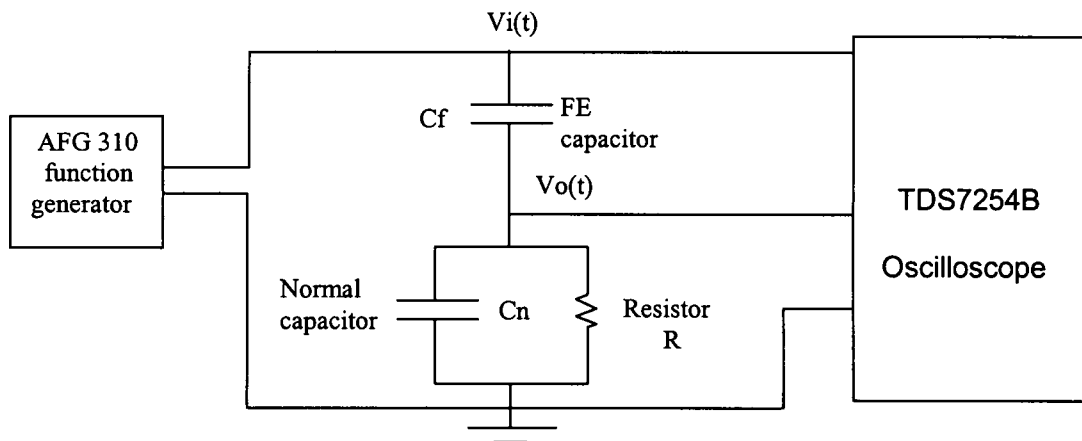


Figure 4.7. Hysteresis loop measurement with a ST circuit.

4.2.3 Insertion loss measurement setup

A fixture as shown in Figure 4.8 was built for insertion loss measurement. It includes a small printed circuit board on which a 6 pin DIP integrated circuit socket, a right angle BNC jack for input signal and a right angle BNC jack for output signal were mounted. During measurement the selected capacitor was plugged into the IC socket so that it works as a shunt capacitor to produce filtering effect.

Figure 4.9 shows the experimental diagram for the measurement of decoupling effect of FE capacitors. Signal V_s was generated from a Rohde & Schwarz signal

generator SML01 with a $50\ \Omega$ output impedance and input into a $50\ \Omega$ cable. This cable is connected to the input BNC jack of the fixture shown in Figure 4.8. The output signal is measured by a Rohde & Schwarz power meter URV5 which has an input impedance of $50\ \Omega$. The system was controlled by a computer so that automatic measurement could be made by sweeping frequency. Insertion loss is determined by values measured with and without the decoupling capacitor.

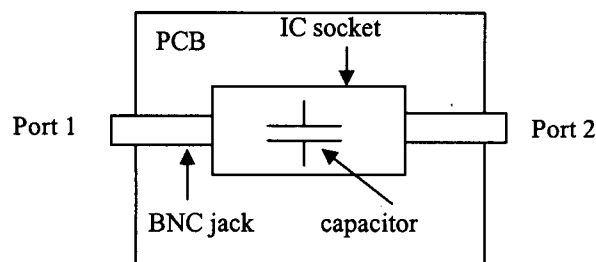


Figure 4.8. The fixture for insertion loss measurement.

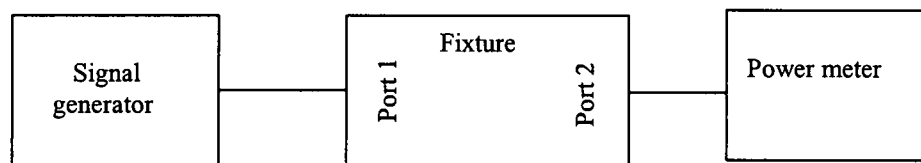


Figure 4.9. The diagram for insertion loss measurement setup.

4.2.4 Impedance measurement setup

A fixture as shown in Figure 4.10 was built for impedance measurement. It includes a small PCB on which a 6 pin DIP IC socket and a right angle BNC jack for input signal were mounted. During measurement the selected capacitors were plugged into the IC socket so that they work as a termination load to give reflection.

Impedances were obtained from the S_{11} parameter measured with a network analyzer HP8253C connected with a S parameter test set HP85046A. Figure 4.11 shows the diagram for the setup. Port 1 on HP85046A was connected to the input of the fixture through a $50\ \Omega$ cable. One port measurements were carried out and

calibration was conducted for S_{11} parameter before measurement. The calibration was made with an SMA cable and SMA jigs. During measurement a SMA to BNC adaptor was used to connect the output cable of the network analyzer with the input BNC jack of the fixture. The total length of the BNC jack and the SMA to BNC adaptor was measured to be 7 cm. This length was later compensated for in the impedance calculation. Once S_{11} parameters were obtained the component impedance was calculated. The measurement was controlled by a Visual Basic program through a GPIB cable. All the measurement amplitude and phase data can be recorded.

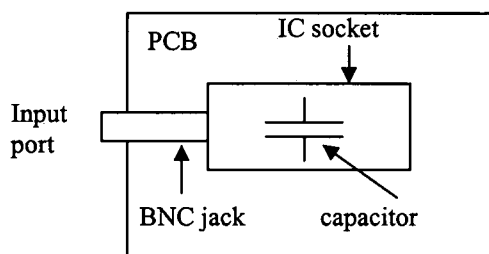


Figure 4.10. The fixture for impedance measurement.

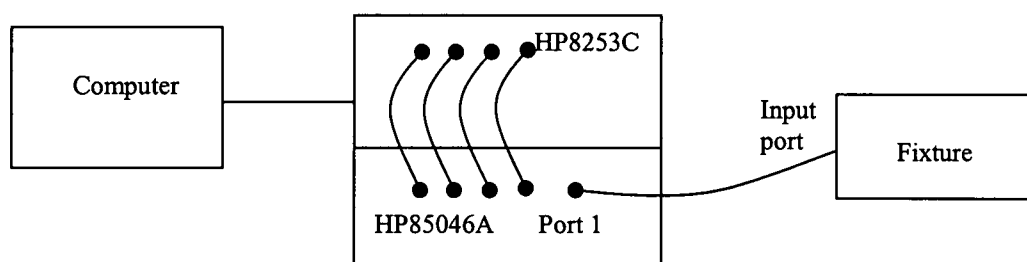


Figure 4.11. The diagram for impedance measurement.

4.2.5 Measurement setup for the S parameter of varactor shunt switches

For S parameter measurements, the varactor shunt switches were measured using an HP 8510 vector network analyzer (VNA), with a line-reflect-reflect-match (LRRM) calibration done over a wide frequency range (0.1 to 20 GHz). The samples were

probed using standard GSG probes, with the dc bias applied through the bias tee of the VNA. The setup is given in Figure 4.12.

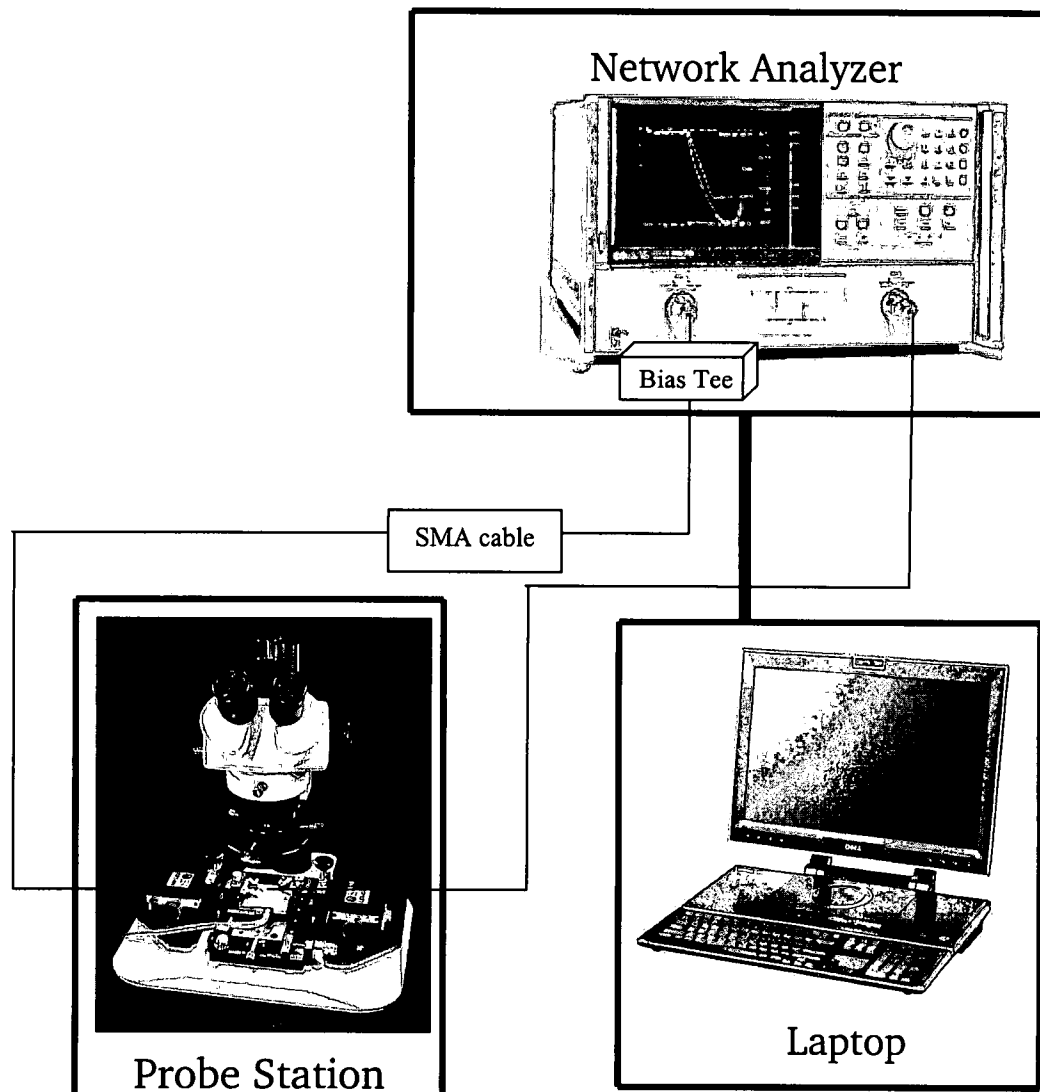


Figure 4.12. The setup for S parameter measurement.

CHAPTER 5

RESULTS AND DISCUSSIONS

To achieve the objectives set for this dissertation, measurements, simulations and analyses were conducted regarding the electric field distribution inside the ferroelectric thin film, capacitance, hysteresis loops and EMC applications of FE/AFE. They are addressed in this chapter.

5.1 PERFORMANCE OF THIN FILM FERROELECTRICS WITH DOPANT-ION CHARGES

5.1.1 Electric Field Distribution

Based on the model given in chapter 3, the electric field distribution can be obtained if the required parameters are given. Figure 5.1.1 and 5.1.2 give some examples of the field distribution in thin film FE with uniform charge density. In these simulations, the material parameters are given as: $P_s=0.1 \text{ C/m}^2$, $\delta=2000000 \text{ V/m}$, $E_c=3500000 \text{ V/m}$ and $\epsilon_f=350$. Simulations show that field distributions depend on both the charge density and applied voltage. Generally speaking, higher charge density in the film increases the non-linearity of the field distribution. Field non-linearity becomes obvious when the electric field strength is close to coercive field. Once the applied voltage is high enough to make the local field at all the portions much stronger than the coercive field, the field distribution is almost linear. This phenomenon is consistent with the model of the FE. When the field is close to the

coercive field, switching polarization will be very sensitive to the electric field and plays an important role on the field distribution. Therefore, more non-linearity will be observed. Once the field is much higher than the coercive field, the switching polarization will be saturated, therefore, only the linear polarization will be contributing to the distribution and linear field distribution will be observed. FE polarization comprises of switching and linear polarizations. Switching polarization contributes to nonlinear field distribution while linear polarization causes linear field distribution. In FE these two factors work together to give the field distribution. To understand how these two factors work together, the FE field distribution with different ϵ_r were investigated. Figure 5.1.3 gives the field distribution in a FE with the same switching parameters as in Figure 5.1.1 except for the varying linear dielectric constant. The applied voltage for all the three cases is $V_a = -1.4$ V. Results show that the non-linearity of FE field distribution increases with the decrease of ϵ_r . This result is consistent with the model described in 3.1. Increasing ϵ_r increases the contribution of the linear polarization and therefore increase the linearity of the field distribution.

Analyses show that the field distribution curve can be divided into two segments. One segment corresponds to the condition of $|P_{\text{linear}}(E_x)| > |P_{\text{switching}}(E_x)|$ and linearity dominates the field distribution. Another segment corresponds to the condition of $|P_{\text{linear}}(E_x)| < |P_{\text{switching}}(E_x)|$ where non-linearity dominates. When the film thickness is given, all the parameters as N_A , V_a and ϵ_r affect the junction point position of the two segments. Some times this connection points can move out of the whole film so that only one type of field distribution will appear: linear field distribution is contributed to by linear polarization or non-linear field distribution is contributed to by switching polarization.

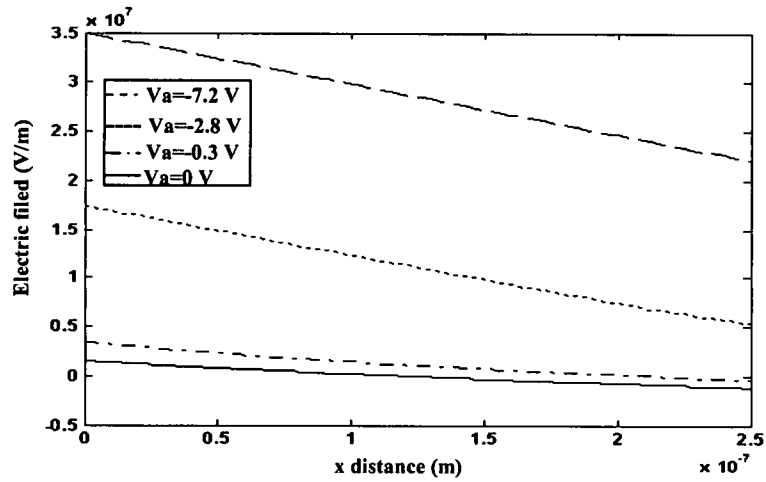


Figure 5.1.1 Field distribution with different applied voltage for FE with $N_A=10^{24}$ / m^3 .

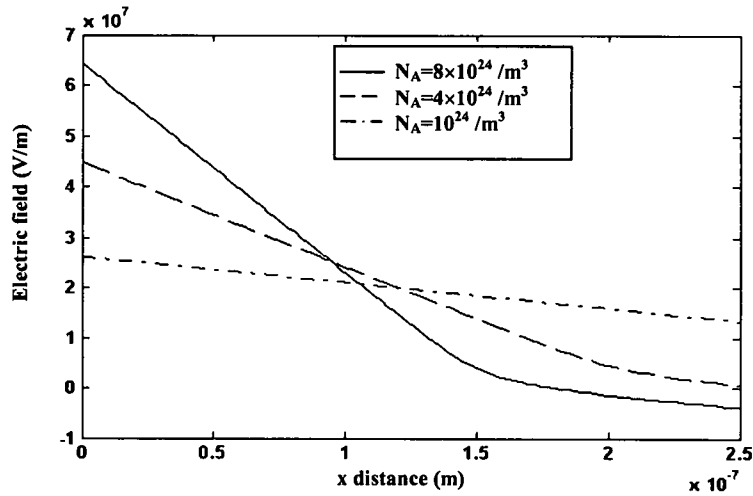


Figure 5.1.2. Field distribution for FE film with $V_a=-5$ V.

Further simulation shows that for the extreme case of $\epsilon_r=1$ the field is very strong near the left electrode ($x=0$). The result of slightly increasing the value of V_a is a huge increase of electric field at around $x=0$ and very little change of electric field at other places, especially when x approaches the other electrode. This phenomenon needs to be considered for the application of FE films. According to Figure 5.1.3, the field strength at $x=0$ for $V_a=-1.4$ V and $\epsilon_r=1$ is 1.75×10^8 V/m. It has been

reported that the breakdown field strength for PZT is about 7.5×10^7 V/m. In this case the film will be broken down before the applied voltage reaches -1.4 V, even though the applied voltage is small.

An analytical model is developed for the extreme case when ϵ_f is very small. In this situation, let us ignore the effect of linear polarization. Equation (3.10) becomes

$$P_s \left\{ \tanh\left[\frac{E(x) + E_c}{2\delta}\right] - \tanh\left[\frac{E(0) + E_c}{2\delta}\right] \right\} = -qN_A x. \quad (5.1.1)$$

$$\text{Let } k = \tanh\left[\frac{E(0) + E_c}{2\delta}\right], \quad (5.1.2)$$

one gets the following relationship between $E(0)$ and V_a :

$$-\frac{(V_a - t \cdot E_c)N_A q}{\delta P_s} = \left(k - \frac{q}{P_s} N_A t\right) \ln \frac{1 + k - \frac{q}{P_s} N_A t}{1 - k + \frac{q}{P_s} N_A t} + \ln\left[1 - \left(k - \frac{q}{P_s} N_A t\right)^2\right] - \left[k \ln \frac{1+k}{1-k} + \ln(1-k^2)\right]. \quad (5.1.3)$$

The equation has to be solved using numerical methods.

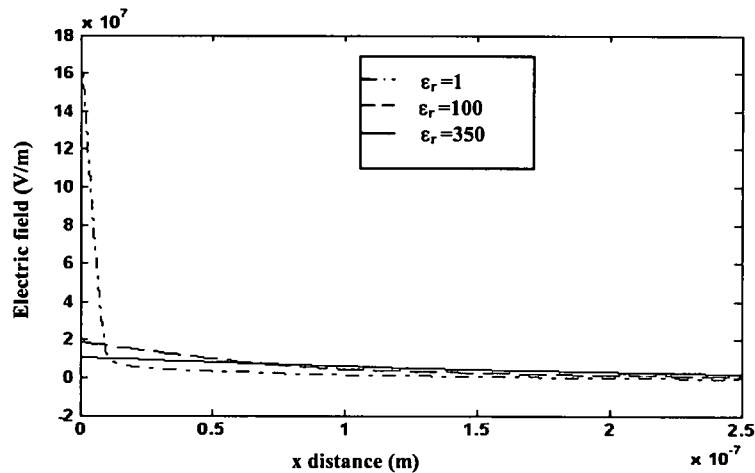


Figure 5.1.3. Field distribution in FEs with $N_A = 10^{24} / \text{m}^3$ and $V_a = -1.4$ V.

5.1.2 Capacitance

The FE film dynamic capacitance can be defined as the ratio of charge change on the electrodes over the changing applied voltage. It can be expressed as

$$C(V_a) = \frac{dQ}{dV_a} = - \frac{dD(x=0)}{dV_a} . \quad (5.1.4)$$

This definition of capacitance reflects the derivative of the hysteresis loop and the capacitance depends on the applied voltage. Another method to get the capacitance is to consider the capacitor as many thin films ("bulk regions") in series. Inside each bulk region, the field is considered to be uniform, therefore; its capacitance can be expressed as [81]

$$\Delta C = \epsilon(x) / \Delta t . \quad (5.1.5)$$

where $\epsilon(x)$ is the permittivity of the thin film and Δt is the finite thickness of the thin film considered. The total capacitance C of the whole film can be expressed as

$$\frac{1}{C} = \int_a^b \frac{dx}{\epsilon(x)} . \quad (5.1.6)$$

With the definition of

$$\epsilon(x) = \frac{dD(x)}{dE(x)} \quad (5.1.7)$$

and the assumption that

$$D(x) = \epsilon_0 \epsilon_f E(x) + P_d(x) , \quad (5.1.8)$$

one gets the expression for $\epsilon(x)$ as

$$\epsilon(x) = \epsilon_0 \epsilon_f + \frac{P_s}{2\delta} \operatorname{sech}^2\left(\frac{E - E_c}{2\delta}\right) \quad (5.1.9)$$

for the decreasing side of hysteresis loop; and

$$\epsilon(x) = \epsilon_0 \epsilon_f + \frac{P_s}{2\delta} \operatorname{sech}^2\left(\frac{-E - E_c}{2\delta}\right) \quad (5.1.10)$$

for the increasing side of the hysteresis loop [81].

The two definitions for FE capacitance come from different concepts. However; simulations show that they give same values. The second method was used here since it gives more accurate results for numerical analysis. Figure 5.1.4 shows the

effect of charge density on thin FE film capacitance. The parameters used for the simulations are the same as that used in Figure 5.1.2 except for the varying charge density. As the charge density increases the peak capacitance reduces. Analysis shows that this property is related to the field distribution in the film. As charge density increases, field in the FE film becomes more non-uniform. Stronger field in some locations of the FE thin film will make the FE polarization more saturated at these locations and reduce the distributed capacitance at these points. Since the total capacitance is considered to be a series of distributed capacitance, the smaller distributed capacitance play more decisive role in the total capacitance than larger capacitance. Therefore; higher charge density causes smaller peak capacitance. Another interesting phenomenon is that the C-V curves widen as the peak capacitance reduces due to the increase of charge density. Further simulations show that the areas below these curves are same. The following analysis confirms this statement.

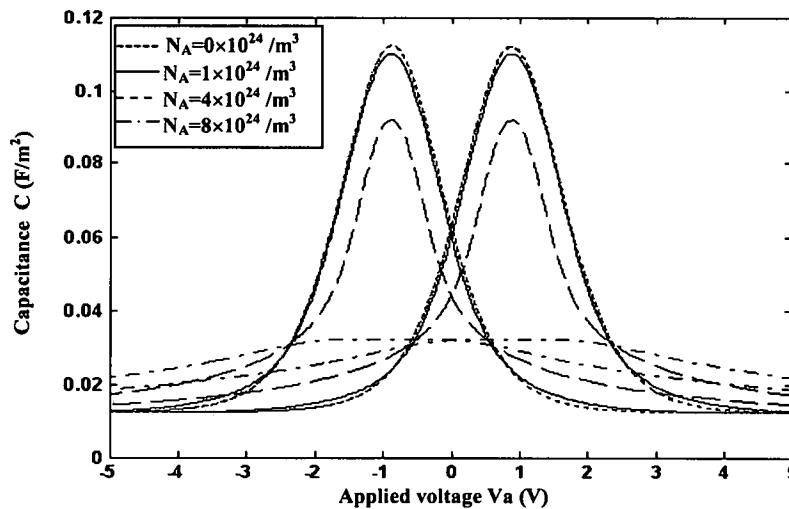


Figure 5.1.4. C-V curves of FE thin films with different dopant-ion charge density.

Supposing that V_{a1} (with a negative value) is strong enough to make all the FE switching polarization saturated in the positive x direction and V_{a2} (with a positive

value) is strong enough to make all the FE switch polarization saturated in the negative x direction, the area below the C-V curve between these two points is expressed as

$$S = \int_{V_{a1}}^{V_{a2}} C(V) dV. \quad (5.1.11)$$

With the first method of capacitance definition as given in (5.1.4), one has

$$\begin{aligned} S &= \int_{V_{a1}}^{V_{a2}} \frac{dQ}{dV} dV = \int_{V_{a1}}^{V_{a2}} dQ = [D(V_{a2}) - D(V_{a1})]_{x=0} \\ &= [\epsilon_0 \epsilon_f E(V_{a2}) - \epsilon_0 \epsilon_f E(V_{a1}) + P_d^-(V_{a2}) - P_d^-(V_{a1})]_{x=0}. \end{aligned} \quad (5.1.12)$$

Since V_{a1} and V_{a2} make the FE film switching polarization saturated at all locations, one has $P_d^-(V_{a2}) = -P_d^-(V_{a1}) = P_s$. At this time the field distribution in the film is also linear and (6.1.12) can be changed to

$$S = \epsilon_0 \epsilon_f \frac{V_{a2} - V_{a1}}{t} + 2P_s. \quad (5.1.13)$$

The area is the sum of the linear and switching polarization changes.

To verify the correctness of (5.1.13), hysteresis loops were measured on two capacitors from Radiant Technologies, Inc. One is type AA which is made of 4% niobium doped PZT (20/80) film with a thickness of 270 nm and area of $100000 \mu\text{m}^2$. The other is type AB which is made of undoped PZT (20/80) film with a thickness of 255 nm and area of $100000 \mu\text{m}^2$. The capacitance as defined in (5.1.4) is given in Figure 5.1.5 for the two capacitors. In order to compare the two capacitors, the capacitance of type AA capacitor was processed with a ratio of 270/255 and the voltage over type AA capacitor was processed with a ratio of 255/270. It is found that type AA has larger peak capacitance than AB. The explanation is that type AB has unintentional doping and has dopant-ion charges inside. Niobium doping in type AA compensated the unintentional doping and made its dopant-ion charge smaller.

Therefore, type AA has larger peak capacitance than type AB. Figure 5.1.6 gives the expanded view of Figure 5.1.5 around the peak capacitance at negative voltage. It is clear that type AB has a smaller but wider peak. This complies with the prediction.

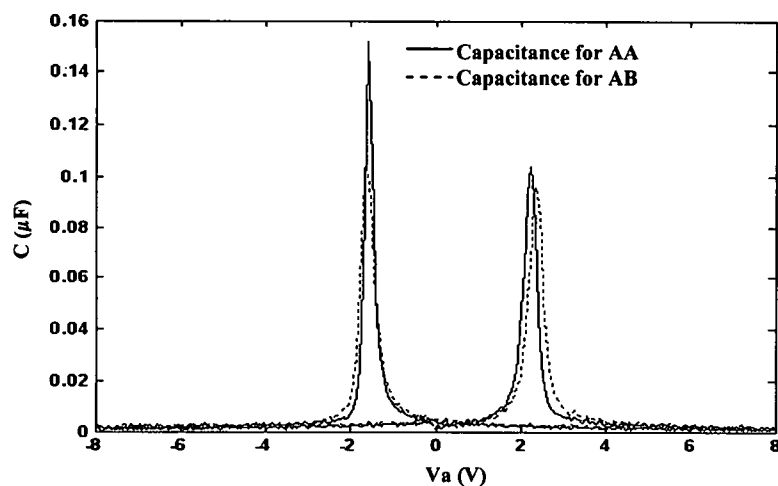


Figure 5.1.5. C-V curves obtained from the derivative of hysteresis loops for two types of capacitors: AA and AB.

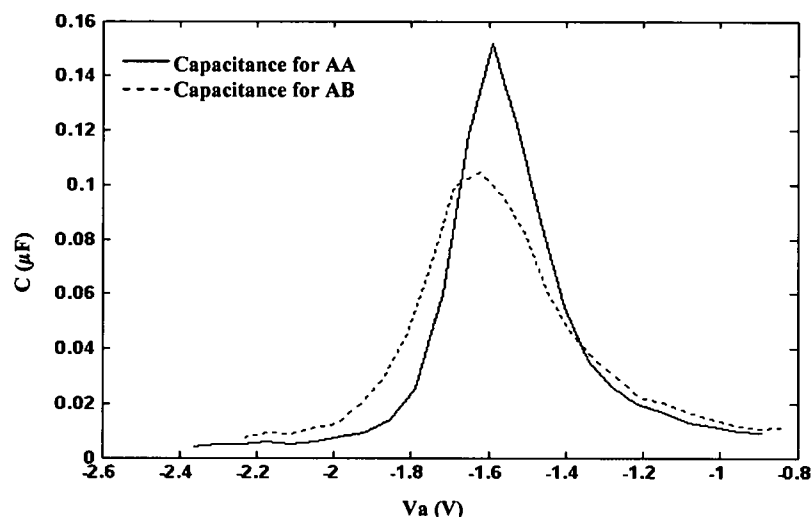


Figure 5.1.6. Expanded view of Figure 5.1.5 around the negative voltage peak capacitance.

5.2 PERFORMANCE PROPERTIES OF THIN FILM FERROELECTRICS

HYSTERESIS LOOP

This section will investigate the hysteresis loop of thin film FE. The hysteresis loop dependence on charge density in the film is theoretically analyzed. The difference between ideal and practical hysteresis loops is investigated. Influence of signal source frequency and measurement equipment input impedance on hysteresis loop is analyzed. The transition of hysteresis loop offset with time is presented and analyzed. The methods and results presented shall be beneficial to FE capacitor applications in EMC and other circuits.

5.2.1 Ideal hysteresis loop

FE hysteresis loops describe the relationship between FE polarization and applied electric field (voltage). An ideal hysteresis loop is assumed to be obtained by an ideal ST circuit without any leakage resistance. Therefore, it reflects the relationship between the applied voltage and the charge produced on the measured capacitor electrodes. As discussed before, FE can have space charges inside. This can give rise to non-uniform field distribution. And the polarization inside the FE film varies according to position. Assuming the FE capacitor electrode at $x=0$ in Figure 3.1 is connected with the normal capacitor in the Sawyer-Tower circuit, the observed hysteresis loop describes relationship between the electric displacement at $x=0$ and the applied voltage. According to the model introduced in chapter 3, this relationship can be expressed as;

$$D(0) = \epsilon_0 \epsilon_f E(0) + P_s \tanh\left[\frac{E(0) - E_c}{2\delta}\right] \quad (5.2.1)$$

for decreasing V_a and

$$D(0) = \epsilon_0 \epsilon_f E(0) - P_s \tanh\left[\frac{-E(0) - E_c}{2\delta}\right] \quad (5.2.2)$$

for increasing V_a .

Once a value is given for V_a , the electric field $E(0)$ is obtained as explained in chapter 3. After that the $D(0)$ can be obtained from (5.2.1) or (5.2.2).

Figure 5.2.1 gives simulated hysteresis loops of FE thin film capacitor with various doping densities. In these simulations, the material parameters are given as: $P_s=0.1 \text{ C/m}^2$, $\delta=2000000 \text{ V/m}$, $E_c=3500000 \text{ V/m}$ and $\epsilon_f = 350$. The results show that as the absolute value of the charging density increases the hysteresis loop shrinks and moves down. The hysteresis loops can be divided into two segments. When the applied voltage is small, both the linear polarization and switching polarization contribute to the total polarization. In this section, the difference between the increasing voltage and decreasing field responses are clear and both the hysteresis loop shape and position are related to the charge density in the FE film. Once the applied voltage is high enough, the strong electric field in the film will make the FE switching polarization saturated at any point in the film and only linear polarization changes with the applied voltage. This corresponds to the linear section of the hysteresis loops. It is a straight line which shifts along the vertical direction with charge density.

Let us take the decreasing side (E increases) of the hysteresis loop as an example.

Once the value of V_a is high enough, it can be assumed that both $E(x)$ and $E(0) \gg E_c$; terms $\tanh[\frac{E(x)-E_c}{2\delta}]$ and $\tanh[\frac{E(0)-E_c}{2\delta}]$ can be approximated to be 1 so

(3.10) becomes

$$\epsilon_0 \epsilon_f [E(x) - E(0)] = -qN_A z. \quad (5.2.3)$$

Solving (5.2.1) together with (5.2.3), one can get

$$-D(0) = -(\epsilon_0 \epsilon_f E(0) + P_s) = -P_s + \frac{\epsilon_0 \epsilon_f}{t} V_a - \frac{qN_A}{2} t \quad (5.2.4)$$

for $E(x) \ll E_c$, and

$$-D(0) = -(\epsilon_0 \epsilon_f E(0) - P_s) = P_s + \frac{\epsilon_0 \epsilon_f}{t} V_a - \frac{qN_A}{2} t \quad (5.2.5)$$

for $E(x) \gg E_c$.

Let $-P_s - \frac{qN_A}{2} t = a$ C/m²; $P_s - \frac{qN_A}{2} t = b$ C/m² and $\epsilon_0 \epsilon_f / t = c$, if a , b and c are extracted

from curve fitting, one has

$$qN_A t = -(a + b), \quad (5.2.6)$$

$$P_s = (b - a) / 2 \text{ and} \quad (5.2.7)$$

$$\epsilon_f = ct / \epsilon_0. \quad (5.2.8)$$

The analyses show that charge density, saturation polarization and the dielectric constant can be extracted from the hysteresis loops obtained from the ideal hysteresis loop.

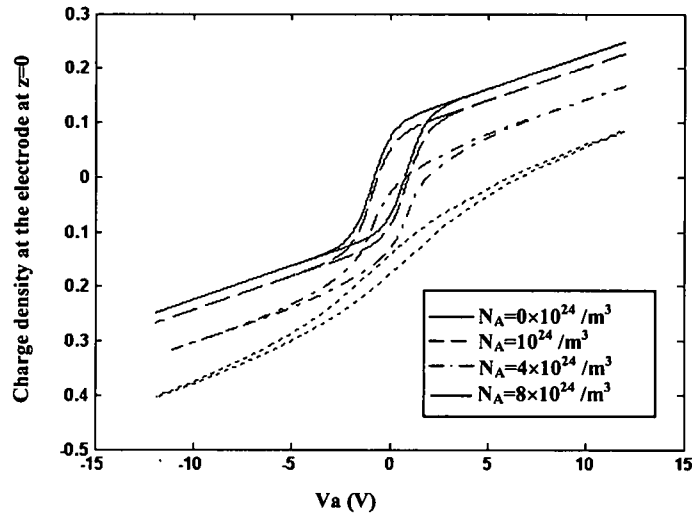


Figure 5.2.1. Hysteresis of FE films with doping density $N_A = 0, 10^{24} / \text{m}^3, 4 \times 10^{24} / \text{m}^3$ and $8 \times 10^{24} / \text{m}^3$ from top to bottom.

5.2.2 Hysteresis loop measurements using a Sawyer Tower (ST) circuit

Practical hysteresis loops can be obtained with a ST circuit. Figure 5.2.2 shows an equivalent circuit of practical ST circuit. A time dependant input voltage $V_i(t)$ is applied to the circuit, resulting in an output voltage $V_o(t)$, which is supposed to represent the charge on the FE capacitor electrode. The resistor $R_f(t)$ simulates the effect of current leakage through a FE capacitor. The resistor $R_n(t)$ might represent the input impedance of the measuring equipment or leakage conductance of a normal capacitor.

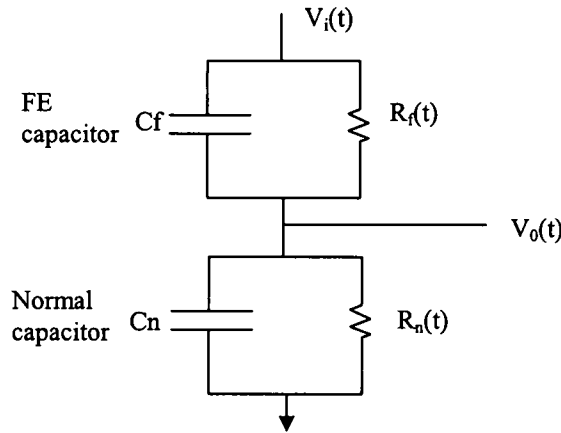


Figure 5.2.2. An equivalent circuit of a ST circuit.

In order to describe the relationship between $V_i(t)$ and $V_o(t)$, a general electrical description for FE films needs to be given. If the effect of the space charge on the switching polarization is neglected, the hysteresis loop can be expressed, by using (5.2.1) and (5.2.2), as

$$Q^+ = AP_s \tanh \frac{V_a - V_c}{2\delta} + \frac{V_a A}{t} \epsilon_0 \epsilon_f - \frac{q}{2} N_A A t \quad (5.2.9)$$

for increasing V_a , and

$$Q^- = -AP_s \tanh \frac{-V_a - V_c}{2\delta} + \frac{V_a A}{t} \epsilon_0 \epsilon_f - \frac{q}{2} N_A A t \quad (5.2.10)$$

for decreasing V_a ,

where $V_a = V_i - V_o$ is the applied voltage across the FE capacitor,

Q^+ and Q^- represent the charge on the FE capacitor electrodes,

A is the area of the FE capacitor electrodes and

N_A is the doping density.

As shown in the previous section, besides P_s , P_r , E_c and ϵ_f , the doping concentration N_A also influence the ideal hysteresis loop of a FE film. To simplify the problem, (5.2.9) and (5.2.10) can be used to describe thin film FE with electric charges inside. The values of P_s , V_c , δ , ϵ_r and N_A here are extracted from curve fitting to measured hysteresis loops. They have different physical meanings from the original material parameters as defined in the previous section because this method assumes a uniformly distributed field in thin film FE.

With the above description, one can get the relationship between V_i and V_o as [88]:

$$\frac{dP_{\text{switch}}}{dt} = \frac{dP_{\text{sat}}}{dV_a} \Gamma \left(\frac{dV_i}{dt} - \frac{dV_o}{dt} \right), \quad (5.2.11)$$

$$\frac{dV_o}{dt} = \left[\left(A \frac{dP_{\text{sat}}}{dV_a} \Gamma + \epsilon_0 \epsilon_f \frac{A}{t} \right) \frac{dV_i}{dt} - \frac{V_o}{R_n} + \frac{V_a}{R_f} \right] / \left(C_n + A \frac{dP_{\text{sat}}}{dV_a} \Gamma + \epsilon_0 \epsilon_f \frac{A}{t} \right), \quad (5.2.12)$$

where

$$P^+_{\text{sat}} = P_s \tanh \frac{V_a - V_c}{2\delta}, \quad (5.2.13)$$

$$P^-_{\text{sat}} = -P_s \tanh \frac{-V_a - V_c}{2\delta}, \quad (5.2.14)$$

$$\Gamma = 1 - \tanh \frac{P_{\text{switch}} - P_{\text{sat}}}{\xi P_s - P_{\text{switch}}}, \quad (5.2.15)$$

$\xi = 1$ for increasing V_a and $\xi = -1$ for decreasing V_a .

Since the transition status of switching polarization needs to be considered, the term Γ is introduced in the above equations to describe the arbitrary status of switching polarization [88].

With the extracted parameters of P_s , V_c , δ and ϵ_f plus the initial condition for $V_o(0)$ and $P_{switch}(0)$, $V_o(t)$ can be obtained for a given $V_i(t)$. It is worth noting that the charge density, which plays an important role in the offset of ideal hysteresis loop, is not reflected in the equations and therefore shall not affect the hysteresis loop offset.

5.2.3 Results and discussions

Hysteresis loops were measured for FE capacitors provided by Radiant Technologies, inc. These capacitors are composed of undoped 20/80 PZT thin films which has a thickness of 255 nm and area of 10^{-8} m^2 . Measurements were made with a ST circuit as described in chapter 4.

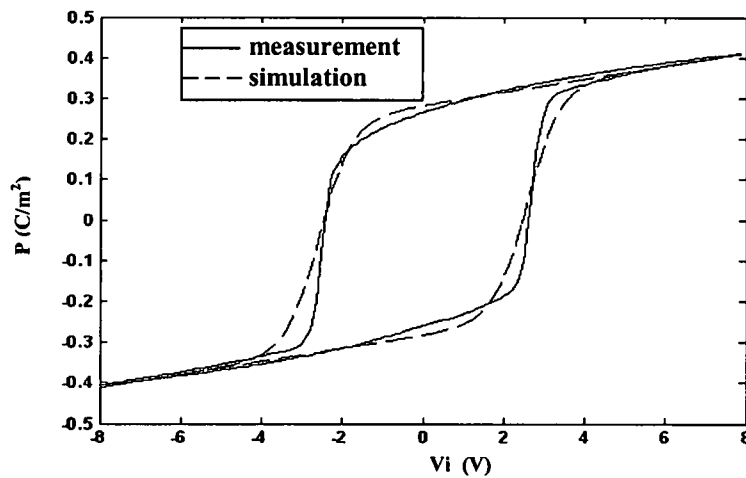


Figure 5.2.3. Hysteresis loops for FE capacitor with $A=10^{-8} \text{ m}^2$ and frequency=100 kHz.

Hysteresis loops in Figure 5.2.3 were measured with a ST circuit with $C_n=100 \text{ nF}$. The solid curve is obtained by measurement with an 8 V/10 kHz input sinusoidal signal. Hysteresis loop parameters extracted from the curve are $V_c=2.575 \text{ V}$, $P_r=0.282 \text{ C/m}^2$, $P_s=0.2829 \text{ C/m}^2$, $\epsilon_f=463.5$. The hysteresis loop in dashed line is

produced with the extracted parameters and the introduced model. Good agreement is found between the measurements and the simulation results.

Figure 5.2.4 gives three types of hysteresis loop and each has ten cycles: simulated hysteresis loop according to (5.2.16) and (5.2.17) with initial conditions as $(V_o(0), P_{switch})=(0V, 0 \text{ C/m}^2)$; simulated hysteresis loop according to (5.2.16) and (5.2.17) with initial conditions as $(V_o(0), P_{switch})=(0V, P_{sat}(0))$; hysteresis loop obtained by measurement. For all these hysteresis loops the input signal is $8V@10 \text{ kHz}$, $R_n=1 \text{ M}\Omega$, $C_n=100 \text{ nF}$ and $R_t \approx \infty$. Although the simulated hysteresis loop with initial condition as $(V_o(0), P_{switch})=(0V, 0 \text{ C/m}^2)$ becomes symmetric rapidly, simulated hysteresis loop with initial condition as $(V_o(0), P_{switch})=(0V, P_{sat})$ agrees with the measurement results and this reflects the actual initial situation since the preset V_i scans were performed before the scans used for data collection. It is shown that the hysteresis loop has an initial offset.

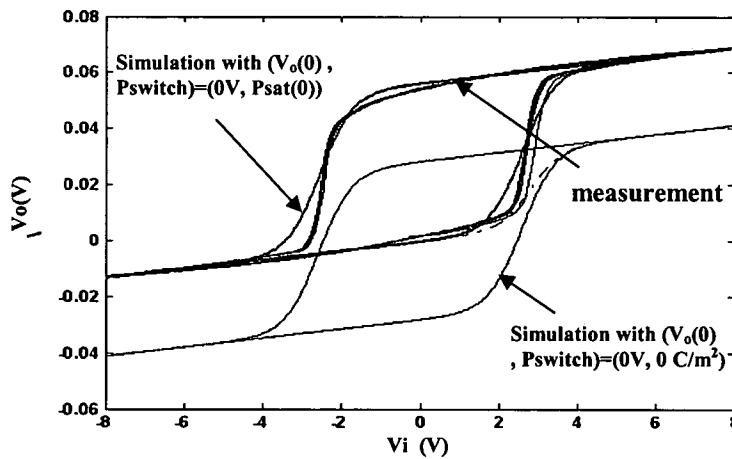


Figure 5.2.4. Ten cycles of hysteresis loop with $C_n=100 \text{ nF}$, $R_n=1 \text{ M}\Omega$, $A=10^{-8} \text{ m}^2$ and frequency= 10 kHz .

To further study the properties of thin film FE hysteresis loop, the frequency of applied signal V_i was changed from 10 kHz to 100 Hz and the other parameters

were kept same as in Figure 5.2.4. Figure 5.2.5 gives measurement results for about 30 cycles. It indicates that the hysteresis loop has an initial offset similar to that in Figure 5.2.4. As the time goes on, the hysteresis loop moves down and finally becomes symmetric. Figure 5.2.6 gives the simulated hysteresis loop with 100 Hz input signal V_i and has a good match to the measurement results.

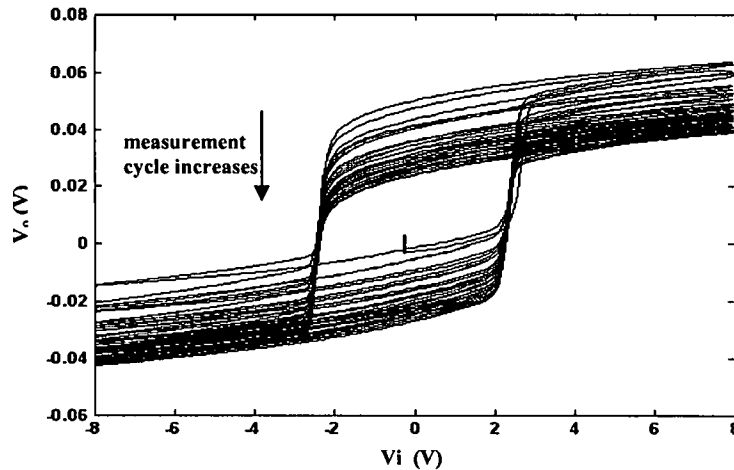


Figure 5.2.5. Hysteresis loop by measurement for FE capacitor with frequency=100 Hz, $C_n=100$ nF, $R_n=1$ M Ω and $A=10^{-8}$ m².

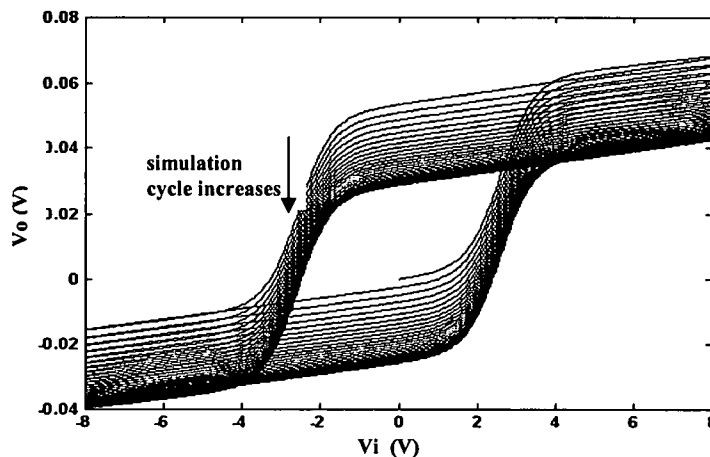


Figure 5.2.6. Hysteresis loop by simulation for FE capacitor with frequency=100 Hz(10 kHz), $C_n=100$ nF, $R_n=1$ M Ω (10 k Ω) and $A=10^{-8}$ m².

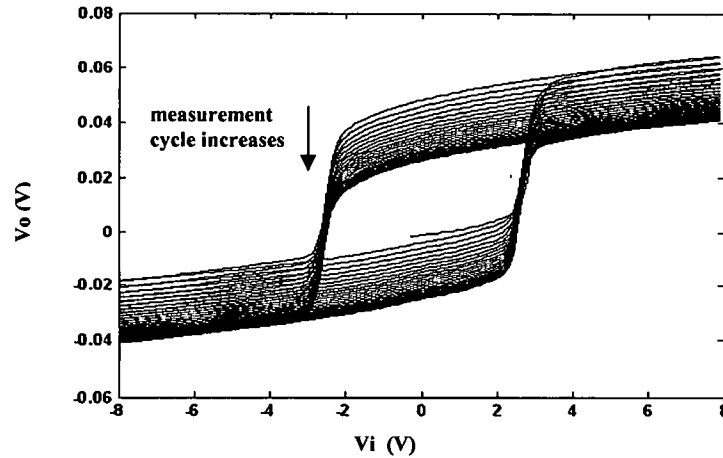


Figure 5.2.7. Hysteresis loop by measurement for FE capacitor with frequency=10 kHz, $C_n=100$ nF, $R_n=10$ k Ω and $A=10^{-8}$ m².

Why couldn't a similar phenomenon be found as shown in Figure 5.2.4 where the input signal frequency is 10 KHz? It is suspected that the hysteresis loop shift is related to the input signal frequency and is due to the input impedance of the measurement equipment and its equivalent resistance, as mentioned in section II. An ideal hysteresis loop is supposed to be obtained with ST circuit where these resistances are not considered and reflect the direct relationship between the applied voltage V_a and the electric charge on the electrodes of the capacitor. Simulation shows that FE films with and without doping charge will generate stable hysteresis loops with and without offset and the offset is related to the doping charge density. In practical ST circuit, The V_o and V_i relationship is governed by (5.2.11) and (5.2.12). Since the doping charge density does not appear in the equations, it is thought that it has no effect on practical hysteresis loop offset. The initial offset observed in Figure 5.2.4, 5.2.5 and 5.2.6 comes from the film initial conditions $V_o(0)$ and $P_{switch}(0)$. It is the measurement equipment input impedance and the leakage current equivalent resistance that causes DC leakage current and finally gives

symmetric hysteresis loop. The reason that the property was not found in Figure 5.2.4 for 10 KHz input signal is that the observation time is very short for 10 cycles of signal compared to that for 100 Hz signal. To verify the statement, the equipment input impedance R_n was changed from 1Mohm to 10 k Ω and the input signal frequency was set at 10 kHz. Simulation was carried out according to (5.2.11) and (5.2.12). The DC leakage current with a 10 k Ω resistor could be as high as 100 times higher than with a 1 M Ω resistor. Since leakage time for 10 kHz input signal is 1/100 of that for 100 Hz input signal, the shift of offset will move with same amplitude for every cycle and therefore the hysteresis loops will have the same shape. Simulation result for 10 kHz input signal with 10 k Ω resistor is exactly the same as given in Figure 5.2.6. Figure 5.2.7 also gives the measured hysteresis loop for 10 kHz input signal and $R_n=10$ k Ω . It is similar to that in Figure 5.2.5. This indicates that hysteresis loop obtained by practical ST circuit will eventually become symmetric and the reason is the DC leakage current existing in the circuit. In [89], asymmetrical leakage current was analyzed to be a possible origin of the polarization offsets observed in compositionally graded ferroelectric films. It also proves that leakage current plays an important role on FE hysteresis loop.

5.3 Capacitance of thin ferroelectric films obtained with different methods

5.3.1 Measurements

Section 5.1 did some analyses on FE capacitance and its large signal capacitance which is obtained as the derivative of its hysteresis loop. In this section the relationship between the large signal and small signal capacitance of a thin film FE will be investigated. Measurements were conducted on thin film FE capacitors provided by Radiant Technologies, Inc. The capacitors are composed of undoped

20/80 PZT thin film which has a thickness of 255 nm and area of 10^{-8} m^2 . Measurements were made with a precision LC tester from Radiant Technologies, Inc. Figure 5.3.1 gives the large signal capacitance and Figure 5.3.2 gives the small signal capacitance measured directly with a small signal of 0.2 V and 1 kHz. The capacitances obtained with the two methods have significantly different properties: The large signal C-V curve has very sharp peaks and the peak value is about as 40 times large as that of the small signal C-V curve.

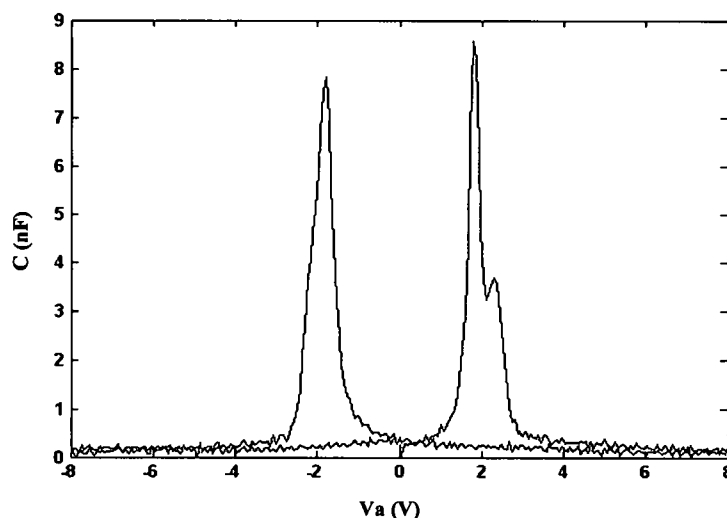


Figure 5.3.1. Large signal C-V curve obtained by the derivation of hysteresis loop.

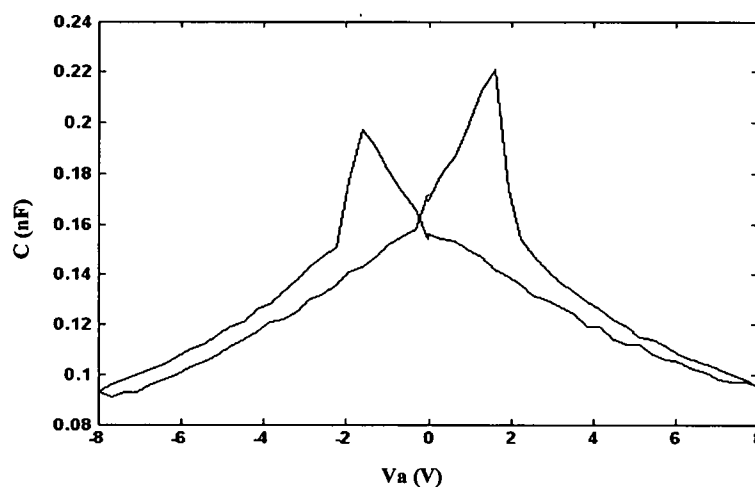


Figure 5.3.2. Small signal C-V curve directly measured with small AC signal.

5.3.2 Effects of space charges on FE capacitance

Space charge in the FE films complicated electric field distribution and changes the capacitance. One assumption for the cause of the difference between small signal capacitance and large signal capacitance of thin FE films is that the bias voltage applied at each step of small signal C-V measurement makes the space charge distribution change. Two mechanisms are reported in the literature to be able to make it happen: charged defects migration and electron trapping.

Reference [83] studied the C-V changes of thin FE film under different bias sweep rate. The authors pointed that both the coercive voltage V_m and the peak capacitance of PZT thin film C-V curves are dependent on the sweep rate of bias voltage change rate. Once the sweep rate increases, the coercive voltage V_m increases and the peak capacitance C_m decreases. It was further pointed that the effect is due to the spatial separation of mobile charge carriers under the action of the bias field and the accumulation of charged defects in the near-electrode regions of the films. However, our study shows that the measurement results given in that paper is most likely due to the used RC circuit method as shown in Figure 4.4.

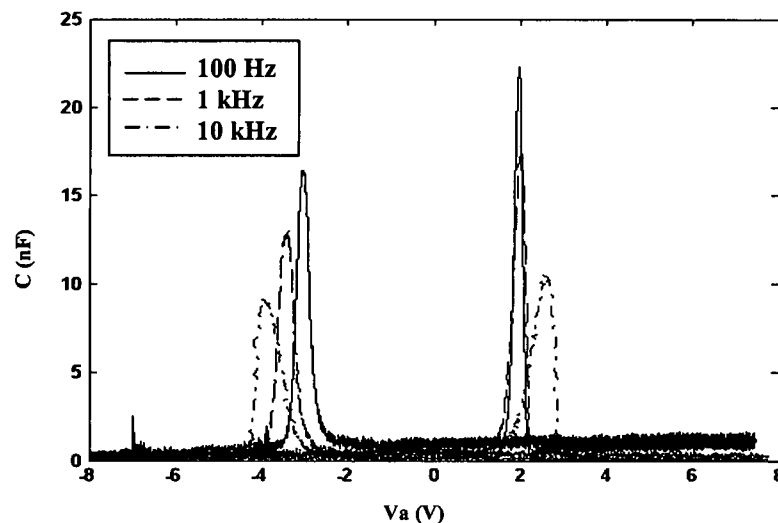


Figure 5.3.3. Capacitance measured with a RC circuit.

Figure 5.3.3 gives the measurement results on the same FE capacitor as used in section 5.3.1 with the RC circuit method. It is shown that peak capacitance value decreases and the coercive voltage increases with the input signal frequency. To verify that the C-V change is due to the resistor the FE capacitor is described as (refer to chapter 3)

$$Q^+ = AP_s \tanh \frac{V_i - V_c}{2\delta} + \frac{V_i A}{t} \epsilon_0 \epsilon_f \quad (5.3.1)$$

for increasing V_a , and

$$Q^- = -AP_s \tanh \frac{-V_i - V_c}{2\delta} + \frac{V_i A}{t} \epsilon_0 \epsilon_f \quad (5.3.2)$$

for decreasing V_a ,

where $V_i = V_a - V_o$ is the applied voltage across the FE capacitor;

Q^+ and Q^- represent the charge on the FE capacitor electrodes,

A is the area of the FE capacitor electrodes,

V_c is the coherent coercive voltage,

t is the thickness of the film,

The circuit performance can be described as

$$\frac{dQ}{dt} R + V_i = V_a . \quad (5.3.3)$$

With (5.3.1)-(5.3.3), the observed hysteresis loops can be simulated and the capacitance can be obtained from their derivatives. Simulation results correlate the measurements. Since the RC circuit can be considered as a Deby model, it is reasonable to attribute the C-V curve changes to the resistor R .

To find whether the capacitance different is due to defect migration in the film, a thin film FE capacitance was measured at several DC biases with different times as given in Table 5.3.1. The measured capacitor is composed of undoped 20/80 PZT thin film which has a thickness of 255 nm and area of $1 \times 10^{-7} \text{ m}^2$. The

measurements were made with a precision LC tester. It shows that the capacitance doesn't change obviously with time. On the contrary, if charge-defect migration is assumed to affect the small signal C-V, the following analyses will tell us how the capacitance will be affected.

Table 5.3.1. Measured capacitance of thin FE film vs time

Va (V)	Capacitance (nF)			
	10 ms	100ms	1s	10s
2	1.789	1.754	1.766	1.762
3	1.664	1.648	1.641	1.645
4	1.551	1.547	1.547	1.523

Under a bias field E, the charge defect distribution must meet the following equation:

$$-D \frac{dN}{dx} = EN\mu, \quad (5.3.4)$$

where D and μ are the defect diffusion coefficient and mobility; N is the defect density and E is the electric field. Using Einstein relation:

$$D = \mu kT/q, \quad (5.3.5)$$

where k is the Boltzmann constant, q is the defect charge, one obtains

$$N(x) \sim \exp(-qxVa/kTL). \quad (5.3.6)$$

Let us assume an defect charge is +e, where e is the elementary charge. Since at T=360 K, $q \cdot Va/k \cdot T \approx 100$, the abrupt change of N(x) at small x takes place. Therefore, a two-layer model can be used to describe the defect distribution: a homogeneous defect-enriched layer near one electrode with thickness h and defect concentration of N_1 ; an uncompensated layer with thickness of t-h and space charge density of N_2 . With the relation of $h \approx t \cdot k \cdot T/q \cdot Va$, it can be assumed that $h \approx 5$ nm [84] under the voltage of $Va=4$ V. The general h(Va) can be obtained as

$h(V_a) = h(V_a = 4) \cdot 4 / V_a$ and the general defect density $N_1(V_a)$ can be obtained as $N_1(V_a) = N_1(V_a = 4) \cdot h(V_a = 4) / h(V_a)$. Once the space charge distribution is obtained the field strength distribution and therefore C-V curve can be simulated using the model given in [90]. Figure 5.3.4 gives the simulation C-V results for FE films with the following material parameters: $t = 250$ nm, $P_s = 0.1$ C/m², $\delta = 2000000$ V/m, $E_c = 3500000$ V/m and $\epsilon_f = 350$. In these simulations, N_2 is assumed to be 0 /m³ and N_1 was give three different values as -1×10^{24} /m³, -2×10^{24} /m³ and -4×10^{24} /m³. The solid line indicates the increasing V_a C-V curves and dashed line indicates the decreasing V_a curves. Although it shows that film capacitance varies with applied voltage, the curves have many fluctuations and are not as smooth as that given by measurements. Therefore, it is stated that the deference between small signal C-V curve and large signal C-V curve of thin FE film can not be due to charged defect migration.

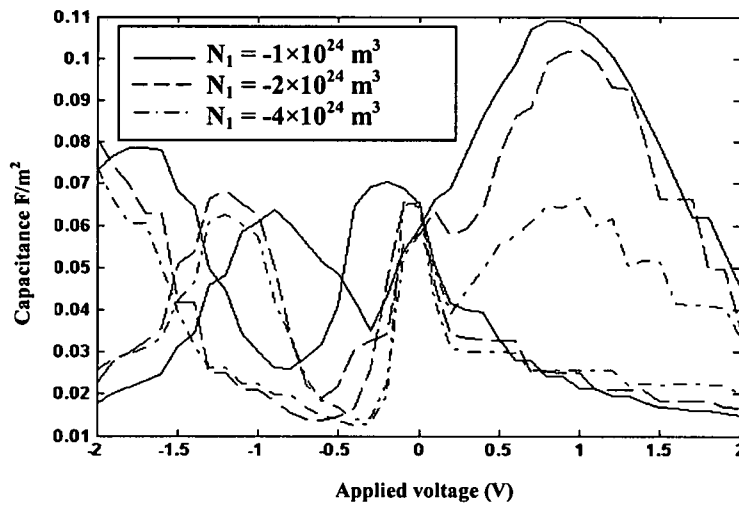


Figure 5.3.4. Simulated C-V curves of FE thin film with different charged defect density.

Once a bias is applied over a thin FE film, electron trapping can take place. Reference [91] studies the effect of constant voltage stress on FE PZT thin film

capacitors. The stress was found to give rise to capacitance reduction and voltage shift of C-V curve of the capacitors. A correlation between the stress effects and the electron trapping inside the films was established. Assuming leakage current to be $J(x, t)$ and, in the absence of detrapping, the rate equation governing the change of trapped electron density n_T can be written as [91]

$$q\left(\frac{\partial n_T(x, t)}{\partial t}\right) = \sigma_T J(x, t)[N_T - n_T(x, t)], \quad (5.3.7)$$

where N_T is the density of neutral trap centers; σ_T is the electron capture cross section of a trap center; q is the electronic charge and x is the distance of the electron-trap center from the interface. If the film is very thin, the trapped electron density can be considered even and given as

$$n_T(x, t) = \frac{N_T[\exp(\sigma_T N_{inj}) - 1]}{\exp(\sigma_T N_{inj})}, \quad (5.3.8)$$

$$\text{where } N_{inj} = \int [J(0, t')/q] dt' \quad (5.3.9)$$

is the number of injected electrons per unit area. Regardless of the applied voltage polarity and amplitude, electron trapping shall take place all the time during small signal capacitance measurement. Therefore, the space charge density in the FE thin film will increase continuously during small signal capacitance measurement. Using the model introduced in [90], the C-V curves of a thin FE film with different space charge density were simulated and are given in [92]. The results show that the capacitance peak decreases with the space charge density. As mentioned previously, capacitance of thin PZT films were measured under a bias voltage at different times didn't show significant change. That means electron trapping does not play an important role in the C-V change. On the other hand, if serious electron trapping takes place during small signal capacitance measurement and changes the

film C-V curve, it would be expected that the trapping effects last for some time and change the hysteresis loop measured afterwards. However, the hysteresis loop measured before and after the small signal C-V measurement didn't show obvious change.

5.3.3 Explanation based on Miller's model

The previous capacitance analyses are based on the large signal and are only applicable to the stable status when the applied voltage changes between two values that are strong enough to make the spontaneous polarization to be saturated. Since the small signal capacitance is related to domain switch under small signals, the relation between FE polarization and applied voltage with arbitrary shape and initial conditions needs to be investigated. This is also addressed in 5.2. The general derivative of the switching polarization can given as

$$\frac{dP_{\text{switch}}}{dt} = \frac{dP_{\text{sat}}}{dV_a} \Gamma, \quad (5.3.10)$$

where Γ is defined as

$$\Gamma = 1 - \tanh \frac{P_{\text{switch}} - P_{\text{sat}}}{\xi P_s - P_{\text{switch}}}, \quad (5.3.11)$$

$\xi = 1$ for increasing V_a and $\xi = -1$ for decreasing V_a .

With this description, the D-E relations can be given when applied signal is a small AC signal with DC bias. Figure 5.3.5 gives the simulated small AC signal response of a thin FE film with bias. The materials parameters used for the simulation are the same as those used in Figure 5.3.4. A signal with large amplitude was applied first for a cycle. Once the applied field strength reaches E_c which is considered to be a bias, the applied field amplitude was changed to $0.1E_c$. Initially when the applied small signal increases, the polarization changes with the same rate as that for a large signal. Then the small signal decreases and the polarization decreases at a

slower rate than that for a large signal with the same applied value. Once the small signal takes its second cycle of increase and decrease, the polarization increases with a slower rate and decreases with a faster rate than in the first cycle. After many cycles, the increase and decrease rates become equal and D-E curve becomes stable. In Figure 5.3.5 50 cycles of small signal were applied. It is logical to assume that capacitance measured at small signal reflects the stable polarization change rate instead of the polarization change rate for large applied signals which determines large signal capacitance.

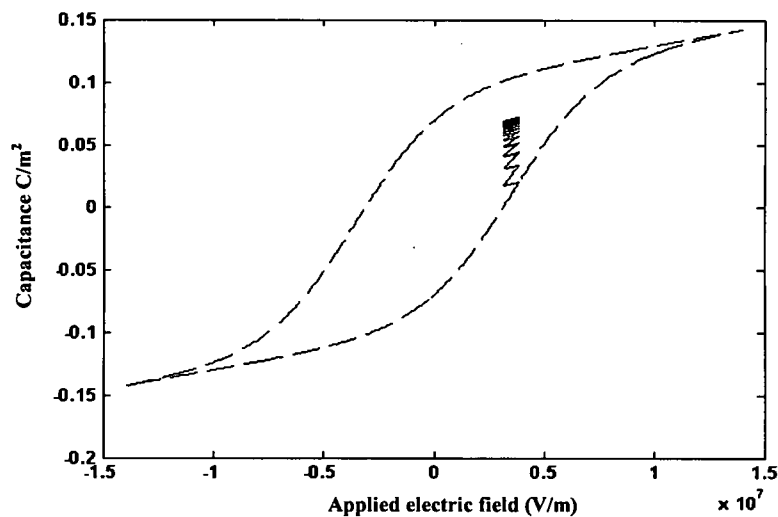


Figure 5.3.5. The small signal response with a bias of a FE film.

In order to see if the above analysis is correct, D-V curves were measured with a Sawyer-Tower circuit as described in [90]. In Figure 6.3.6 the measured capacitor is composed of undoped 20/80 PZT thin film which has a thickness of 255 nm and area of $4 \times 10^{-9} \text{ m}^2$. The value of the normal capacitor is 4.7 nF. The measurement was done with an oscilloscope. After one cycle of signal with amplitude of 8 V applied, the small signal with an amplitude of 0.1 V was applied at around 3.6 V

bias. It is found that the polarization change rate under small signal is much smaller than that of the increasing side of large signal of D-V at the bias voltage.

It seems that the model in [90] can qualitatively explain the capacitance difference between small and large signals. However; several issues remains to be investigated. First, figure 5.3.7 shows a gradual polarization drop under small signal while Figure 5.3.6 shows a gradual polarization increase. This can be explained by the hysteresis loop offset shift due to the leakage current of the oscilloscope input impedance as investigated in [90].

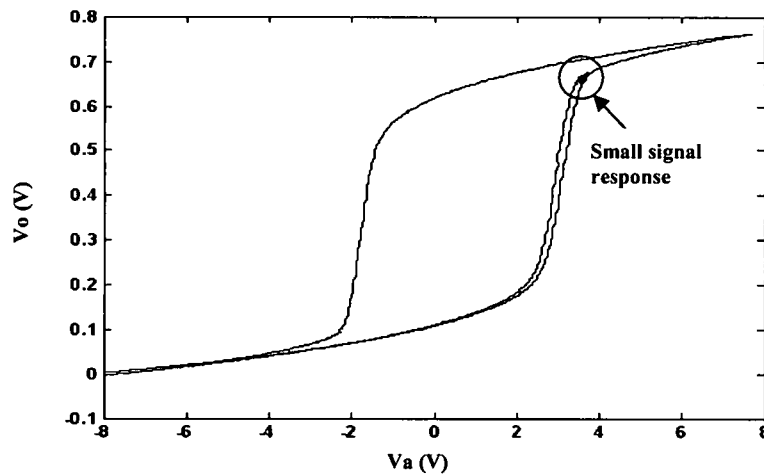


Figure 5.3.6. Measured D-V curve of FE thin film with small AC signal and large bias signal applied.

Second, if a FE film has a symmetric hysteresis loop, the model predicts that the small signal capacitance of the FE film under a bias has the same value no matter whether the bias is in increasing status or decreasing status. Let V_a be the bias. The stable point (V , P_{switch}) is subject to the following relation:

$$\frac{dP_{\text{switch}}^+}{dt} = \frac{dP_{\text{switch}}^-}{dt} , \quad (5.3.12)$$

where the left side term indicates the increasing polarization change rate and the right side term indicates the decreasing polarization change rate. According to (5.3.10)-(5.3.12), P_{switch} can be determined for each V_a , and therefore, stable polarization change rate and small signal capacitance can be determined. In this way only one C-V curve will be obtained. However, usual measurements show that FE films have different increasing and decreasing C-V curves. This issue needs to be investigated in the future.

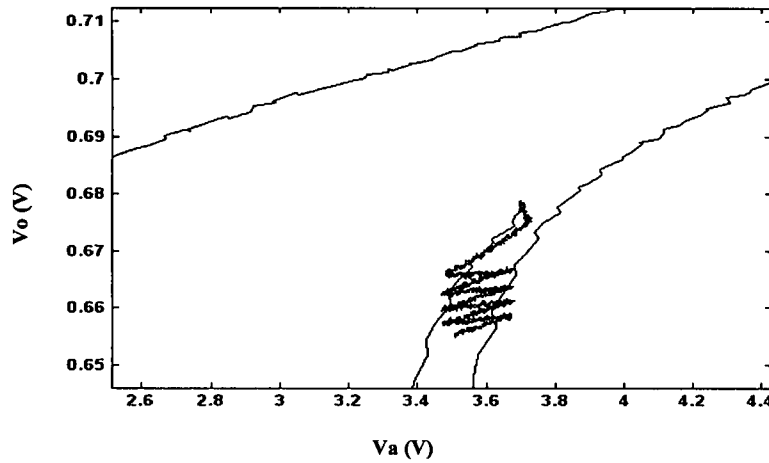


Figure 5.3.7. Expanded view of D-V curve for small signal.

5.3.4 Explanation based on the Preisach model

A thin film FE can be modeled into a group of dipoles. With the Preisach model [87], the coupling between the dipoles, the effect of space (defect) charge on the dipoles and the presence of grain boundaries or stress are considered by a distribution function of $f(V_c^+, V_c^-)$ in the Preisach plane, where V_c^+ and V_c^- stand for the coercive voltage for positive and negative switching of the dipoles. The distribution function stands for the ratio of number of the dipoles that have the values of V_c^+ and V_c^- with respect to the total dipole number. Figure 5.3.8a shows an applied signal

across a thin film FE. Assuming that the signal before point 1 has large signal cycling and the film is saturated. After point 1 small AC signal is applied. The status

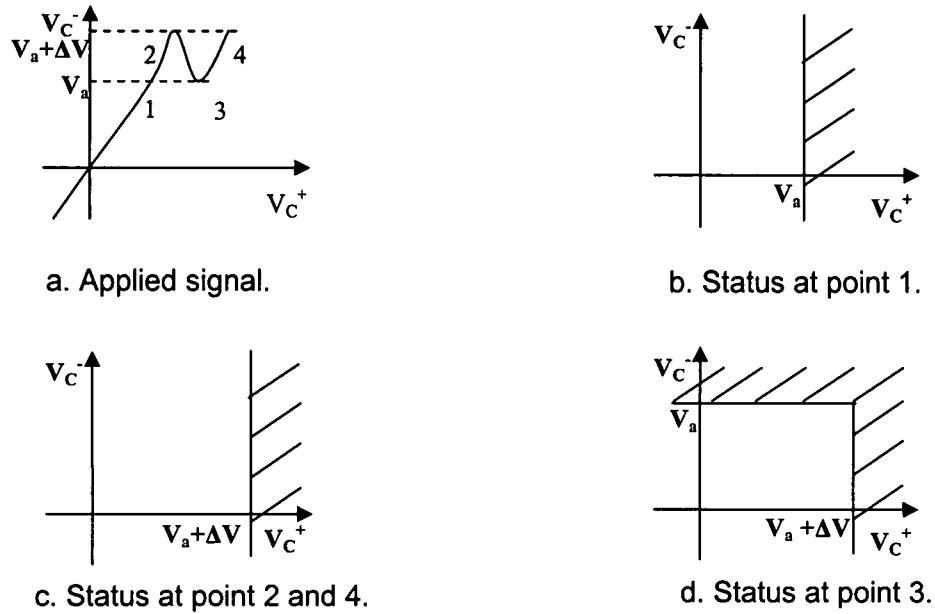


Figure 5.3.8. Status change of thin film FE under signals.

of the film at point 1 is shown in Figure 5.3.8b where the shaded area indicates negatively switched dipoles and white area indicate positively switched dipoles. Figure 5.3.8c shows the film status at point 2 and the ratio change of the switched dipoles after point 1 is given as $\Delta P_{12}^+ = \int_{-\infty}^{+\infty} dV_C^- \int_{V_a}^{V_a+\Delta V} f dV_C^+$, where the positive sign of the result means positive switching. This contributes to the large signal capacitance. The film status at point 3 is shown in Figure 3d and the ratio change of the switched dipoles after point 2 is $\Delta P_{23}^+ = - \int_{V_a}^{+\infty} dV_C^- \int_{-\infty}^{V_a+\Delta V} f dV_C^+$, where the minus means negative switching. Once the signal goes to the point 4, the film status comes back to Figure 5.3.8c and the related switched dipole ratio change is $\Delta P_{34}^+ = \int_{V_a}^{+\infty} dV_C^- \int_{-\infty}^{V_a+\Delta V} f dV_C^+$ and this contributes to small signal capacitance. Figure 5.3.8 shows that different areas

in the Preisach plane are involved for large signal and small signal capacitance. The values are dependent on the function f and can be different. Our study shows that the Preisach model can under-estimate the small signal capacitance. However, further study shows that the predicted small signal C-V curve has only one peak, and is symmetric to the C axis and doesn't agree with the observed measurements.

5.3.5 Explanation based on the Landau-Khalatnikov circuit model

5.3.5.1 Ideal hysteresis and capacitance

According to 3.4 the stable response of Q to V of a FE capacitor depends on the initial value $Q(t=0)$, the signal amplitude V_0 and frequency. Let us assume that we are dealing with a saturated hysteresis loop and the applied signal has a large value of V_0 . Under some situations, the system can be simplified and an ideal hysteresis loop can be obtained. First, If f is very small, it is reasonable to assume that the $dQ/dt \approx 0$. Second, if the material has very small viscosity, R_s can be assumed to be 0. Under these conditions, (3.17) can be changed into

$$Q^3 + \frac{\alpha S^2}{\beta} Q - \frac{S^3}{\beta L} V = 0. \text{ Let} \quad (5.3.13)$$

$$\Delta = \left(\frac{\alpha S^2}{3\beta}\right)^3 + \left(\frac{S^3}{2L\beta} V\right)^2, \quad (5.3.14)$$

and a value is given to V , the corresponding polarizations can be obtained by solving

$$(5.3.14). \text{ If } |V| > V_C = -\frac{2L\alpha}{3\sqrt{3}} \sqrt{-\frac{\alpha}{\beta}}, \text{ where } V_C \text{ is ideal coercive voltage, then } \Delta > 0 \text{ and } Q$$

has only one real value

$$Q = \sqrt[3]{\frac{S^3}{2L\beta} + \sqrt{\Delta}} + \sqrt[3]{\frac{S^3}{2L\beta} - \sqrt{\Delta}}. \quad (5.3.15)$$

If $|V| \leq V_C = -\frac{2L\alpha}{3\sqrt{3}}\sqrt{-\frac{\alpha}{\beta}}$, then $\Delta \leq 0$ and Q has two values related to the minimum free

potential of the system:

$$Q_1 = \sqrt[3]{\frac{S^3 V}{2L\beta} + \sqrt{\Delta}} + \sqrt[3]{\frac{S^3 V}{2L\beta} - \sqrt{\Delta}} \quad \text{and} \quad (5.3.16)$$

$$Q_2 = \omega^3 \sqrt[3]{\frac{S^3 V}{2L\beta} + \sqrt{\Delta}} + \omega^2 \sqrt[3]{\frac{S^3 V}{2L\beta} - \sqrt{\Delta}}, \quad (5.3.17)$$

where $\omega = \frac{-1+i\sqrt{3}}{2}$ and $\omega^2 = \frac{-1-i\sqrt{3}}{2}$.

When $V=0$ V, $Q = \pm Q_S = \pm S\sqrt{-\frac{\alpha}{\beta}}$, where Q_S is called the spontaneous polarization.

Figure 5.3.9 gives an example of an ideal hysteresis loop. The parameters used are $\alpha = -6.062 \times 10^7$ Vm/C², $\beta = 6.7358 \times 10^8$ Vm/C⁴. $S = 10^{-7}$ m² and $L = 0.255$ μ m. The related hysteresis loop parameters are Q_S is 3×10^{-8} C and the coercive voltage V_C is 1.785 V.

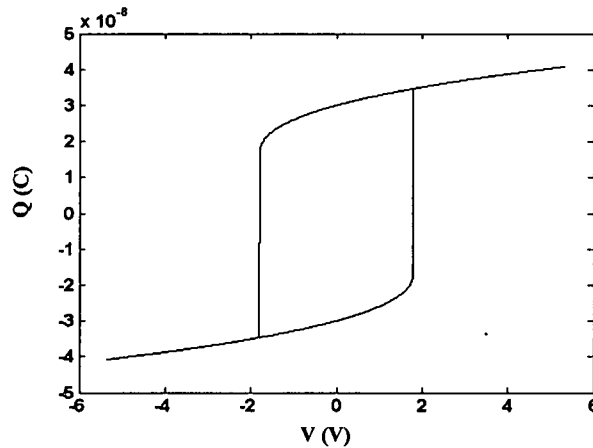


Figure 5.3.9. Ideal hysteresis loop of a thin film FE capacitor

The ideal capacitance of a FE film can be obtained as the derivative of its ideal hysteresis loop as

$$C_i = \frac{dQ}{dV} = \frac{S}{L} \frac{1}{\alpha + 3Q^2\beta/S^2}. \quad (5.3.18)$$

In (5.3.18) C_i is related to Q . Figure 5.3.9 shows that Q is not a continuous function of V . On the rising phase of the hysteresis loop, Q continuously increases with V initially and this causes C_i continuously increases with V . Once V approaches V_C , Q will switches from $-S_3\sqrt{\frac{V_C}{2L\beta}}$ to $2S_3\sqrt{\frac{V_C}{2L\beta}}$. This gives a maximum value of $C=+\infty$ and then suddenly changes to 2.1563 nF. After that, Q continuously increases with V and C continuously decreases. Both Q and C are not continuous around the coercive voltage. Figure 5.3.10 gives the ideal C-V curve corresponding to Figure 5.3.9.

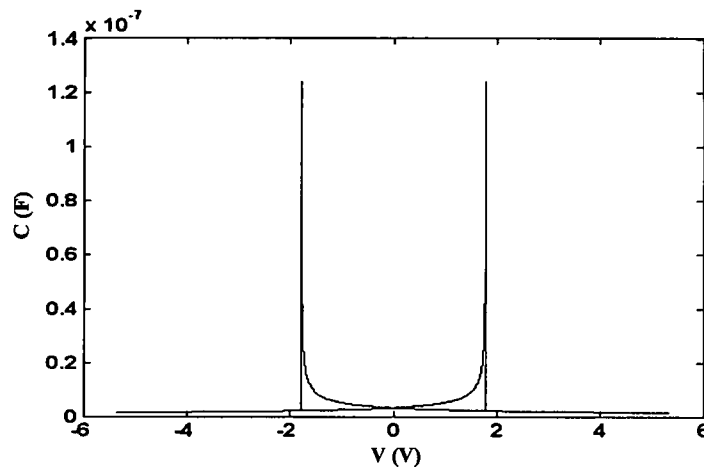


Figure 5.3.10. Ideal capacitance of a thin film capacitor.

5.3.5.2. Practical hysteresis loop and capacitance

A practical hysteresis loop comes from (3.17). The dissipation effect of R_S needs to be taken into consideration. Since this is a nonlinear system, a numerical method is used for the analyses. The first case considered is when the applied signal is large. Regardless of the initial condition of $Q(0)$, simulations show that the stable hysteresis loop always converges and depends on the applied signal frequency and amplitude. Figure 5.3.11 gives the simulated hysteresis loops for different applied signals where V_0 is the amplitude of the applied signal, f is the signal frequency and

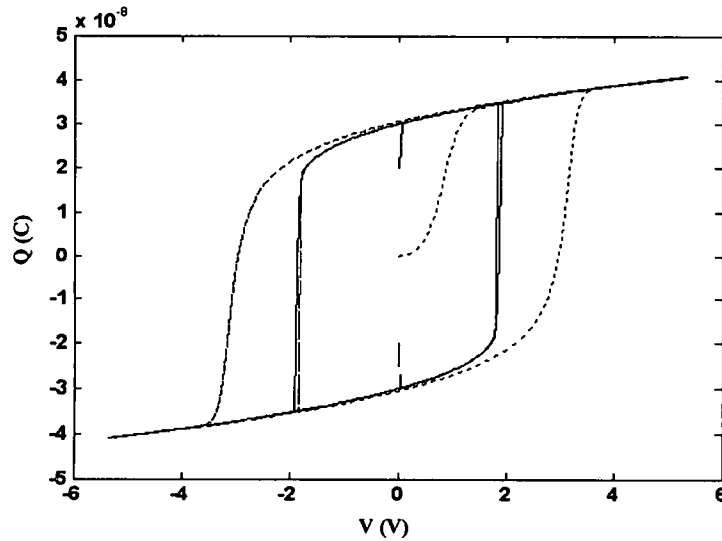


Figure 5.3.11 Hysteresis loops from different applied signals. The dotted line stands for $V_0=3 V_C$, $f=1$ MHz, $Q(0)=0$ C; the dashed line stands for $V_0=1.5 V_C$, $f=10$ kHz, $Q(0)=-0.2 \times 10^{-8}$ C and the solid line stands for $V_0=3 V_C$, $f=10$ kHz, $Q(0)=0.2 \times 10^{-8}$ C.

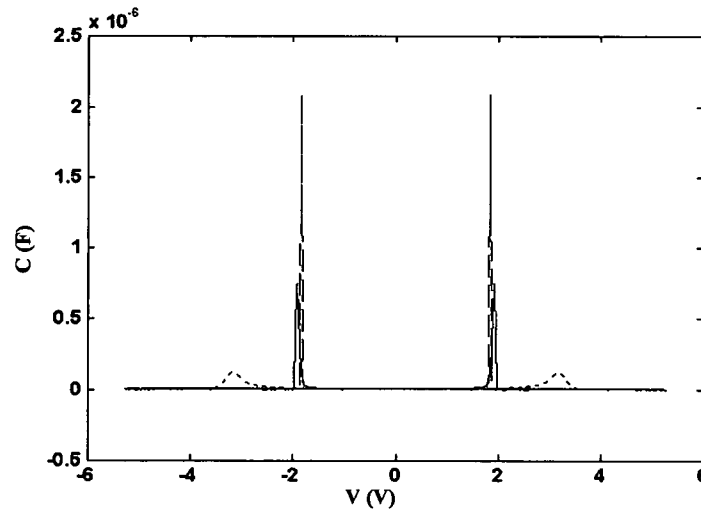


Figure 5.3.12. Large signal capacitance with different applied signals as described in Figure 5.3.11.

$Q(0)$ is the initial charge on the capacitor. R_S is set to be 1.53Ω and is related to γ as $R_S=\gamma L/S$. As the applied signal frequency and amplitude decrease, dQ/dt approaches zero and (3.17) changes to (5.3.13). Therefore, the stable hysteresis

loop shrinks and approaches the ideal hysteresis loop. The hysteresis loop dependence on applied signal frequency has also been reported in the literature [76]. Figure 5.3.12 gives the corresponding large signal C-V curves. They are obtained as the derivative of the hysteresis loops. If we think that the voltage at the capacitance peak is the observed coercive voltage, it is found that the observed coercive voltage increases and the capacitance peak value decreases as the voltage and frequency of the applied signal increase. The reason that its peak values are higher than the ideal C-V curve is that there are not enough simulation points around the coercive voltage for the ideal C-V curve.

The second case considered is when the applied amplitude is small and the gradually stable conditions are not always met in the whole plane. Simulation shows that two stable hysteresis loops exist for a small applied signal and it depends on the initial condition $Q(0)$. In Figure 5.3.13 the curve in magenta is the ideal hysteresis loop for reference. All the small signal hysteresis loop was obtained by simulation with an applied AC signal $V=0.2\sin(2\pi\times 1000t)$. Hysteresis loop 1 is obtained with a bias voltage of 0.9 V. Starting from $Q(0)=-0.2\times 10^{-8}$ C, it quickly moves to the rising phase of the ideal hysteresis loop and become stable. Hysteresis loop 2 is obtained with a bias voltage of 0.9 V too. But its initial condition is $Q(0)=0$ C. Its stable status is on the decreasing phase of the ideal hysteresis loop. Hysteresis loop 3 is obtained with a bias voltage of 1.6 V and initial condition of $Q(0)=-0.2\times 10^{-8}$ C. It initially follows the rising phase of the ideal hysteresis loop. Once the total applied voltage (bias plus small AC voltage) reaches the coercive voltage, it makes the film switch and film polarization goes to the one value range (one real Q for a given V). When the applied AC signal reduces, the polarization will follow the decreasing phase of the ideal hysteresis loop and will become stable over there. Dividing the

difference between the maximum and the minimum polarization of the stable hysteresis loop by the peak-peak value of the applied AC signal, we have the small signal capacitance of hysteresis loop 1, 2 and 3 as 5.0 nF, 2.76 nF and 2.34 nF separately. The calculated ideal capacitance corresponding for voltage 0.9 V and 1.6 V on rise/decrease sides are 4.80 nF/2.55 nF and 11.6 nF /2.22 nF. If we realize that the stable hysteresis loop 3 is on the decreasing side, the small signal C-V capacitance agrees well with the ideal capacitance. If the amplitude of the AC signal for hysteresis loop 3 is reduced to 0.1V, the maximum applied voltage applied to the FE film will be less than the coercive voltage and the stable curve will stay on the rising side of the ideal hysteresis loop. Simulation gives the small signal capacitance to be 12.4 nF and is close to the ideal capacitance value on rising phase. It is therefore concluded that the ideal C-V curve coming from the ideal hysteresis loop is actually the small signal C-V curve. In practice small signal capacitance are also affected by signal frequency. Since the applied signal amplitude is very small, the effect is dQ/dt can be ignored under some frequency. This makes its value close to the ideal capacitance value. On the other hand, in practice a small signal C-V curve is measured with an AC signal that has definite amplitude V_0 . There are two clearance ranges around the ideal coercive voltages: $[V_C - V_0, V_C]$ and $[-V_C, -V_C + V_0]$, where the measured capacitance does not follow the ideal capacitance since the film switches and the stable hysteresis loop jumps to the opposite phase. This makes the peak values of practical small signal C-V curves are much lower than the ideal values. Figure 5.3.11, Figure 5,3,12 and (3.18) show that the practical hysteresis loops are affected by the material's viscosity, measuring signal frequency and amplitude. It makes it difficult to extract the real coercive voltage of the film. Simulation shows that when a biased small AC signal is applied,

the switching of the film only depends on whether the maximum total voltage exceeds the ideal coercive voltage. By controlling the magnitude of the small AC signal, it is possible to obtain more accurate coercive voltage from the small signal C-V curves since the film switch always happens at voltages $V_C - V_0$ and $-V_C + V_0$.

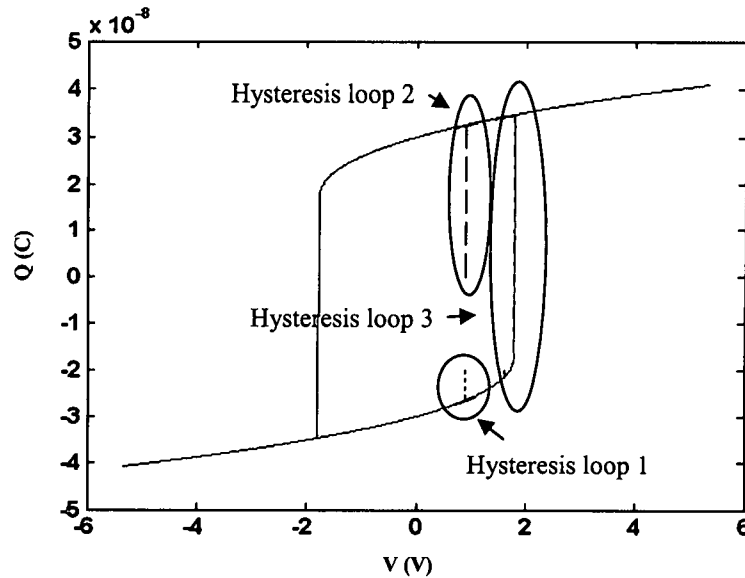


Figure 5.3.13. Hysteresis loops of small AC signal.

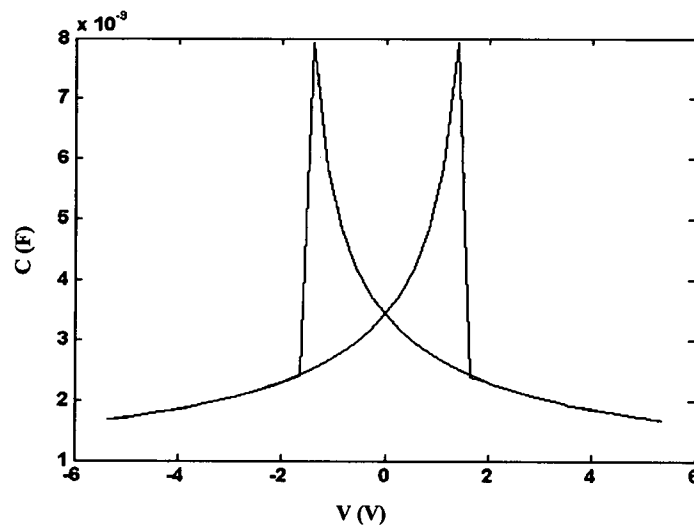


Figure 5.3.14. Small signal capacitance of a thin film FE.

To get the small signal C-V curve, the applied signal amplitude is set to be 0.2 V and its frequency is set to be 1 kHz. Its bias voltage is set to sweep from -5.3 V to 5.3 V

and back to -5.3 V. 121 points are simulated. For every bias the polarization on the ideal hysteresis loop is set to be the initial condition. Figure 5.3.14 gives the simulation results. Like the measurements, its peak values are much smaller than the large signal C-V curve.

5.4 The effects of capacitance nonlinearity on the application of EMC

5.4.1 Filtering properties

The C-V relations of an AFE/FE capacitor can be complicated. To simplify the calculation, a polynomial can be used to express the relationship between the capacitance and DC bias voltage as:

$$C = C_0 * \sum_{i=1}^n k_i V^i, \quad (5.4.1)$$

where C_0 and k_i are constants and V is the applied voltage.

In [65] one AFE capacitor was introduced. A simple expression is used in this paper to express the C-V relationship as

$$C = C_0(1 + kV^3), \quad (5.4.2)$$

where $C_0 = 48$ nF and $k = 2 \times 1/V_{\max}^3$.

In the above V_{\max} is the maximum DC bias for the capacitor to indicate antiferroelectric property. Since the dielectric constants of FE and AFE are related with the applied electric field strength. The C-V curves of FE/AFE can be adjusted by changing the thickness of the films in the capacitors to make AFE/FE capacitors effective in PCB and IC applications. Mostly V_{\max} is set to be 7.5 V here.

A pure FE capacitor that demonstrates ferroelectric property for all the DC bias is used for analysis. The mathematical expression of the capacitance is assumed to be

$$C = C_0(1 - kV^3), \quad (5.4.3)$$

where $C_0=144 \text{ nF}$ and $k=2 \times 1/7.5^3$.

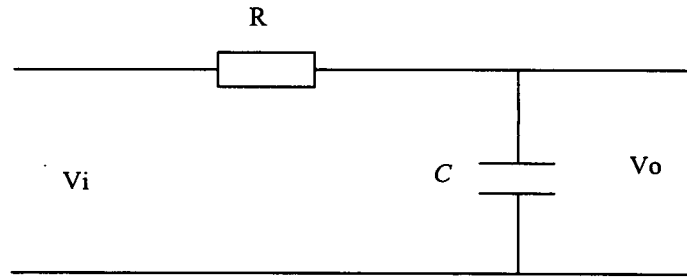


Figure 5.4.1. An RC filter for power bus noise decoupling.

Figure 5.4.2 gives a RC filter circuit composed of a capacitor and an equivalent resistor. This is a typical model for the power bus noise decoupling circuit used in a PCB. If the capacitor is a regular (fixed value) one, the circuit can be easily analyzed as a linear system. However; if the capacitor is made of ferroelectrics or antiferroelectrics, the analysis shall start from the following differential equation:

$$\frac{V_i - V_o}{R} = \frac{d(V_o C)}{dt} \quad (5.4.4)$$

According to (5.4.1) one has $C=C_0(1+kV_o^3)$ for an AFE capacitor. Substituting (5.4.1) into (5.4.4), one gets

$$\frac{dV_o}{dt} = \frac{V_i - V_o}{RC_0(1+4kV_o^3)} \quad (5.4.5)$$

With $V_i=5+2\sin(2\pi ft)$ V, $R=0.5 \Omega$ and $k=2 \times 1/7.5^3$ the filter output was obtained by means of numerical simulation in the frequency range from 2 MHz to 30 MHz. As a comparison, the output of the filter composed of a regular capacitor with a fixed value $C=C_0(1+k \times 5^3)$, which is thought to be the nominal value of the AFE capacitor's capacitance, is also given in Figure 5.4.2. Generally, the output of the filter with an AFE capacitor is considerably lower than that of the filter with a regular fixed value capacitor.

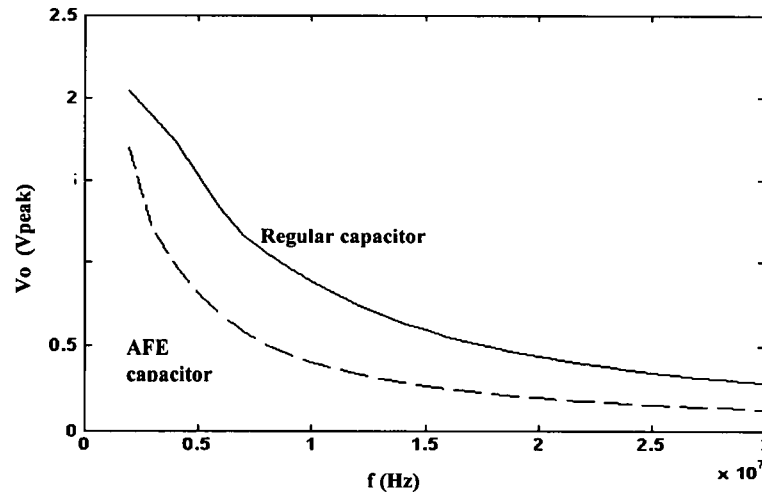


Figure 5.4.2. Output of the RC filter with a AFE and regular capacitors.

Simulation results show that the ratio of the output voltage of the filter with a regular capacitor to that with an AFE capacitor at 20 MHz is about 2.22. It is almost a 7 dB difference. Further simulation shows that the difference of the filtering properties of the filters depends on the working point of the AFE capacitor. As the DC bias voltage goes higher in the antiferroelectric range, the AFE capacitor demonstrates stronger filtering capability. This result can be explained from (5.4.5). With a regular fixed value capacitor, the denominator of the right side of (5.4.5) is $RC_0(1+k \times 5^3)$. With an AFE capacitor the denominator becomes $RC_0(1+4kV_o^3)$. There is a difference of coefficient 4 between the two terms. As DC component in V_i increases, V_o also increased, the influence of constant 1 in the term $1+4kV_o^3$ reduces and the filtering ability of the AFE capacitor increases.

At this point one will have a natural feeling on the filtering properties of FE capacitors. Since the capacitance of a FE capacitor decreases with the increase of the applied voltage, FE capacitor will have a weaker filtering capability than that of a regular capacitor with same nominal capacitance. With $C=C_0(1-kV_o^3)$ one gets the differential equation for the output of a filter with a FE capacitor as

$$\frac{dV_o}{dt} = \frac{V_i - V_o}{RC_0(1 - 4kV_o^3)} \quad (5.4.6)$$

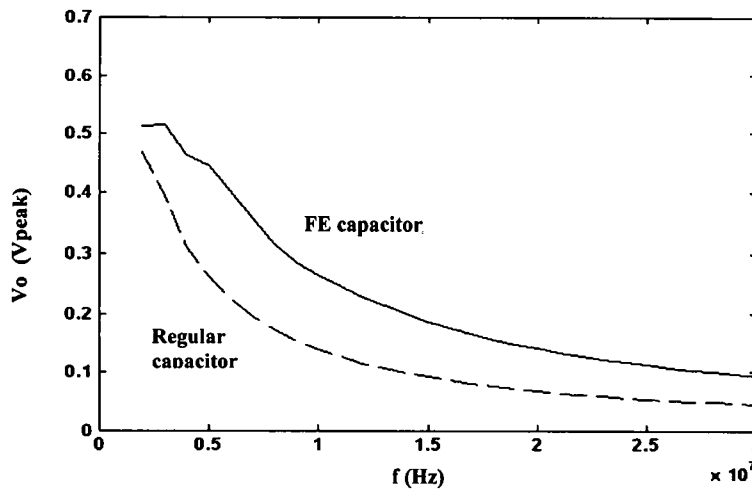


Figure 5.4.3. Output of the RC filter with a FE and regular capacitors.

With $V_i = 5 + 0.5 \sin(2\pi ft)$ V, $C_0 = 144 \text{ nF}$ and $k = 2 \times 1/12^3$, one gets the output response of the filter in the frequency range from 2 MHz to 30 MHz. As a comparison, outputs of the filter with a regular fix value capacitor $C = C_0(1 - k \times 5^3)$, which is thought to be the average capacitance value of the FE capacitor, is also given in Figure 5.4.3. Generally, the output of the filter with a FE capacitor is considerably higher than that of the filter with a regular fixed value capacitor. Here the AC signal amplitude was changed from 2 V to 0.5 V and constant k was changed from $2 \times 1/7.5^3$ to $2 \times 1/12^3$ to make the simulation stable.

5.4.2 Self resonance

One factor that needs to be considered in EMC application for a capacitor is its self-resonance. At a frequency, the parasitic inductance and the design capacitor has an equal reactance [93].

Figure 5.4.4 is an equivalent circuit of a capacitor. The impedance of the whole component is

$$Z = j2\pi fL + \frac{1}{j2\pi fC} + R. \quad (5.4.7)$$

The self-resonance frequency is

$$f_0 = \frac{1}{\sqrt{2\pi LC}}. \quad (5.4.8)$$

Normally, the impedance decreases with increasing frequency until the frequency reaches the self-resonance frequency, above which impedance increases with increasing frequency. It is generally the self-resonant frequency that limits the useful frequency range of a capacitor.

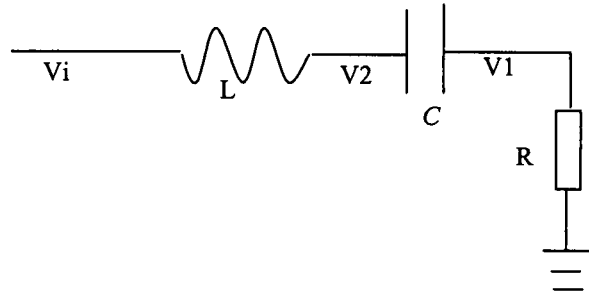


Figure 5.4.4. An equivalent circuit of a capacitor

According to (5.4.8), self-resonance frequency decreases with the value of capacitance. In the above section, AFE capacitor shows an “increased capacitance” in the RC filter. It is useful to know whether this “increased capacitance” will be reflected in the self-resonance. The investigation was started by set the status equation of the circuit in Figure 5.4.4 as

$$\frac{V1}{R} = \frac{d}{dt}[(V2 - V1)C] \text{ and} \quad (5.4.9)$$

$$\frac{dV1}{dt} \frac{L}{R} = V_i - V2. \quad (5.4.10)$$

Using (5.4.2), one gets

$$\frac{dV1}{dt} = \frac{V_i - V2}{L} R \text{ and} \quad (5.4.11)$$

$$\frac{dV_2}{dt} = \frac{V_1}{RC_0(1+4k(V_2-V_1)^3)} + \frac{V_i-V_2}{L}R. \quad (5.4.12)$$

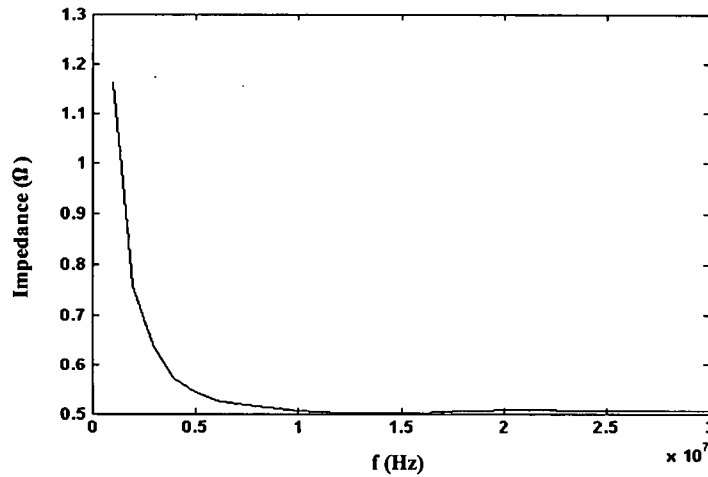


Figure 5.4.5. Series impedance of an AFE capacitor vs frequency

Using a numerical method, these equations can be solved. Once V_1 is obtained the input current can be obtained as $i_i = V_1/R$ and the magnitude of the impedance is obtained as the ratio of amplitude of V_i (AC component) to the amplitude of i_i . An example is given for $V_i = 5 + 2\sin(2\pi ft)$, $L = 1$ nH, $R = 0.5 \Omega$, $C = 144 \times (1 + kV_i^3)$ nF, where $k = 2 \times 10^{-3}$. The result is given in Figure 5.4.5. From simulation results, it can be seen that the self-resonance happens at around 13 MHz. Using the average capacitance $C = 48 \times (1 + k \times 5^3) = 76.4$ nF, one gets a predicted self-resonance

frequency for a regular capacitor as $f_0 = \frac{1}{\sqrt{2\pi LC}} \approx 18.2$ MHz. Since $13 \times \sqrt{2} \approx 18.4$, it

can be stated that the AFE has increased the capacitance by about 2 times. This conclusion complies with the results in the above section where the AFE reduced the output of the filter by almost 7 dB.

5.4.3 Parallel resonance

Another important factor that needs to be considered in the EMC application for capacitors is the parallel resonance. This normally happens when capacitors with different values, or different dielectric types, are connected in parallel (as with a bypass and supply decoupling capacitors) [93]. At a frequency, the parasitic inductance of other components in parallel with the design capacitor has an equal reactance. When parallel resonance happens, the design capacitors show high impedance and this will reduce the decoupling effect. One example is given in [56] where a 22 μF bulk decoupling capacitor resonates with the interplane capacitance. In [57], the high dielectric constant thin film embedded capacitor also demonstrates parallel resonance. FE materials have much higher dielectric constant. This makes it attractive to use FE/AFE materials between power and ground planes to reduce noise. It is valuable to investigate the performance of FE. AFE materials embedded capacitors. Figure 5.4.6 shows the model of the parallel resonance circuit. C is the design (interplane) capacitance. L_b is the packaging inductance of the bulk capacitor which contributes to the parallel resonance. C_b is the capacitance of the bulk capacitor. Since the value of C_b is much higher than C , C_b is ignored in the simulation with proper processing of V_i .

To get the impedance of the model, one can start from the following equations:

$$\frac{dI_1}{dt} = \frac{V_i}{L} \quad \text{and} \quad (5.4.13)$$

$$I_2 = \frac{d(V_i C)}{dt} . \quad (5.4.14)$$

Once I_1 and I_2 is obtained, the impedance of the model is obtained as

$$Z = \frac{V_i}{I_1 + I_2} . \quad (6.4.15)$$

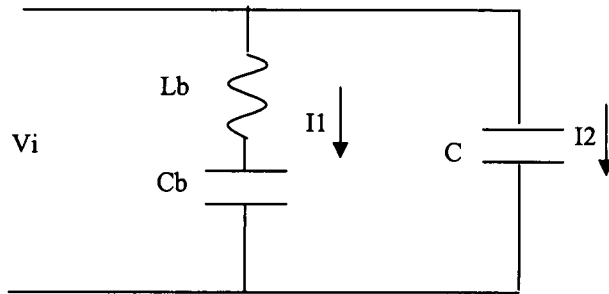


Figure 5.4.6. An equivalent circuit for parallel resonance

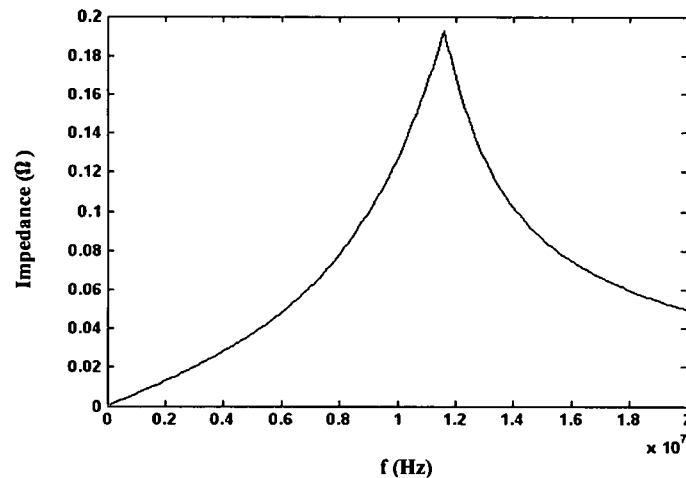


Figure 5.4.7. Parallel impedance of an AFE capacitor vs frequency.

Figure 5.4.7 shows the simulation results for an AFE capacitor. With $C=48(1+kV_i^3)$ nF, $L=1$ nH and $k=2 \times 1/7.5^3$. Study of the results shows that the circuit resonates at around 11.59 MHz and the resonance impedance is about 0.193 ohm. Calculation on the circuit with a regular fixed value capacitor and with a nominal capacitance $C=48(1+k \times 5^3)=76.4$ nF gives a resonance frequency around 18.2 MHz and very high resonance impedance (theoretically, infinite). The shifting of the resonance frequency with an AFE capacitor can be explained by the assumption that AFE has increased capacitance and it is consistent with previous results on filtering properties and self-resonance. The great reduction in resonance impedance by an AFE capacitor is a very useful feature to EMC application. So far, its mechanism is not very clear. One possible reason is that AFE capacitor is not a linear component.

While I1 has the same frequency as Vi, the frequency of I2 will shift from that of Vi and the final result is that resonance effect is reduced.

5.5 Performance of thin film PZT in EMC decoupling

In last section, the theoretical analyses were based on the assumption of simple C-V relationships. This chapter will give a more comprehensive study on the study of decoupling effects of thin film PZT capacitors. Measurements on their filtering results and impedance were carried out and compared for FE and commercial off-the-shelf capacitors. Equivalent circuit models were provided for analysis. Finally, mechanisms for the performance difference are investigated.

5.5.1 Experimental

Two kinds of measurements were carried out in this paper. For the study of filtering properties of thin film FE capacitors, measurements were carried on three capacitors: regular polyester film capacitor with a capacitance of 148.7pF (Cap Pol); thin film FE capacitor with a capacitance of 165.5 pF (cap FE1) and thin film FE capacitor with a capacitance of 62.9 pF (Cap FE2). The FE capacitors were provided by Radiant Technologies, Inc. They are composed of undoped 20/80 PZT thin films which have a thickness of 255nm and area of 10^{-8} m^2 and $4 \times 10^{-9} \text{ m}^2$. All the capacitors show high parallel resistance. Among them Cap FE1 has a parallel resistance of 39 M Ω .

5.5.1.1 Filtering properties

One common EMC application of capacitors is the decoupling of the noises on power bus [15-16]. Decoupling capacitors are normally implemented directly between power bus and ground to reduce the noise in the power bus. They can be divided into two categories. While bulk decoupling capacitors are responsible for the

decoupling of low frequency noise in a section of a PCB and have larger capacitance; local decoupling capacitors are responsible for the decoupling of higher frequency noise from particular IC and have smaller capacitance. Figure 5.5.1 shows the experimental schematic for the measurement of decoupling effect of FE capacitors. The decoupling effect of a capacitor was evaluated according to its insertion loss (IL). That is the ratio of the received signal without and with the capacitor and can be expressed as

$$IL(\text{dB}) = 20\log_{10}\left(\frac{2V_o}{V_s}\right). \quad (5.5.1)$$

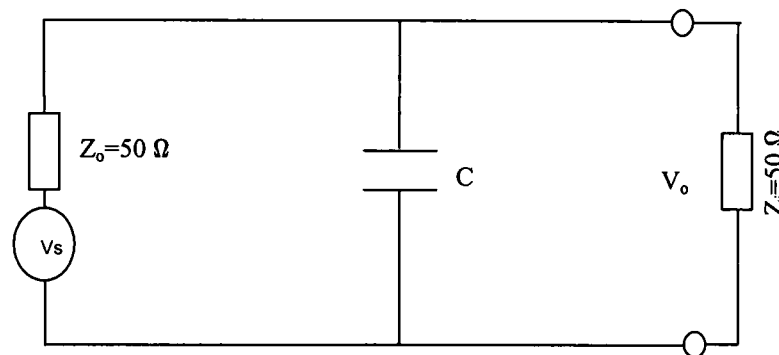


Figure 5.5.1. Schematics for the setup of measurement on decoupling effect of capacitors.

All the insertion losses were measured with a signal level set to be 0 dBm. Figure 5.5.2 gives the measurement results. The first observation is that the insertion losses from all the capacitors increase with frequency at lower frequency. After reaching its peak at a frequency it reduces with frequency. Another observation is that the polyester film capacitor has a peak insertion loss around 45 dB which is much larger than that of the FE capacitors, both having a peak insertion loss around 13 dB.

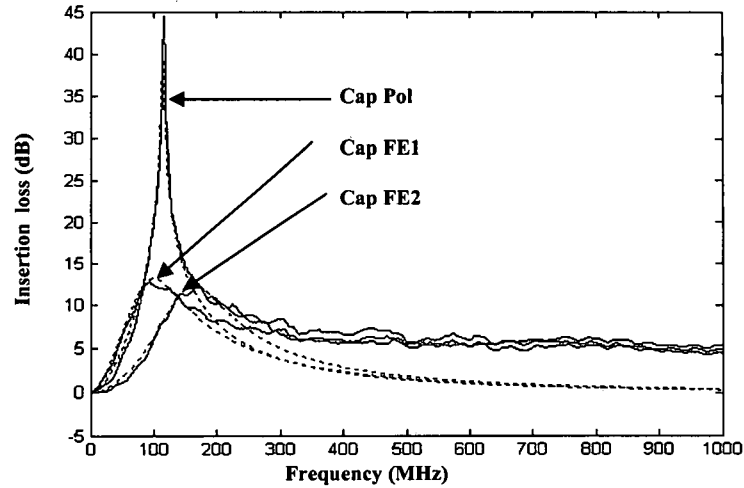


Figure 5.5.2. Measured and calculated insertion losses from capacitors. Solid lines stand for measurements and dotted lines stand for simulation.

To investigate the problem, a commonly used equivalent circuit for a capacitor was used. The equivalent circuit is given in Figure 5.5.3 and consists of a series resistor R_s which simulates the parasitic resistance of packaging leads and bonding wires, a series packaging inductor L_s which also comes from packaging leads and bonding wires, the nominal capacitor C_p and a parallel resistor R_p which accounts for the leakage conductance. If the capacitor C in Figure 8.2 is replaced by this equivalent circuit, (5.5.1) will change to

$$IL(dB) = 20 \log_{10} \left\{ \frac{(R_s + j\omega L_s + \frac{R_p}{1 + j\omega R_p C_p}) \parallel 50}{[(R_s + j\omega L_s + \frac{R_p}{1 + j\omega R_p C_p}) \parallel 50 + 50]} \right\}, \quad (5.5.2)$$

where \parallel indicates parallel connection and $\omega = 2\pi f$ and f is the measurement signal frequency.

With this equivalent circuit, the filter frequency response can be easily analyzed. At lower frequency, the component impedance reduces with frequency and the IL

increases with frequency. At a frequency the component impedance reaches its minimum value and IL reaches its maximum. This is called the resonant frequency f_r . After that the component impedance increases with frequency and the IL loss decreases with frequency.

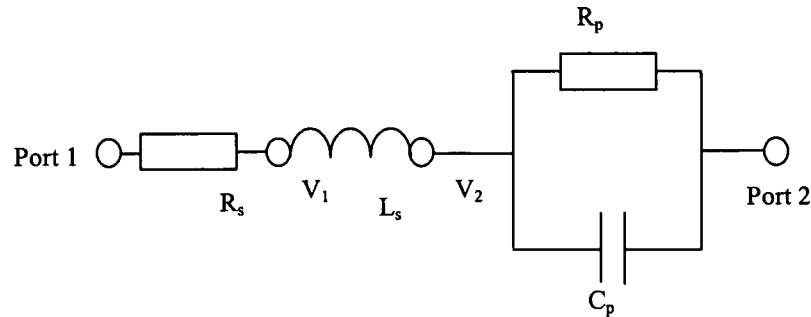


Figure 5.5.3. An equivalent circuit of a capacitor.

In (5.5.2) the value of C_p was given by direct measurement as given in section II. It was measured with a HP 4284A precision LCR meter and the measurement signal was set to be 0.2Vrms @ 1 kHz. L_s can be obtained according to the measured resonant frequency f_r and by the following formula

$$f_r = \frac{1}{2\pi\sqrt{L_s C_p}} \quad (5.5.3)$$

Since the measured R_p is very large compared to the C_p 's impedance, its effect can be ignored. By properly adjusting the value of R_s , a simulated insertion loss curve can be obtained in good agreement with the measurements for each capacitor. Table 5.5.1 gives the parameters for each capacitor. The corresponding simulated insertion losses are given in Figure 5.5.2 with dashed lines. It shows good agreements with the measurement below 200 MHz. Above that frequency, it is assumed that the parasitic parameters of the test fixture significantly influenced the measurements and the results and caused some deviations from simulations. Table 6.5.1 shows that FE thin film capacitors have much larger series resistance than the

polyester film capacitor. This is the component impedance observed at the resonant frequency and determines the peak insertion loss of the component. Since FE thin film capacitors have much larger series resistance than polyester film capacitor, they have much smaller peak IL than polyester film capacitor.

Table 5.5.1. Equivalent circuit parameters for each capacitor.

Capacitor	L_s (nH)	R_s (Ω)	C_p (pF)	R_p (M Ω)	fr (MHz)
Cap Pol	13	0.2	149	1	114
Cap FE 1	15	7	166	1	101
Cap FE 2	15	8	63	1	164

5.5.1.2 Impedance

Insertion loss of a capacitor is directly related to its impedance. To verify the correctness of the measurement and analyses given in previous section, the direct impedance of capacitors needs to be analyzed. Impedances were measured on the three capacitors used previously and they were obtained from the S_{11} parameter. Once S_{11} parameters were obtained the component impedance was calculated as

$$Z_{\text{mea}} = 50 \frac{1+S_{11}}{1-S_{11}}. \quad (5.5.4)$$

Figure 5.5.4 gives the measured impedances of the three capacitors in the frequency range of 300 KHz to 1GHz. All of them have the typical feature of capacitor's impedance. At the beginning, the impedance reduces with the frequency. After the resonant frequency, the impedance increases with the frequency. This feature can be clearly explained by the capacitor equivalent circuit diagram given in Figure 5.5.3. The impedance of the capacitor is given as

$$Z_{cal} = R_s + j\omega L_s + \frac{R_p}{1 + j\omega R_p C_p} . \quad (5.5.5)$$

At lower frequency the capacitance C_s dominates the performance, so that the impedance reduces with the frequency. At the resonant frequency given by (6.5.2) the reactance of the shunt capacitor and the equivalent series inductor will become oppositely equal. A series resonance will occur. The component will show the minimum impedance. Since the value of R_p is large, its effect can be ignored. The resonant impedance is actually determined by the series resistor R_s . Measurement data analyses gives the resonant frequencies and impedances of different capacitors as shown in Table 5.5.2. According to the capacitance measurement values as given in Table 5.5.1 the series inductance in the capacitors was calculated with (5.5.3) and is also given in Table 5.5.2. The values of the series resistors are very close to those extracted according to insertion loss measurement. It is verified that the FE thin film capacitors show a significant series resistance. The values of the series resonant frequency and extracted inductance are close to those given in Table 5.5.1. The difference may be due to the different fixtures used for the measurements.

Besides series resonance, parallel resonance can also take place between local decoupling capacitors and bulk decoupling capacitors. Figure 5.5.5 gives the equivalent circuit diagram. On the bottom is the bulk capacitor comprising of the inductance L_b , R_b , both coming from the packaging leads, and PCB trace and the nominal capacitance C_b . On the top is the local decoupling capacitor as described before. The impedance of total impedance measured at the site of the local decoupling capacitor is given as

$$Z_{par} = \frac{Z_{local} Z_{bulk}}{(Z_{local} + Z_{bulk})} , \quad (5.5.6)$$

where

$$Z_{\text{bulk}} = R_b + j 2 \pi f L_b + 1/(j 2 \pi C_b) \quad (5.5.7)$$

and Z_{local} is given by (6.5.5) and f is the signal frequency.

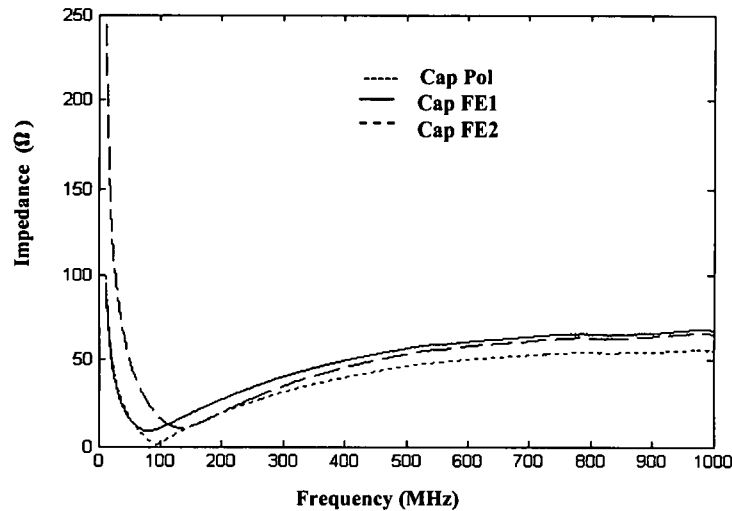


Figure 5.5.4. Measured impedances of capacitors.

Table 5.5.2. Capacitor equivalent circuit parameters extracted from impedance measurements.

Capacitor	$L_s(\text{nH})$	$R_s(\Omega)$	$C_p(\text{pF})$	$F_r(\text{MHz})$
Cap Pol	19	0.83	149	94
Cap FE 1	23	9.05	166	81
Cap FE 2	22	10.7	63	134

Since the value of the nominal capacitance the bulk capacitor is normally very large, its impedance is very small at our concerned frequency and its effect can be ignored here. At a frequency, the reactance of L_b in the bulk capacitor will have the same value as that of the local decoupling capacitor but with opposite sign and a parallel resonance will take place. The total impedance can vary greatly around the parallel

resonance. If the values of resistances are very small, the impedance will be very high and the decoupling effects will be greatly reduced.

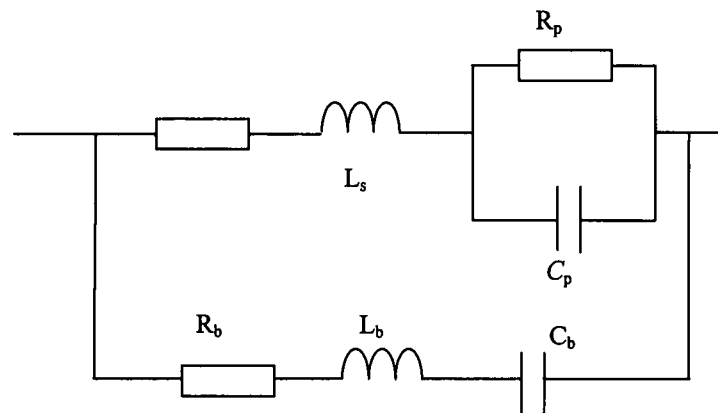


Figure 5.5.5. Equivalent circuit for parallel resonance.

Figure 5.5.6 gives the results of the impedance measurement made on different capacitors connected in parallel with an electrolytic capacitor of $22\ \mu\text{F}$. These measurements were made with the same setup as for the capacitor's direct impedance measurement. The only difference is that the capacitors are now biased with 3.3 V DC to simulate a printed circuit board environment. It is found that the polyester film capacitor gives an obvious parallel resonance around frequency 86 MHz with an impedance peak value of $22\ \Omega$. However, the FE capacitors don't show obvious parallel resonances. It indicates that the series resistance in the local decoupling capacitor plays an important role. The FE thin film has larger series resistance, therefore; has weaker parallel resonance. This is a valuable feature for the application of FE capacitors since parallel resonance is hoped to be damped as far as possible for EMC decoupling. Based on the parameters extracted for the local capacitors as given in Table 5.5.2 and by adjusting the values of L_b and R_b , simulation gives similar results although the magnitude have some difference and this may be due to the tolerance of the assumed values for L_b and R_b ,

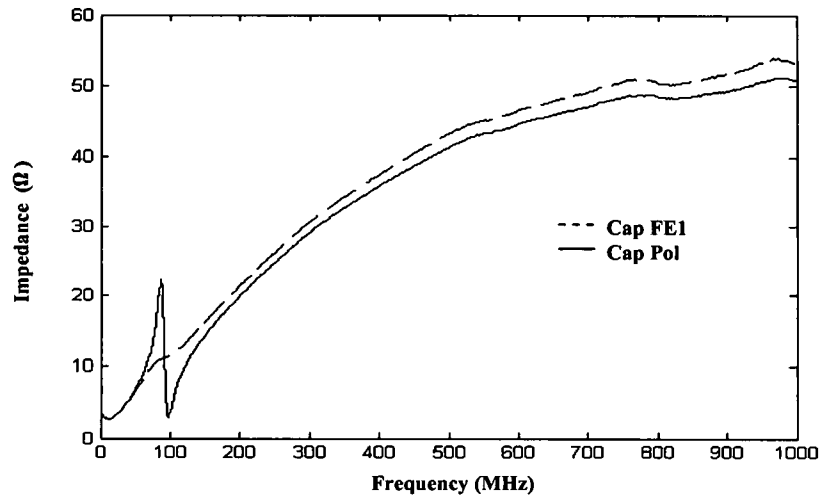


Figure 5.5.6. Measured impedances when bulk and local capacitors are connected in parallel.

5.5.2 Results and discussions

Previous results have shown that thin film FE capacitors have lower peak IL and weaker parallel resonance than polyester film capacitors and the differences are attributed to the significant series resistance of thin film FE capacitors. It is worth investigating the mechanism of the significant series resistance of thin film FE capacitors. As mentioned in section II the series resistance was originally used to represent the resistance coming from the packaging leads of the component and the bonding wire inside the component. From this point of view, the polyester film capacitor and the thin film FE capacitors shall not show any significant difference. Therefore, the significant resistance must have something to do with the FE thin film itself. As indicated before, the special property of FE thin film is its capacitance nonlinearity. Reference [94] shows that FE capacitors have smaller parallel resonance impedance magnitude than regular capacitors and assumes that this may be due to FE's capacitance nonlinearity. It is wondered here if the capacitance nonlinearity is the cause for the significant series resistance. In Figure 5.5.3 if one

lets port 1 be grounded, and apply a signal $V_a(t)=V_m\sin(2\pi ft)$ to port 2; where V_m is the amplitude of the applied signal and f is the frequency. The current I flowing through the component can be obtained by solving the following equations:

$$\frac{dV_1}{dt} = \frac{V_2 - V_1}{L_s} R_s, \quad (5.5.8)$$

$$\frac{dV_2}{dt} = \frac{dV_a}{dt} + \frac{V_a - V_2}{C_p R_p} - \frac{V_1}{R_s C_p}, \quad (5.5.9)$$

$$I = \frac{V_2 - V_1}{R_s}. \quad (5.5.10)$$

After that the impedance of the thin film capacitor can be calculated. In [94] the performance of the FE capacitor was just analyzed by assuming a simple voltage dependant capacitance. As given in [95], it is seen that even under small applied periodic signal, the polarization of the thin film FE capacitors has different mathematical description for increasing and decreasing process. The capacitance C_p can be expressed as

$$C_p^+ = \frac{\epsilon_0 \epsilon_f}{t} + k \frac{P_s}{2\delta} \text{sech}^2\left(\frac{V - V_c}{2\delta}\right) \text{ and} \quad (5.5.11)$$

$$C_p^- = \frac{\epsilon_0 \epsilon_f}{t} + k \frac{P_s}{2\delta} \text{sech}^2\left(\frac{-V - V_c}{2\delta}\right). \quad (5.5.12)$$

Where C_p^+ and C_p^- stands for the instantaneous capacitance for increasing signal and decreasing signal; ϵ_f is the linear portion of the FE dielectric constant; V_c is the coercive voltage, P_s is the spontaneous polarization of FE and t is the thickness of the FE film; $\delta = V_c \{ \ln[(P_s + P_r)/(P_s - P_r)] \}^{-1}$. Here k is introduced to take into consideration of non saturated polarization [92].

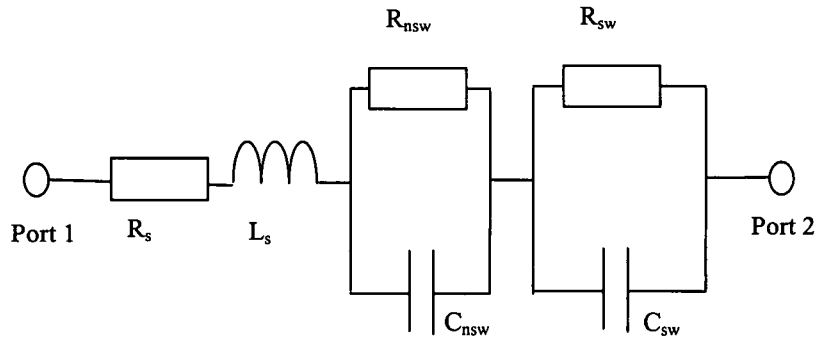


Figure 5.5.7. An equivalent circuit model for a thin film FE capacitor with a nonswitching layer.

[90] gives the values of these parameters for the FE used in this paper: $V_c=2.575$ V, $P_r=0.282$ C/m², $P_s=0.2829$ C/m², $\epsilon_f=463.5$. According to these, k is set to be 3 to keep the capacitance of thin film FE capacitor to be 166 pF at 0 V bias as measured. The signal amplitude used for the simulation is 0.2V; the value of the series resistance is 0.8 Ω ; the value of the series inductance is 23nH and the shunt resistance is 1 M Ω . The minimum impedance obtained from the simulation is 0.1 Ω . Therefore; introducing the capacitance nonlinearity doesn't increase the minimum impedance.

Another possible explanation for the significant series resistance of thin film FE capacitor is the nonswitching layer. According to [71, 96-97], a nonswitching layer (dead layer) can be formed between the electrode and the FE material. There are several reasons for that. If the space charge density near the electrodes is high, strong electric field will be generated there and the switching polarization will be always directed to one direction and does not respond to the applied signal. Cycling can cause the formation of conductive dendrites growing from the electrodes into the FE. The dendritic structures can shield the domains under the dendritic branches

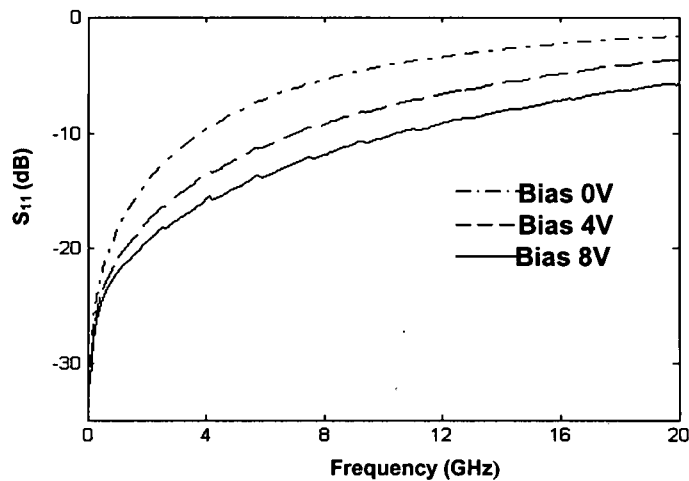
from the applied field, causing them not switch [71]. Once the nonswitching layer is considered in the application, the equivalent circuit of a thin film FE capacitor changes from Figure 5.5.3 into Figure 5.5.7. In Figure 5.5.7, FE film itself is considered to be a series connection of the switching layer (sw) and nonswitching (nsw) layer, each comprising of a capacitor and a resistor in parallel. Since $R_{nsw}C_{nsw} \ll R_{sw}C_{sw}$, R_{nsw} will dominate the impedance of the nonswitching layers before the frequency is very high and the observed series resistance in thin film capacitors are the sum of R_s and R_{nsw} .

5.6 Performance of thin film BST in EMC decoupling

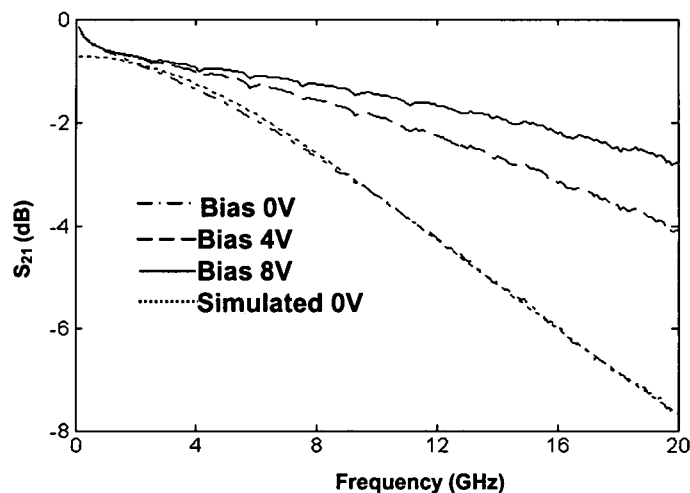
5.6.1 Experimental

In this study, we fabricated BST varactor shunt switches with varactor areas of $5 \times 5 \mu\text{m}^2$ and $20 \times 20 \mu\text{m}^2$ on a single high-resistivity Si chip with a 250 nm SiO_2 layer. Standard positive photoresist lift-off photolithography was used for the metal1 layer with a Ti adhesion layer (20 nm) deposited first, followed by 800 nm of gold and 100 nm of Pt in an e-beam evaporation system. After the metal1 layer was defined, the $\text{Ba}_{0.6}\text{Sr}_{0.4}\text{TiO}_3$ thin-film was deposited on the entire surface in a process-controlled pulsed-laser deposition system. The fabrication process for the nanostructured BST thin-films is described elsewhere [98]. After the BST deposition, the metal2 layer ($\approx 1 \mu\text{m}$) was defined and processed using the positive photoresist lift-off technique to complete the device fabrication. Important observations from the measurements were that the smaller the device area, the lower the insertion loss of the devices, the lower the isolation and the higher the reflection below resonance frequency. Figures 5.6.1 and 5.6.2 show the experimental swept frequency responses of with $5 \times 5 \mu\text{m}^2$ and with $20 \times 20 \mu\text{m}^2$ devices, respectively, for different bias voltages. For the 5×5

μm^2 device, the insertion loss is about 7.5 dB at 20 GHz and the zero-bias. The $20 \times 20 \mu\text{m}^2$ device showed higher insertion loss reaching 30 dB at 20 GHz and zero-bias. The results also show that the $20 \times 20 \mu\text{m}^2$ device generally has higher reflection than the $5 \times 5 \mu\text{m}^2$ device. The reason for that is that the $20 \times 20 \mu\text{m}^2$ device has a larger shunt capacitor made of the two overlapped metal and the BST film. Its capacitance is proportional to the area. Higher value capacitance gives rise to smaller shunt impedance and cause more reflection and insertion loss. The impedance of the capacitor directly determines the insertion loss and reflection.



(a)



(b)

Figure 5.6.1. Measurements of the $5 \times 5 \mu\text{m}^2$ device.

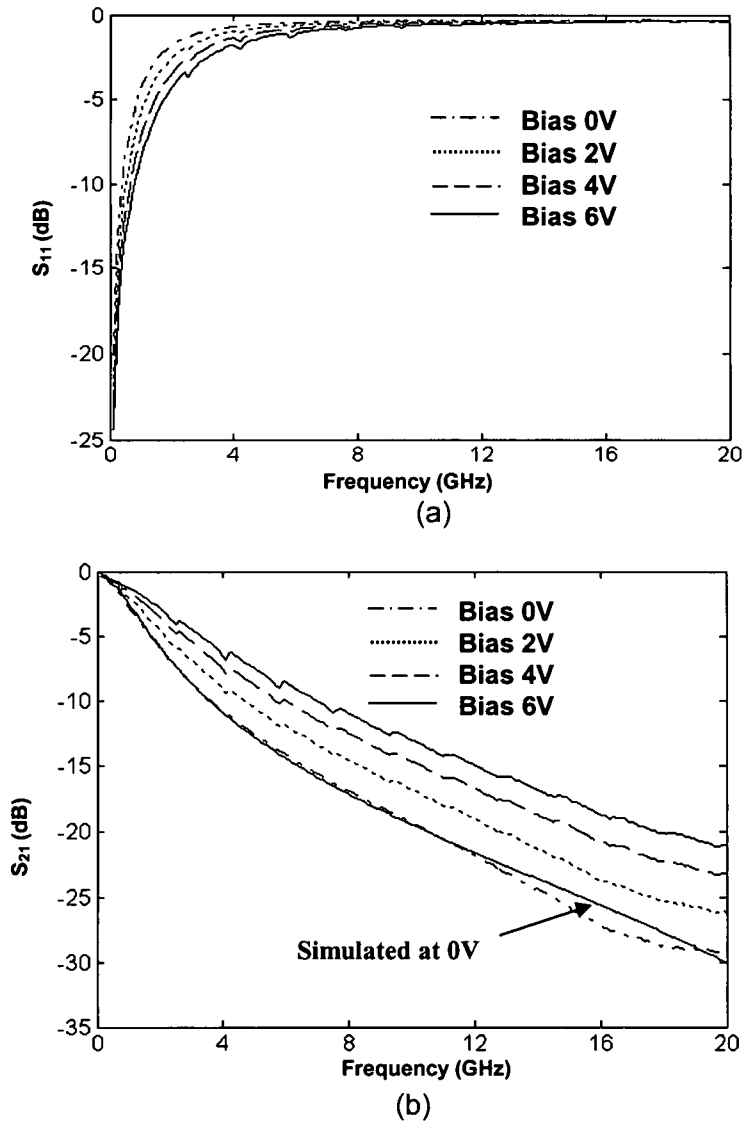


Figure 5.6.2. Measurements of the $20 \times 20 \mu\text{m}^2$ device.

5.6.2 Results and discussions

To extract the varactor impedance, an equivalent circuit for S_{11} parameter is given in Figure 5.6.3. The input impedance of port 2 of the VNA is 50Ω . The output impedance of port 1 of the VNA is 50Ω too. The shunt switch is modeled into a series connection of a PRC network and a SRL network. The normalized input impedance at the input port of the switch can be obtained from S_{11} as

$$S_{imp} = \frac{1 + S_{11}}{1 - S_{11}} \quad (5.6.1)$$

Considering that the switch is very tiny, the transmission lines effect inside the switched can be ignored. The impedance at the input port can be simply considered as the parallel connection result of varactor and 50 Ω . The varactor impedance of the switch is obtained as

$$f_{imp} = 50 \frac{S_{imp}}{1 - S_{imp}} \quad (5.6.2)$$

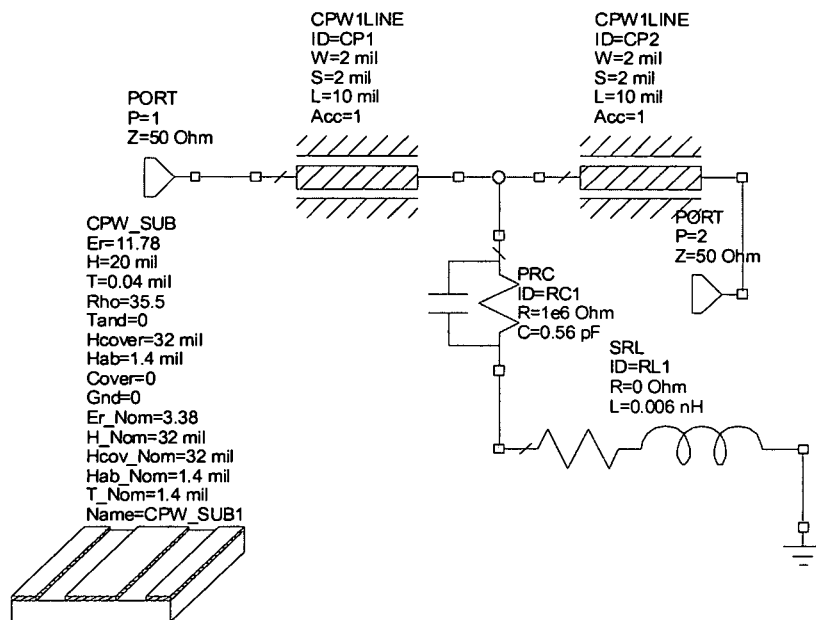
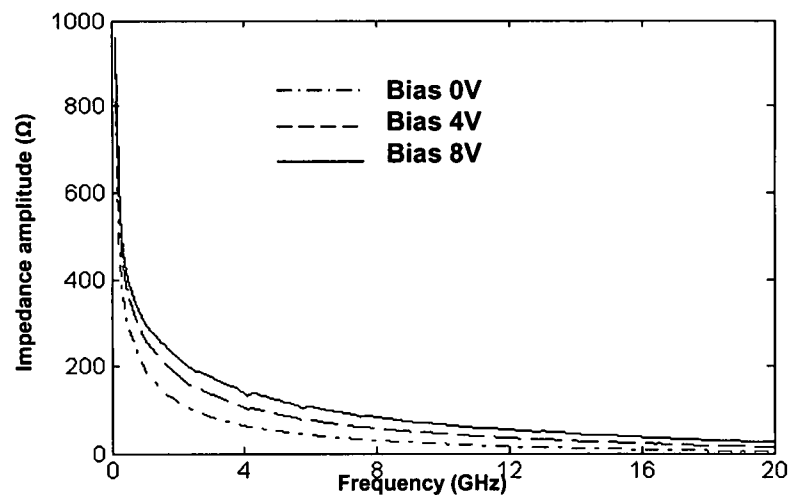


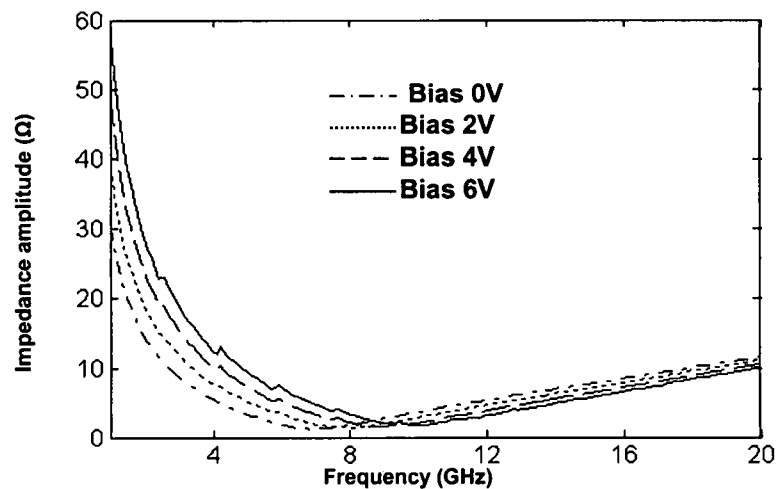
Figure 5.6.3. An equivalent circuit for S_{11} measurement.

Figure 5.6.4 gives the extracted varactor impedance for the $5 \times 5 \mu\text{m}^2$ and $20 \times 20 \mu\text{m}^2$ devices. In [99], a typical impedance property of a capacitor is described. The impedance can be considered as a series combination of a capacitance, inductance and a resistance. At low frequency, the impedance reduces with frequency since the capacitance dominates the impedance. At a frequency when the inductance and capacitance resonates, the impedance reaches its minimum which is equal to the resistance. After that the impedance increases with frequency since the inductance

dominates. For varactor with an area of $5 \times 5 \mu\text{m}^2$, the impedance reduces with the sweeping frequency in all the measured frequency range. No resonance takes place. For varactor with an area of $20 \times 20 \mu\text{m}^2$, The series resonance and resistance are extracted as 0V, $1.2 \Omega @ 6.9 \text{ GHz}$, 2V $1.4 \Omega @ 7.9 \text{ GHz}$, 4V, $1.6 \Omega @ 8.8 \text{ GHz}$, 6V, $1.8 \Omega @ 9.8 \text{ GHz}$. In [99], the significant series resistance is attributed to the interface. Here, no obvious interface resistance was found.



(a) $5 \times 5 \mu\text{m}^2$



(b) $20 \times 20 \mu\text{m}^2$

Figure 5.6.4. Extracted impedance of ferroelectric capacitors.

The varactor capacitance of the $20 \times 20 \mu\text{m}^2$ device was measured to be 6.23 pF at 0 V bias. The dielectric constant ϵ_r of $\text{Ba}_{0.6}\text{Sr}_{0.4}\text{TiO}_3$ is calculated to be 439. Simulation with AWR design environment for EM structures was conducted and results for the impedance of the $5 \times 5 \mu\text{m}^2$ and $20 \times 20 \mu\text{m}^2$ devices at zero bias. The parameters for the materials are given as SiO_2 ($\epsilon_r=3.9$, $\tan\delta=0.05$), Si ($\epsilon_r=11.7$, $\tan\delta=0.05$) and BST ($\epsilon_r=438$, $\tan\delta=0.05$). The simulation results for varactor impedance are given in Figure 5.6.5. They have the basic properties of the measurements. The difference may be due to the tolerance of the used material. Using the circuit schematics and parameters given in Figure 5.6.3, the simulated S_{21} values for the $5 \times 5 \mu\text{m}^2$ and $20 \times 20 \mu\text{m}^2$ devices at zero bias are given in Figure 5.6.1b and Figure 5.6.2b. The capacitance values of RC network are 0.56 pF and 4.91 pF separately. Good agreements are obtained between the measurements and the simulations.

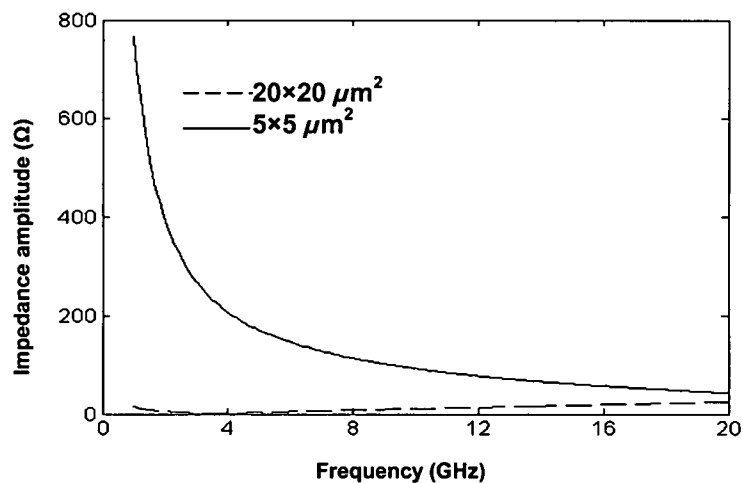


Figure 5.6.5. Simulated impedance.

CHAPTER 6

SUMMARY AND CONCLUSIONS

The applications of FE/AFE in memory have been widely studied in the literature. The study of EMC decoupling with ferroelectrics/antiferroelectrics is relatively new and its objective is to introduce FE/AFE into the EMC field and provide better understanding for the applications. The analyses and conclusions also benefit other circuit applications of FE/AFE. The results of the study are summarized as follows:

- (1) A model was developed for the description of FE electrical properties. Its polarization is divided into two portions: linear polarization and switching polarization. While linear polarization is proportional to the electric field, the relationship between the switching polarization and the electric field follows a hyperbolic function. By dividing the thin FE film into many layers in the thickness direction, the electric field inside the film can be obtained with a one dimensional numerical method.
- (2) Analyses show that the field distribution can be divided into two types: linear and non-linear distributions. While uniform space charge gives linear field distribution, the switching polarization around coercive field causes non-uniform space charge distribution, and hence causes non-linear field distribution. The non-linearity increases with the dopant-ion charge density and decreases with the linear permittivity of the FE thin film. This is important to prevent the breakdown of the film, and choose the maximum voltage that can be applied. Once the

applied voltage is strong enough to make all the switching polarization saturated in one direction, the field distribution will become linear.

- (3) The FE thin film peak capacitance reduces with the dopant-ion charge density since non-linearity of field distribution increases the variance of the permittivity of the FE thin film. For the same FE thin film capacitor with uniform dopant-ion charge, once the peak capacitance reduces, the large signal C-V curve is widened. The total area under the C-V curve between two large voltages with opposite signs is fixed and is determined by the spontaneous polarization of the material, the linear dielectric constant, the voltages and the thickness of the film.
- (4) For ideal hysteresis loop analysis, the interference between switching and linear polarization is considered. For a general electrical description of thin film FE in a practical circuit, interaction between dopant-ion charge density and switching polarization is neglected. Numerical analyses show that dopant-ion charge density in the film influence both the shape and offset of ideal hysteresis loop. However, hysteresis loop obtained with practical ST circuit always result in symmetrically stable shape and the dopant-ion charge has no effect on the hysteresis loop offset. Analysis shows that the initial offset comes from the initial condition (remnant polarization) of the film; the disappearance of the offset is due to the DC current leakage; the leakage current is affected by the measurement equipment input impedance and the equivalent leakage conductance of the film. Factors such as the signal source and leakage resistance in ST circuit can affect the appearance of the hysteresis loop.
- (5) Measurements on PZT thin films show that large signal C-V curves has much larger peak capacitance and sharper capacitance peak than small signal curves. Defect migration in thin film FE under a bias can cause its capacitance change, but it is not the cause for this capacitance change since defect migration will

make fluctuations in C-V curves. Since the measured capacitance didn't change with time under a bias and the electric properties of the measured film didn't change after small signal C-V measurement, electron trapping can not be the cause either.

- (6) The theory introduced by Miller and the Presach model can predict the reduction of small signal capacitance. However, the predicted small signal C-V curve only has one peak and doesn't agree with the measurements. According to the Landau-Khalatnikov circuit model, the ideal hysteresis loop is obtained when the effect of viscosity is neglected. The ideal capacitance is obtained as the derivative of the hysteresis loop. Practical large signal hysteresis loops including the effect of the viscosity are affected by the applied signal frequency and amplitude. The observed coercive voltage and peak capacitance are different from the ideal one and is affected by the applied signal. Practical small signal hysteresis loops can have two different stable statuses and it is related to the initial polarization. Small signal capacitance is actually close to the ideal capacitance when the bias voltage is far away from the coercive voltage. Depending on the small signal AC signal amplitude, the FE film switches to the opposite phase before the ideal coercive voltage. Therefore the polarization switching which is reflected in large signal C-V curves is missing in small signal C-V curves. This greatly reduces the peak value of small signal C-V curves. Properly controlling the amplitude of the small AC signal can give more accurate coercive voltage of the film from small signal C-V curves than from hysteresis loops.
- (7) Due to the hysteresis loop properties, the small signal capacitance of ferroelectrics/antiferroelectrics changes with the applied electric field/voltage. Simulation indicates that AFE shows an "increased capacitance" than its nominal

value based on DC bias and FE shows a "decreased capacitance" than its nominal value. Therefore AFE capacitors increase the filtering response of RC filters, whereas FE capacitors reduce the filtering response. Due to the "increased capacitance", AFE capacitors also reduce self-resonance frequency and parallel-resonance frequency. While the mechanism is not clear, it is a very useful finding that AFE greatly damps the parallel-resonance.

- (8) Measurements indicate that a FE PZT capacitor has much less peak insertion loss than that of a polyester film capacitor with close capacitance value. Analyses show that there exists a significant series resistance in thin film FE capacitors and it is this series resistance that reduces the peak insertion loss of thin film FE capacitors. Measurements and analyses also show that this resistance damps the parallel resonance when local decoupling capacitor and bulk decoupling capacitor are connected in parallel. Further analyses show that this large series resistance does not come from the capacitance nonlinearity. Instead, it is most likely due to the nonswitching layer (dead layer) that exists in FE film capacitors.
- (9) The experimental results obtained for BST-based varactor shunt switches of different sizes for RF performance evaluation and impedance extraction have been presented. The devices tested were fabricated on a single high-resistivity Si substrate. All the devices showed insertion loss tunability because of the tunability of the shunt capacitor. The impedance extraction showed that the equivalent series resistance of the shunt capacitor is small. No obvious interface resistance was observed. Simulation with AWR design environment was conducted and results agree with the measurements. Since $\text{Ba}_{0.6}\text{Sr}_{0.4}\text{TiO}_3$ is paraelectrics at room temperature, it indicates that the interface effects of FE

depend on the type of materials. This makes FE promising in the applications of EMC decoupling.

CHAPTER 7

SCOPE FOR FUTURE WORK

The results drawn from this project are comprehensive and valuable. However, the study has some limitations and further work can be conducted in the future.

1. The model developed is for one dimensional numerical method. The thin film FE is considered to be composed of many identical layers and all the layers have the same hysteresis loop. To get more accurate results and obtain the effects of more parameters like the size of the film, a three dimensional model may need to be developed.
2. The switching nature of FE domains with unsaturated hysteresis loop is currently not well addressed. The relationship between the large and small signal capacitance can be affected by the presence of space (defect) charge, grain boundaries and stress. Further work can be conducted to give direct analyses on unsaturated hysteresis loops.
3. The interface layers between thin film FE and electrodes have been widely studied in the literature. Most studies were focused on their effects on hysteresis loop and capacitance. In the EMC application of thin film FE, the resistance of the interface layers also plays an important role. The nature of the interface layer needs to be carefully investigated to give a correct model for the interface layers so that both the capacitance and resistance are taken into considerations.

4. Application of FE/AFE in PCBs and ICs as embedded decoupling capacitors is very valuable since it directly kills the noise source. The investigations into the application can be divided into two types. The first type, analyzed in this project, is to investigate the features of the embedded capacitors that have small sizes and can be treated as discrete capacitors. The second type is to investigate the features of the embedded capacitors that have large sizes. The transfer impedance concept needs to be investigated. Embedded decoupling capacitors made of different materials also need to be investigated.

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APPENDICES

1 Code to find the field distribution inside a thin film FE with space charge.

```
% This program calculates the applied voltage va when a field strength e0
% is given at the normal capacitor side is given. charge density=a*x+b
eef=350;
%eef=0;
ps=0.1;
ec=3500000;
delta=2000000;
N=1*10^24;
ee0=8.852*10^(-12);
eq=1.6*10^(-19);
thickness=0.25*10^(-6);
aa=-0*N/thickness;
bb=-2*N;
xnum=100;
dx=thickness/(xnum-1);
e0num=400;
%de0=70*ec/(e0num-1);
de0=40*ec/(e0num-1);
exnum=200;
dex=20*ec/(exnum-1);
%dex=60*ec/(exnum-1);
%for rise hysteressis loop Va rises
for i=1:e0num
    e0=-10*ec+(i-1)*de0;

    for j=1:xnum
        x=(j-1)*dx;
        for k=1:exnum
            tex(k)=e0-(k-1)*dex;
            eerr(k)=abs(ee0*eef*(tex(k)-e0)-1*ps*(tanh((-1*tex(k)-ec)/(2*delta))-tanh((-
1*e0-ec)/(2*delta))))+eq*(0.5*aa*x*x+bb*x));
        end
        [y,indexk]=min(eerr);
        exup(i,j)=tex(indexk);
    end
    polup(i)=ps*tanh((-1*e0-ec)/(2*delta))-ee0*eef*e0;
    %polup2(i)=ps*tanh((-1*exup(i,xnum)-ec)/(2*delta))-ee0*eef*exup(i,xnum);
```

```

    eex=ps*1/(2*delta)*sech((-1*exup(i,:)-ec)/(2*delta)).*sech((-1*exup(i,:)-
ec)/(2*delta))+ee0*eef;
    inveex=eex.^-1;
    invcap=sum(inveex)*dx;
    capup(i)=1/invcap;
    vaup(i)=-1*sum(exup(i,:))*dx;
    es=vaup(i)/thickness;
    polupeven(i)=ps*tanh((es-ec)/(2*delta))+ee0*eef*es;
    eexeven=ps*1/(2*delta)*sech((-1*es-ec)/(2*delta)).*sech((-1*es-
ec)/(2*delta))+ee0*eef;
    capupeven(i)=eexeven/thickness;
end
%for reducing hysteresis loop
for i=1:e0num
    e0=-10*ec+(i-1)*de0;
    for j=1:xnum
        x=(j-1)*dx;
        for k=1:exnum
            tex(k)=e0-(k-1)*dex;
            eerr(k)=abs(ee0*eef*(tex(k)-e0)+ps*(tanh((tex(k)-ec)/(2*delta))-tanh((e0-
ec)/(2*delta)))+eq*(0.5*aa*x*x+bb*x));
        end
        [y,indexk]=min(eerr);
        exdown(i,j)=tex(indexk);
    end
    poldown(i)=-1*ps*tanh((e0-ec)/(2*delta))-ee0*eef*e0;
    %poldown2(i)=-1*ps*tanh((exdown(i,xnum)-ec)/(2*delta))-
ee0*eef*exdown(i,xnum);
    eex=ps*1/(2*delta)*sech((exdown(i,:)-ec)/(2*delta)).*sech((exdown(i,:)-
ec)/(2*delta))+ee0*eef;
    inveex=eex.^-1;
    invcap=sum(inveex)*dx;
    capdown(i)=1/invcap;

    vadownd(i)=-1*sum(exdown(i,:))*dx;
    es=vadownd(i)/thickness;
    poldowneven(i)=-1*ps*tanh((-es-ec)/(2*delta))+ee0*eef*es;
    eexeven=ps*1/(2*delta)*sech((es-ec)/(2*delta)).*sech((es-ec)/(2*delta))+ee0*eef;
    capdowneven(i)=eexeven/thickness;
end
figure (1);
plot(vaup, polup, 'r');
hold on;
plot(vaup, polupeven, 'b:');
plot(vadownd, poldown, 'r');
plot(vadownd, poldowneven, 'b:');
xlabel('x applied volatge V');
ylabel('P polarization C/m2');
figure (2);
plot (vaup, capup, 'r');
hold on;

```

```

plot (vaup, capupeven, 'b:');
plot (vadown, capdown, 'r');
plot (vadown, capdowneven, 'b:');
xlabel('x applied volatge V');
ylabel('capacitance F/m2');
xx=[0:dx:thickness];

```

2 Code for the extraction of thin film FE hysteresis loop parameters

```

% extract parameters pr, vc, ps and er uC/cm2 without doping  data comes
% from LC equipment
er0=520;
pr0=27;
vc0=2;
ps0=27.01;
er=er0+[-0.3:0.03:0.3]*er0;
pr=1.1*pr0+pr0*[-0.3:0.03:0.3];
vc=1.1*vc0+vc0*[-0.3:0.03:0.3];
ps=1.1*ps0+ps0*[-0.3:0.03:0.3];
thickness=2.55*10^(-7);
e0=8.852*10^(-12);
min=10000000000;
len=length(vol);
for ernum=1:21
    for prnum=1:21
        for vcnum=1:21
            for psnum=prnum:21
                err=0;
                delta=vc(vcnum)/log((1+pr(prnum)/ps(psnum))/(1-pr(prnum)/ps(psnum)));
                for k=1:len-1
                    if vol(k+1)>vol(k)
                        polcal=ps(psnum)*tanh((vol(k)-
vc(vcnum))/(2*delta))+er(ernum)*e0*vol(k)/thickness*100;
                    else
                        polcal=-1*ps(psnum)*tanh((-1*vol(k)-
vc(vcnum))/(2*delta))+er(ernum)*e0*vol(k)/thickness*100;
                    end
                    err=err+(polcal-pol(k))^2;
                end
                if vol(len)>vol(len-1)
                    polcal=ps(psnum)*tanh((vol(len)-
vc(vcnum))/(2*delta))+er(ernum)*e0*vol(len)/thickness*100;
                else
                    polcal=-1*ps(psnum)*tanh((-1*vol(len)-
vc(vcnum))/(2*delta))+er(ernum)*e0*vol(len)/thickness*100;
                end
                err=err+(polcal-pol(len))^2;
                if err<min
                    min=err;
                    erindex=ernum;

```

```

        prindex=prnum;
        vcindex=vcnum;
        psindex=psnum;
    end
end
end
end
end
%calculate the hysteresis loop
delta=vc(vcindex)/log((1+pr(prindex)/ps(psindex))/(1-pr(prindex)/ps(psindex)));
for i=1:len-1
    if vol(i+1)>vol(i)
        polcal(i)=ps(psindex)*tanh((vol(i)-
vc(vcindex))/(2*delta))+er(erindex)*e0*vol(i)/thickness*100;
    else
        polcal(i)=-1*ps(psindex)*tanh((-1*vol(i)-
vc(vcindex))/(2*delta))+er(erindex)*e0*vol(i)/thickness*100;
    end
end
    if vol(len)>vol(len-1)
        polcal(len)=ps(psindex)*tanh((vol(len)-
vc(vcindex))/(2*delta))+er(erindex)*e0*vol(len)/thickness*100;
    else
        polcal(len)=-1*ps(psindex)*tanh((-1*vol(len)-
vc(vcindex))/(2*delta))+er(erindex)*e0*vol(len)/thickness*100;
    end
    plot (vol, pol, 'g');
    hold on;
    plot (vol, polcal, 'r');

```


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