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Tunable frequency selective surface and high-impedance ground plane using ferroelectric thin-films

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Tunable Frequency Selective Surface and High-Impedance Ground Plane Using Ferroelectric Thin-films

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By

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Abstract

TUNABLE FREQUENCY SELECTIVE SURFACE PLANE AND HIGH IMPEDANCE GROUND PLANE USING FERROELECTRIC THIN-FILMS

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This study is concerned with the proof of concept of the use of ferroelectric material, thin-film barium strontium titanate ($Ba_xSr_{1-x}TiO_3$, BST), for the development of tunable electromagnetic band gap structures in the form of a two-dimensional surface. Knowledge gained from previous experiments with devices using BST thin-films is extended to a larger planar surface. The presented study hopes to explore the concept of development of an electronically tunable frequency selective surface (FSS), or a high impedance ground plane (HIGP) using BST material for operation in the 5 to 40GHz range.

The basic concept relies on the development of a series *LC* resonance within the ground plane. The inductance is provided by inductive strips while the capacitance is provided by overlapping strip regions in a multi-layer structure separated by the BST thin-film. The dielectric constant of BST can be altered with the application of an electric field. BST based varactors are incorporated into

the inductive strip structure to form a high impedance ground plane which is electronically tunable. Several designs are proposed and analyzed using traditional lumped element analysis techniques based on finite element simulation results obtained from Sonnet. Biasing schemes are explored so that dc voltage supplies can be used to tune the device response. Devices are manufactured on thin-films deposited by sputtering and PLD process. The results proved to be lossy than expected, but clearly displayed the existence of a band gap.

Acknowledgments

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Chapter 1 Introduction

The knowledge of ferroelectric materials and their ability to change their dielectric constant in the presence of an electric field has been available to engineers since the middle of the 20th century. Engineers have used the properties of ferroelectric materials to scale down microwave devices due to their high dielectric constants, and use their variable dielectric permittivity to introduce a level of tunability into their devices. Barium strontium titanate ($Ba_xSr_{1-x}TiO_3$), often referred to as BST, is a ferroelectric material growing in importance for many applications. As the manufacturing procedures for the growth of ferroelectric materials in the form of thin-films are still underway, with time and energy, the quality and manufacturing scale of the films will increase. Microwave devices using BST thin-films have already been demonstrated as viable components for high frequency operation.

This work deals with the development of an electromagnetic bandgap structure in the form of a two-dimensional surface. Knowledge of microwave devices using BST is extended to incorporate periodic surfaces. Variations of periodic surfaces exist in the form of frequency selective surfaces (FSS), and high impedance ground planes (HIGP). This study will serve as an initial venture into the area by introducing tunability to periodic surfaces through the use of BST material. The primary goal is to demonstrate that an electromagnetic bandgap can be created

using BST using a planar surface. The performance levels of the device are of secondary importance.

The first chapter provides an introduction to the ferroelectric phenomenon and periodic surfaces in the form of FSS and HIGP. Ferroelectric materials have been widely studied and a great body of knowledge is already available. Their use in microwave devices in the form of thin-films is well understood. FSS have been around for a significant period of time and their design and analysis techniques are well established. HIGP are a more recent invention and their development, along with meta-materials, is still in progress.

The second chapter is devoted to the development of the two-dimensional surface. Simulation results obtained through Sonnet are the main source of material for analysis of various designs. Rigorous mathematical analysis is not conducted as there is currently no understanding of the device available based on existing techniques. Based on simulation results, designs are chosen for manufacturing and their results are presented in the third chapter. Final conclusions and ideas for further progress are presented in the final chapter.

1.1 Ferroelectricity and BST thin-films

1.1.1 Ferroelectricity

Ferroelectricity is a phenomenon in which polarization is induced in a dielectric by an external electric field [1]-[4]. In most dielectrics such a phenomenon is small, yet there are a group of crystals, called ferroelectrics, which show

significant levels of polarization when an electric field is applied. Within certain temperature regions, such crystals show spontaneous polarization and a hysteresis loop is formed by the relationship between the applied electric field and the resulting electric displacement. The Curie temperature marks the temperature below which ferroelectricity is observed and is also referred to as the Curie point.

The polarization is produced by the alignment of individual dipoles within the material. The creation of dipoles is dependent on the atomic and molecular arrangement within the material. Below the Curie point it is possible that there may be favored positions of the ions in a lattice structure, having lower total energy when compared to other orientations. The displacement of the ions from their relative symmetric position can cause a dipole to appear. The crystal is said to be spontaneously polarized if an overall dipole moment per unit volume is observed in the absence of an external electric field. The direction of net polarization is called the polar axis. Crystals having spontaneous polarization are named ferroelectric. Multiple adjacent dipoles having the same polarization direction form a domain. Neighboring domains are separated by a relatively small region called the domain wall, which is a neutral region where neither of the two domain orientations is particularly favored.

Some materials have multiple stable orientations with minimum energy. By the application of an electric field the dipoles within such a material can be made to switch from one stable orientation to another stable orientation in the direction of the applied field. The electric field provides the necessary energy for the

structure to go through unstable orientations and overcome energy barriers. This ability to switch the direction of polarization of individual dipoles is distinctive of ferroelectric materials. Ferroelectrics show both pyroelectric and piezoelectric behaviors, but the ability to switch domains using an external electric field sets them apart. Through the process of nucleation and domain wall motion, the domains are able to change their direction of polarization.

An interesting phenomenon resulting from domain wall switching is the formation of a hysteresis loop in the relationship between applied electric field and the resulting electric polarization as shown in Figure 1-1. Suppose that initially a crystal in its ferroelectric phase (below Curie temperature) has net zero polarization and the applied electric field is also zero. This point forms the origin *O* in the curves relating the applied electric field *E* and the polarization *P*. Now if the electric field is increased in the positive direction, the polarization will increase slowly, which is typical dielectric behavior. This region is depicted by the curve *OA*. As the electric field is increased further, domain switching begins resulting in a rapid increase in the polarization (*AB*). Once all the domains have been switched and the crystal is essentially a single domain crystal, a state of saturation is reached (*BC*). If the electric field is now decreased, the relationship will not follow the curve *CO*, but will move along *CD*. This is because the domains that were initially switched by the electric field in the positive direction are still oriented in the positive direction. Until an electric field is applied in the negative direction, the dipoles do not have enough energy to switch to their previous stable orientation. Even when the electric field is reduced down to zero,

a remnant polarization P_r (OD), is seen due to the switched domains. An electric field, called the coercive field E_c (OF), must be applied in the negative direction in order to neutralize the remnant polarization. Similar observation are made as those seen earlier as the electric field is further increased in the negative direction. In most cases when dealing with isotropic materials, a rotationally symmetric curve is obtained. A point of note is that the extrapolation of the linear region BC to the polarization axis gives the spontaneous polarization P_s (OE).

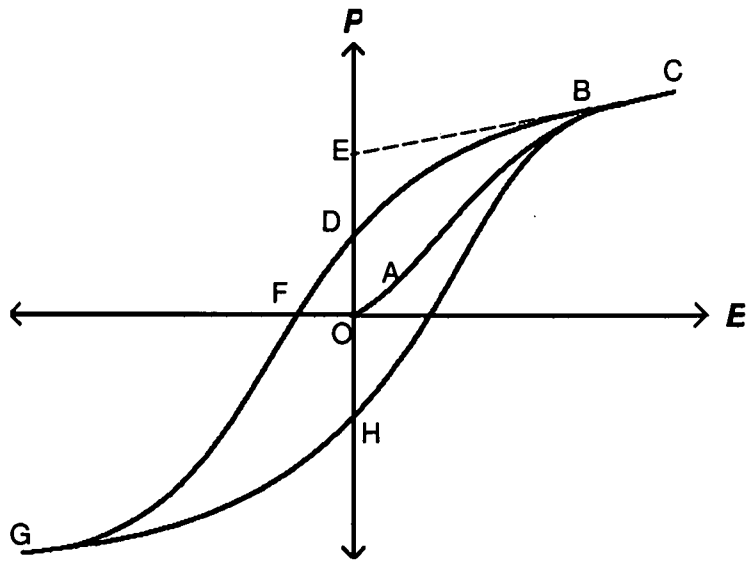


Figure 1-1: Ferroelectric hysteresis curve

The displacement vector D is dependent on the spontaneous polarization P_s, the electric field E, and the stress T. The piezoelectric equation relates the variables using the dielectric permittivity ε, and the piezoelectric coefficient d.

$$D = P_s + \varepsilon E + dT$$ **Equation 1-1**

As the relationship between *P* and *E* shows a hysteresis loop, the loop is also observed in the relationship between *D* and *E*. Relating *D* and *E* is important because it then allows for a measure of ε, which is usually defined as the derivative of the electric displacement with respect to the electric field. Due to the non-linear relationship between *D* and *E* it is possible to tune the dielectric constant of a ferroelectric by the application of an external field. This tunable property is critical for creating frequency/phase agile components and circuits using ferroelectrics.

For ferroelectric crystals there is considerable dependence of the dielectric permittivity on the temperature. Near phase transitions very high values of dielectric permittivity can be measured. In general, it is the Curie-Weiss Law that is used to relate the dielectric permittivity to the temperature above the Curie point (paraelectric phase).

$$\varepsilon = \varepsilon_0 + \frac{C}{T - T_0}$$ **Equation 1-2**

The temperature independent term ε_0 can usually be neglected near phase transition, *C* is the Curie constant which varies for different materials, and T_0 is the Curie-Weiss temperature. T_0 is not the Curie temperature T_c, but depending on whether the order of the transition is first or second order, T_0 is either less than or equal to T_c respectively. In general the permittivity of the ferroelectric falls of as the temperature is increased beyond the Curie point.

1.1.2 Ferroelectric Crystals

Barium titanate ($BaTiO_3$) belongs to the perovskite family of ferroelectric having the basic ABO_3 formula, where A and B are cations of different ionic radius, and O represent the oxygen anions, as shown in Figure 1-2. $BaTiO_3$ is one of the simpler perovskite structures and because its Curie point is 120ºC it exhibits ferroelectric properties at room temperature. Above the Curie point, $BaTiO_3$ has a stable cubic structure and does not have any spontaneous polarization. As the temperature is reduced through the Curie point, there is a phase transition and the lattice structure changes from a cubic to a tetragonal symmetry. There are other phase changes as the temperature is further reduced but the first transition is of concern for this work.

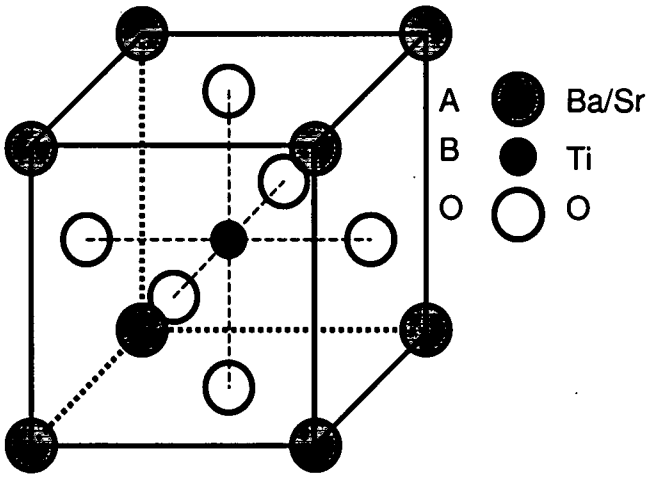


Figure 1-2: Perovskite structure

In the cubic structure there is perfect symmetry with all sides of the structure being the same length, thus there is no spontaneous polarization. When an electric field is applied to the cubic structure the positive and negative ions within

the lattice are displaced slightly forming dipoles in the direction of the applied field. These dipoles align in the direction of the electric field forming a measurable polarization. There is no hysteresis curve in the paraelectric phase, but because there is still a non-linear relationship between the polarization and the applied electric field, the dielectric permittivity is tunable. As predicted by the Curie-Weiss law, the dielectric constant reduces as the temperature increases, and the same is true for the loss tangent of the crystal.

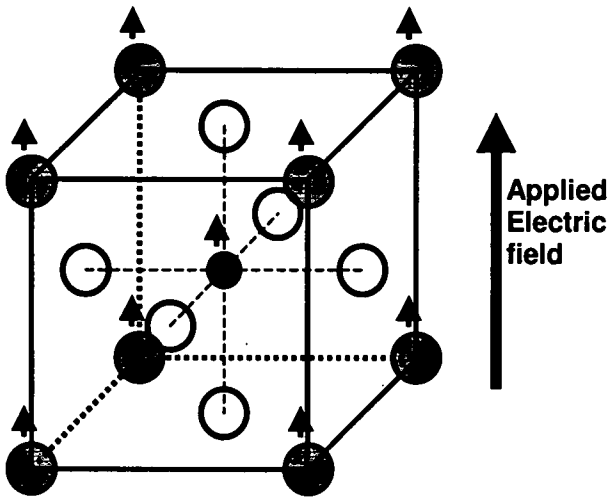


Figure 1-3: Perovskite structure in the presence of an external electric field

At the phase transition points there is always anomalous behavior resulting in extremes for property constants and coefficients. Both the dielectric constant and the loss tangent experience a spike at the phase transition temperatures. Once in the ferroelectric phase both tend to increase with the reduction of temperature until the next phase transition.

In the ferroelectric phase the lattice structure of $BaTiO_3$ has a tetragonal symmetry in which one of the axes is longer than the other two. This distortion forms a dipole moment even in the absence of an external electric field. It is the direction of this dipole that can be switched using an external field and consequently forming the hysteresis loop.

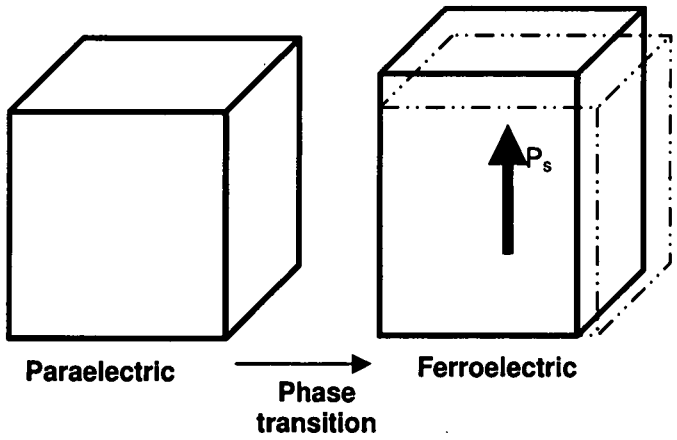


Figure 1-4: Distortion of structure with phase transition

Strontium titanate ($SrTiO_3$) is another member of the perovskite family which behaves very similar to $BaTiO_3$. The Curie temperature of $SrTiO_3$ is below 77K, which is much lower than $BaTiO_3$'s 393K. By doping $BaTiO_3$ with $SrTiO_3$ with the right ratio, it is possible to tailor the Curie temperature of the resulting ferroelectric film. Using a ratio of 60:40 for barium and strontium, barium strontium titanate, $BaSrTiO_3$ (BST), can be formed having a Curie temperature around or below room temperature (293K). The lattice structure remains the same with Ba and Sr atoms replacing each other. BST has a first order transition from the ferroelectric phase to the paraelectric phase. Figure 1-5 shows the variation of the observed polarity of BST with respect to temperature.

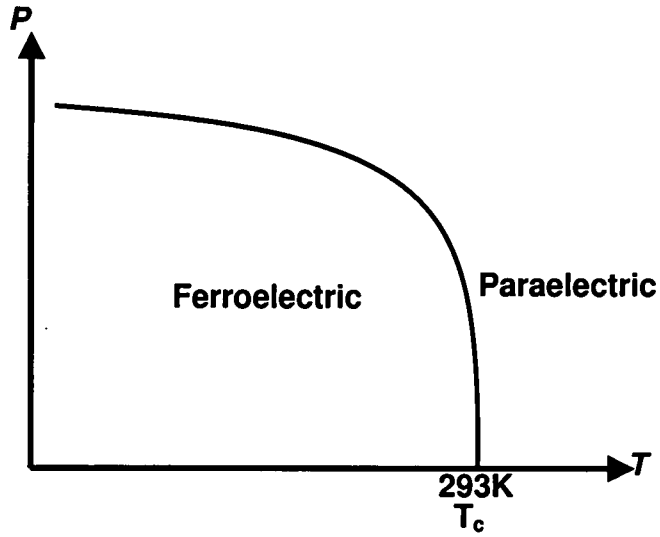


Figure 1-5: Polarization vs. Temperature, Phase transition curve of BST

1.1.3 BST thin-film

Ferroelectric thin-films show all the characteristics of bulk crystals, but all effects are mitigated. None of the extremes in properties at the transition temperatures are observed such as the incredibly high dielectric constant during phase transition. Other physical properties such as elastic, optical, and thermal constants also show anomalous behavior. Single crystal $SrTiO_3$ has been reported to have a dielectric tuning from 20000 to 200 with the application of 10^4V/cm at a temperature of 4.4K, and a tanδ value of less than 0.001, while a SrTiO3 thin-film had a loss tangent of 0.01 and a maximum ε_r of 5000 [5]. Crystals usually have sharp peaks in regions of phase transition while films have much broadened peaks. The differences in behaviors is due to domain wall motion, compositional inhomogeneities, interface layers between electrodes and film, and lattice mismatch induced stress between film and substrate. At 300K a 0.5μm thin-film of BST with 50:50 ratio has ε_r of 1430 and loss tangent of 0.007

when deposited on a single crystal lanthanum aluminate ($LaAlO_3$) substrate [6]. When an external electric field of intensity 2.33V/μm is applied across the film, ε_r and tanδ values are reduced to 960 and 0.001 respectively. Figure 1-6 shows the experimental results obtained for the tuning of an STO sample.

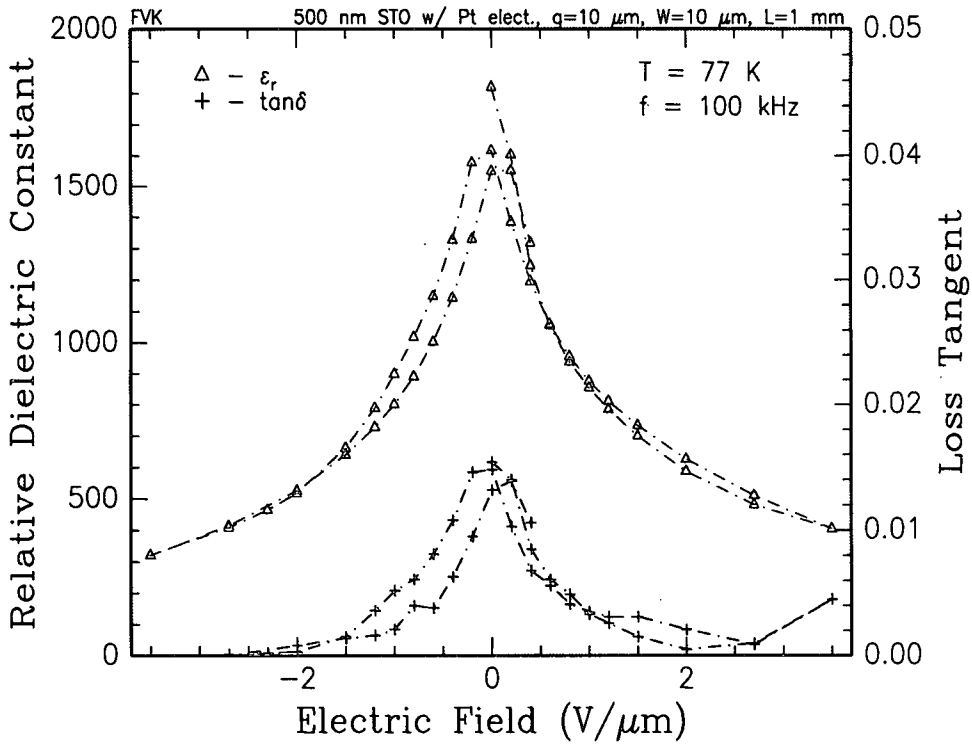


Figure 1-6: Dielectric and loss tangent tuning of $SrTiO_3$ with applied bias

BST thin-films have been shown to have complex dielectric permittivity [7], [8], which is dependent on temperature, bias voltage, and frequency. The loss tangent of the film is approximated as the ratio of the imaginary and real parts of the complex permittivity. For microwave frequencies it is common practice to use the loss tangent and the relative permittivity to characterize a film.

$$\varepsilon = \varepsilon' + j\varepsilon''$$ **Equation 1-3**

$$\tan\delta \approx \frac{\varepsilon''}{\varepsilon'}$$ **Equation 1-4**

$$\varepsilon' = \varepsilon_r \varepsilon_0$$ **Equation 1-5**

The dielectric permittivity tends to decrease with increasing temperature, bias voltage and frequency. Dielectric relaxation is responsible for the reduction in dielectric permittivity as frequency is increased and is caused by the piezoelectric resonances of grains and domains, and sheer waves from domain wall and their vibration. These factors contribute to the dispersion of ε_r and higher tanδ. As the grain size of the film decreases relaxation frequencies increase while ε_r, tanδ, and T_c tend to decrease [9].

The percentage tunability of the dielectric permittivity gives a strong measure of the level of tunablity possible for a frequency agile microwave device. Films have been created which have a dielectric tunability as high as 4 to 1 [10]. Typical formula used for tunability is:

$$\text{Tunability} = \frac{(\varepsilon_{r,0} - \varepsilon_{r,V})}{\varepsilon_{r,0}} \times 100$$ **Equation 1-6**

Where $\varepsilon_{r,0}$ is the relative dielectric permittivity at zero-bias, and $\varepsilon_{r,V}$ is the relative dielectric permittivity with some applies bias *V*. Tunability is a temperature dependent measure. In general, it can be said that "the higher the dielectric constants, the higher the tunability, loss, and temperature dependence of the dielectric permittivity" [11],[12]. A compromise must be made between the level of tunability and the amount of losses that can be tolerated. A figure of merit some times used to gauge film quality is the ratio of tunability to dielectric loss.

Thin-films have the advantage that they are less temperature dependent than their bulk counterparts. As Figure 1-7 shows, the variation in the dielectric constant of thin-film STO and BST with temperature is less and the peaks are boarded at the phase transitions where their crystal counterparts would have had very sharp peals [6]. The advantages in the areas of manufacturing compatibility and the flexibility in design greatly out weigh the greater losses and lower permittivities that thin-films suffer from. Thin-films are able to operate with much lower bias voltages while bulk and single crystal ferroelectrics require much higher bias voltages. The ability to operate at lower bias voltages is very important for wireless and microwave applications, especially in areas of satellite communication and portable electronics. Substrates such as MgO, $LaAlO_3$, and sapphire are commonly used for implementing ferroelectric devices because they provide better lattice matching between the film and the substrate. Lattice mismatch induces stress which results in greater losses. Silicon substrates, which do not provide as good a lattice match, are used because of its compatibility with existing MMIC technology. As the thickness of the films is increased they act more and more like their bulk counterparts, but as dielectric permittivity increases so does the loss tangent.

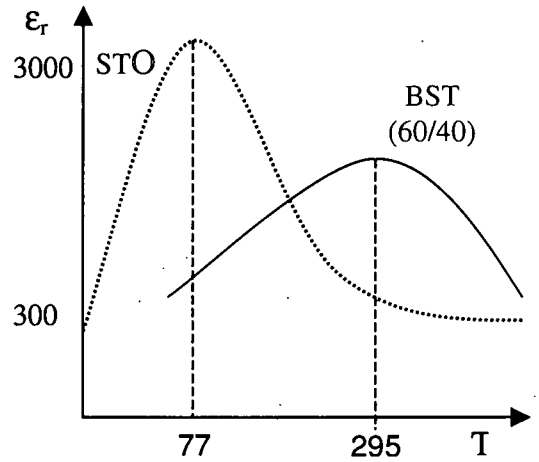


Figure 1-7: Temperature variation of ε_r of thin-film STO and BST

Ferroelectric properties such as the coercive field, spontaneous and remnant polarization, and the general shape of the hysteresis loop are dependent not only on the thickness of the film but also on the presence of charged defects, mechanical stresses, lattice dynamics, and manufacturing procedures [9]. Choices made for manufacturing methods and processing parameters are critical for overall quality of the film and the performance of the device.

The choice of substrate, deposition method, circuit design, and device packaging are important factors concerning cost and performance [10]. For commercial feasibility device processing must be reproducible with quality control, employing high volume deposition technologies for mass production, and be compatible with existing standard IC manufacturing technologies, while adhering to stringent cost requirements. For high frequency applications the desired qualities in a thin-film are low microwave loss, low power consumption, low cost, and ease of integration [13].

Film quality is very important for device performance. A good film has

i) good thickness uniformity
ii) high purity and density
iii) controlled composition and stoichiometry over the entire area
iv) high degree of structural perfection
v) good electrical and dielectric properties
vi) excellent adhesion
vii) good step coverage [14]
viii) good lattice matching with substrate
ix) high quality interface between film and electrodes

Factors effecting film properties are [15],[16]

i)	processing methods	MOCVD, PLD, sol-gel, sputtering
ii)	annealing conditions	temperature, pressure, processing time
iii)	microstructure	grain size and distribution [14]
iv)	interface structure	surface morphology, film-electrode barrier
v)	electrode materials	Pt, Ru, Ag, Au
vi)	choice of substrate	MgO, LaAlO3, sapphire, Si
vii)	dopants	Al, Nb, Mn

BST thin-films have the advantages of

i) high dielectric constants
ii) high degree of continuous tunability
iii) relatively low loss
iv) fast polarization and rapid response
v) high break down voltage and power handling [17], [18]
vi) low voltage operation
vii) negligible dc power consumption [5]
viii) no fatigue or aging problems
ix) low temperature variation of electrical properties
x) low Curie temperature
xi) flexible choice of substrates
xii) compatibility with monolithic processing

[14], [19], [20]

These advantages have lead to the use of BST thin-films in many applications where a high level of tuning is necessary. Phased array antennas are of great importance for low cost earth orbiting communication satellites, automotive radars, and industrial applications because of their swift vibration free tracking ability [5]. Competing technologies include ferrites, GaAs, and MEMS based systems. Ferrites are costly limiting their use to military application, and complex switching circuitry is required to generate the necessary magnetic fields. GaAs MMIC devices are expensive and too lossy for reflect arrays and receiver applications. MEMS based systems can provide a considerable amount of tuning, but suffer from poor switching speeds, and high packaging costs. Phased array antennas based on BST thin-films are compact, low loss, easy to fabricate, and are able to produce phase shifts in excess of 90º/dB[19].

BST thin-films have found their use in the development of tunable lumped element filters. Traditionally, mechanical or electronic tuning is achieved using varactor diodes or switched capacitors [20]. Mechanically tuned filters have high power handling capabilities with low insertion loss, but they suffer from low tuning ability and speed, and the size and mass of the devices pose problems [21]. Devices using varactor diodes have much higher operating speeds, but the losses increase at microwave frequencies [21], [22]. The constraint of reverse biasing limits their power handling and tunability. The use of switched capacitor filter banks is widespread but they are unable to provide continuous tuning ranges and are of considerable physical size. Although MEMS based filters are able to produce substantial tuning with limited loss, they have complex biasing

networks and their stringent packaging requirements result in higher costs [23]. BST based filters have shown a high level of tunability with limited loss. Their compatibility with Si based MMIC technology, and relaxed packaging requirements give them the potential to be a low cost alternative to MEMS devices [24]. A lowpass filter with an insertion loss of 2dB is able to produce 40% tunability (120-170MHz) with 0-9V of bias [20]. A bandpass filter with an insertion of loss of 3dB and tunability of 57% (176-276%) with the application of 0-6V bias has been reported. Improvements in film processing and manufacturing technologies will further improve performance.

BST thin-films are used for RF and microwave application in communications, receiver preselection, transmit filtering, tunable resonators, frequency agile filters, voltage controlled oscillators, local oscillators, remote sensing, phase sifters, delay lines, matching networks, antennas, non-volatile memory, and frequency multipliers [10], [25]-[31]. Advantages of using ferroelectric materials are the substantial miniaturization of microwave components and compatibility with microelectronic circuits. Greater than 50% tunable BST based capacitors using 2-5V dc bias are common [32]-[37], but the nonlinearity responsible for its tunability also causes the generation of intermodulation distortion when used with linear devices [10]. In general BST based devices also suffer from lower Q than other technologies at low GHz frequencies. Above 20 GHz, the Q of BST varactors exceed Q of semiconductor devices and are second only to RF MEMS devices.

At GHz frequencies the internal stresses within the film result in high losses [38]. There are several methods by which microwave loss due to the ferroelectric film can be reduced. Dopants like Al, Nb and Mn are used to reduce the leakage currents. 1% Mn doping has been reported to increase ε_r while reducing tanδ [36], [39]. Rapid thermal annealing (RTA) allows for shorter processing time and simpler processing procedure compared to traditional furnaces [14]. The temperatures used for annealing and the time of exposure are important factors. Another method explored for improving overall film quality is the use of multiple deposition methods [40]. The method involves first the growth of a seed layer by MOCVD and then the deposition of a thicker layer using PLD. Selective etching of the film from areas not contributing to the tuning can reduce the amount of loss due to the film without compromising the level of tunability.

The film is not the only source of loss in a microwave device. The use of lower dielectric substrates can improve loss. The finite quality of conductors also contributes to the problem. Using thicker metal improves these losses, but the metal must be able to fulfill other demands of device manufacturing. The choice of metal must not only have good conduction properties, but it must also form a high quality interface with the film, and be able to survive the high temperatures necessary for the deposition of high quality film. Films deposited at higher temperatures tend to be of greater quality than those deposited at lower temperatures. Films deposited at lower temperatures have smaller grain size, reduced ferroelectric characteristics and lower overall ε_r [25]. Designs involving the deposition of a film on top of a metal layer face problems such as a mismatch

in thermal expansion between the metal and the substrate. Upon cooling residual stresses can cause pealing and the forming of hillocks in the metal layer [20]. This problem is exasperated as the thickness of the metal is increased. Platinum along with an adhesion layer of Ti or TiO_3 is often used as the metal of choice for the electrodes but has been shown to be difficult to etch vertically [41]. Capacitors using Pt electrodes have shown the higher levels of capacitance while leakage current values are relatively lower [42], [43].

1.1.4 Film deposition using PLD

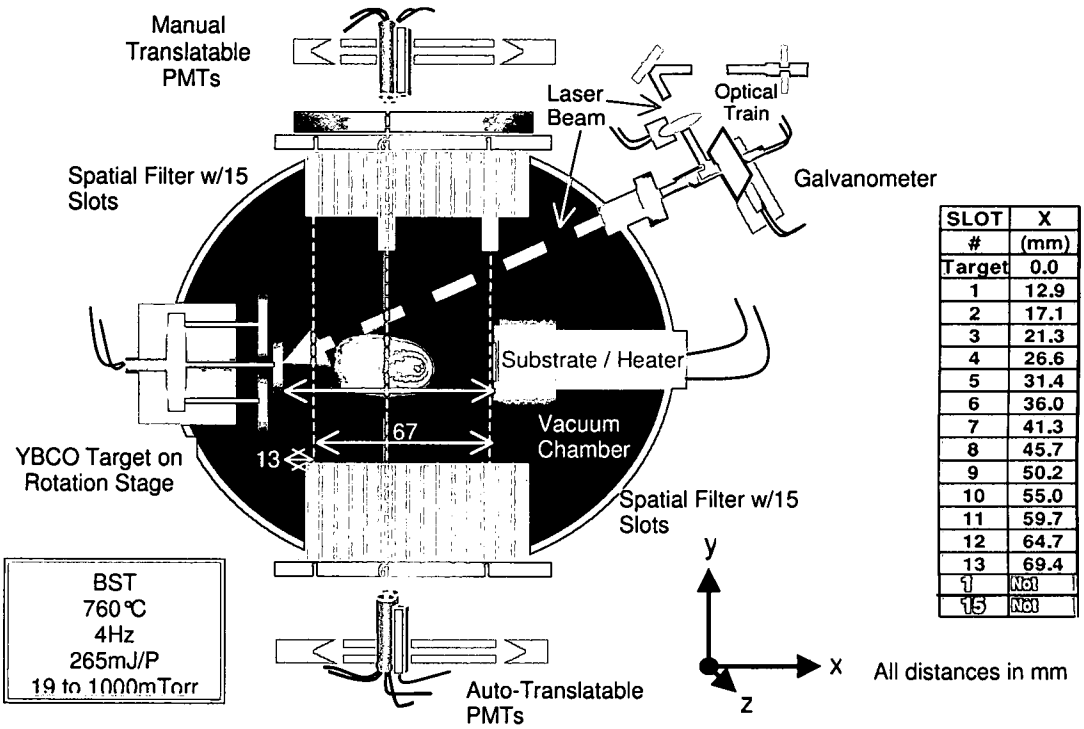
There are several methods available for the deposition of thin-films ranging from MOCVD, PLD, sol-gel processing, and RF magnetron sputtering [19]. Each method has its advantages, but considering that all methods are still in active use for industry and research purposes, they have their individual shortcomings. MOCVD has good step coverage and is used for large scale production, but because of the higher temperatures involved in the processing only certain metals can be used. Sol-Gel processing and sputtering are convenient methods for film deposition but allow for less stoichiometric control. PLD method has the advantage of a high level of composition control, and lower processing temperatures, but can only be used for small scale production.

For this work BST thin-films with a 60:40 ratio is used, which has one of the highest reported levels of tunability. Having a Curie temperature of 290K allows the use of the film in its paraelectric phase. Because there is no hysteresis loop in this phase, the losses are reduced and state of the film is more stable and easier to predict. Using the PLD process it is possible to grow thin-films with

average grain size ranging from 20nm to 140nm with tanδ values less than 0.005 [44]. Larger grain size is better for higher ε_r but also causes greater losses in the film. 45nm average grain size yields a film with a dielectric permittivity of 200 while grain size of 220nm results in an ε_r value of 700 [45].

Pulse laser deposition method utilizes a powerful laser to ablate material from a target and then deposit it onto a substrate via a high energy plume. The composition of the film is ideally the same as the ablated material, giving a high degree of control over the stoichiometry and reproducibility of the process. Factors such as deposition rate, substrate temperature, ambient gases, and target-substrate geometry determine film growth.

The Materials Directorate at the Air Force Research Laboratory, Wright-Patterson Air Force Base, Ohio, have developed a PLD system in which multiple parameters can be precisely controlled. The films produced by the Materials Directorate have high dielectric tunability and low loss-tangent along with a high level of repeatability. Other processing systems are very sensitive to parameter changes causing differences in quality each time the films are processed. The computer controlled PLD system not only allows for accurate parameter change, but also has in-situ real-time process control. Through feedback and real-time adjustments to certain parameters, the uniformity of film deposition can be controlled.



SLOT #	X (mm)
Target	0.0
1	12.9
2	17.1
3	21.3
4	26.6
5	31.4
6	36.0
7	41.3
8	45.7
9	50.2
10	55.0
11	59.7
12	64.7
13	69.4
1	Not
15	Not

Figure 1-8: AFRL process-controlled PLD system

1.2 Frequency Selective Surfaces

1.2.1 Periodic Surface Excitation

Periodic surfaces consist of repeated unit cells in a two- or three-dimensional array. Periodic arrays can be excited in two ways, by an incident electromagnetic plane wave, or by individual generators connected to each element [1]. The latter is the basic structure for phased arrays, and requires the active use of the periodic surface. In the former case, when an electromagnetic plane wave encounters the metallic elements of the periodic surface, currents and voltages are induced on the elements. These currents and voltages re-radiate and the

incident electromagnetic energy is said to be scattered. The combined interaction of scattering from the elements of the periodic surface results in constructive and destructive interference, leading to the formation of its frequency response [47]. The incident wave is partially transmitted through the surface, and partially reflected. The level of transmitted and reflected energy is measured by the ratio of the respective energies to that of the incident energy. The transmission and reflection coefficients are denoted by τ and Γ respectively [1]. Because the level of transmission and reflection changes with frequency, such periodic surfaces are classified as frequency selective surfaces (FSS). Due to the similarity with traditional filters, transmission bands are often referred to as passbands, and reflection bands are called stopbands.

$$\Gamma = \frac{E^r}{E^i}$$ **Equation 1-7**

$$\tau = \frac{E^t}{E^i}$$ **Equation 1-8**

Where E^i is the incident electric field, E^t is the transmitted field in the forward direction, and E^r is the reflected wave in the backward direction. By conservation of energy, it follows:

$$\Gamma^2 + \tau^2 = 1$$ **Equation 1-9**

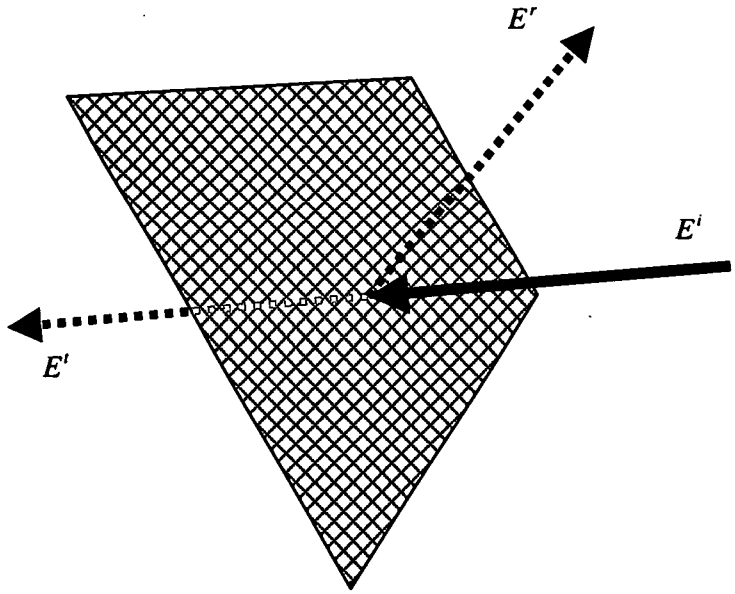


Figure 1-9: FSS with incident plane wave

At resonance, it is theoretically possible to achieve complete transmission and reflection. The shape, location, width, and stability of the resonance is dependent on several design factors. Design parameters such as element shape, lattice geometry, and dielectric loading determine the overall performance of any periodic surface [47]. FSS performance considerations are insertion loss in the transmission band, incident angle and polarization, bandwidth, band spacing ratio, grating lobes, crosspolarization, and edge scattering.

1.2.2 FSS Element

The choice of element is the first and foremost determinant of the performance of an FSS. There are two main classifications of elements, patches and apertures. Patch type elements tend to behave like highpass filters, while aperture based FSS allow lower frequencies to be transmitted and higher frequencies to be

reflected. Variations of the design of the patches and apertures can change the resonance shape and position. Dipoles are the simplest patch type element and when their electrical length is $\lambda/4$ they resonate and produce perfect reflection ($\Gamma=1$) [1]. This can either be understood from the point of view of transmission line theory, with the dipole acting like a quarter wave transformer, or by lumped element analysis of the inductance of the metallic dipole and the capacitance of the gap between dipoles and the resonance of the *LC* combination. Patch and aperture based FSS are, by Babinet's principal, reciprocals of each other, but due to the finite metal thickness and limited conductivity, the complete analysis of one type of FSS does not provide accurate information about its reciprocal [48]. FSS are generally very sensitive to such deviations, and thus require each type of element to be analyzed individually.

Many element shapes exist allowing for variations in performance of the FSS. Figure 1-10 shows a collection of two-dimensional elements. The choice of element determines the stability of resonance, crosspolarization level, bandwidth, and band separation [47]. FSS screens can be either thin screened or thick screened depending on the thickness of the elements. Thick screened FSS are formed from thick bulk metal and require extensive machining. They are important for specific applications requiring very little separation between the transmission and reflection bands, and are used in advanced multi-frequency communication satellite antennas [49]. Thin screen FSS are more prevalent and use printed circuit technology, with the metal thickness being less than 0.001λ. Multiresonant screens require the use of different sized elements on the same

plane. The use of the double circular loop is a prime example in which the second element acts parasitically to improve angular stability of the spectral response [50].

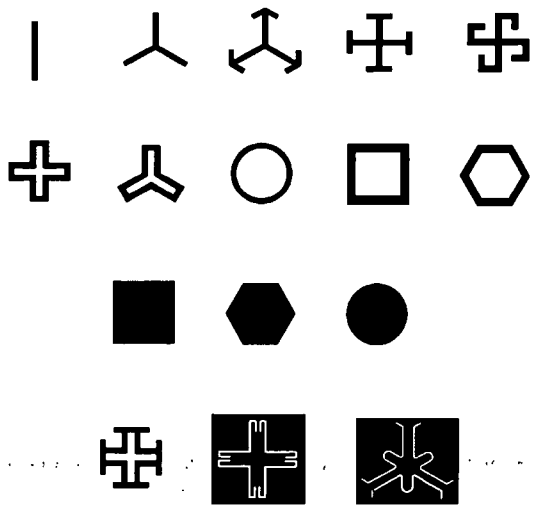


Figure 1-10: FSS elements

1.2.3 Dielectric Loading

The design of an FSS is more complicated than traditional filters. While the response of a normal filter is dependent only on the frequency of the input signal, the response of an FSS (τ and Γ variation with frequency) varies not only with the frequency of the incident wave, but also on the angle of incidence and the polarization of the wave. Due to these characteristics, FSS are used as spatial filters. For certain applications like radomes, the design goal is to stabilize the frequency response and remove the variations caused by incident angle and the polarization. Adding 0.25λ to 0.45λ thick dielectric slabs on the outer most surfaces of an FSS improves the matching conditions and reduces the

dependence of the transmission curve on the angle of incidence and polarization. Dielectric slabs are also used to provide structural support for the FSS and the effects of dielectric loading must be considered during the FSS design [1]. The structure of the FSS is the primary determinant of the resonant frequency, but the addition of dielectrics tends to push the resonance down to lower frequencies. Most practical applications require a resonant curve with a flat top and fast roll off. This is possible by forming a hybrid structure using multiple periodic surfaces cascaded behind each other with dielectric slabs between them. Thin high ε loss dielectrics can be used for an FSS because the incident wave only needs to travel a short distance perpendicular to the substrate [47]. In the case of microstrip and strip line designs, such high loss dielectrics cannot be used because the electromagnetic energy must travel parallel to the substrate rather than perpendicular to it.

1.2.4 Lattice Geometry, Grating Lobes, and Surface Waves

The lattice geometry is another important factor in FSS design. Lattice geometry is concerned with interelement spacing and relative orientation. The element size and the spacing determines the frequency of resonance [48]. Interelement spacing plays a more important role in the prevention of surface waves and grating lobes. Grating lobes occur due to higher order interference, and for spatial application, are observed as secondary beams [47]. Grating lobes can be avoided by having smaller interelement spacing. The rule of thumb is to have an interelement spacing of less than 0.5λ with respect to the highest operating frequency. The condition for the onset of grating lobes is given by:

$$f_{g0} = \frac{nc}{D_x(\sin\eta + 1)}(Hz)$$ **Equation 1-10**

Where D_x is the element spacing, η is the angle of incidence, n is the order of the grating lobe, and c is the speed of light in meters per second (3×10^8 m/s) [1]. Having smaller interelement spacing also improves the stability of the resonance with angle of incidence.

There are two types of surface waves. One type of surface wave (Type I) occurs when a dielectric is placed next to a periodic surface, and grating lobes become trapped within the substrate. As these types of waves are associated with grating lobes, they occur when the wavelength of the incident waves is considerably smaller than the interelement spacing. These types of wave can be found through analysis of infinite or finite arrays. The other type of surface wave (Type II) is unique to finite surfaces and cannot be found through infinite surface analysis [1]. These waves are able to propagate along the surface even in the absence of a stratified dielectric. Type II surface waves propagate strongly below resonance when the element spacing is less than 0.5λ. The presence of Type II surface waves complicates matters by producing interference with Floquet currents.

Surface waves cause an increase in bistatic scattering in an FSS. Specular reflections usually go against the desired design specifications of a good FSS because it causes the RCS of the surface to increase. Surface waves in a phased array cause the terminal impedance to vary considerably from element to element, making it difficult to design a matching network [1].

Type II surface wave are unique to finite arrays but they radiate just like Floquet currents. Floquet currents also radiate in the backward direction, but with the presence of surface wave radiation, the transmissions in the backward direction can increase by as much as 10dB [51]. The presence of surface waves does not alter the main beam significantly although a slight drop in directivity can be observed, primarily due to the increased interference. Surface waves may in some cases be stronger than the Floquet currents, but due to the much lower transmission impedance, they radiate poorly. For the FSS case, resistive loading of individual elements can help reduce the propagation of surface waves. Curved surfaces also tend to hinder Type II surface wave propagation because the wave loses energy as it moves along the curve.

1.2.5 FSS Analysis and Measurement

FSS design has many design variables, and the performance is highly sensitive to changes in any of the parameters. There are too many dimensional degrees of freedom for a purely parametric approach to work. Although the use of computers and the employment of genetic algorithms for optimization of an FSS is necessary, an analytical approach is needed to arrive at the approximate design parameters before computer algorithms can optimize performance. Equivalent circuit modeling is a simple method used to analyze an FSS, where the elements are modeled as inductors and capacitors on transmission lines. Using this technique reflection and transmission coefficients can be found, but due to the quasi-static approximation, it is only accurate up to the resonant frequency of the FSS. The mutual impedance method for analyzing FSS is based

on antenna theory and relies on analyzing the induced current on the elements [1]. The modal (integral equation) method can be employed using the spectral-domain approach, which has been successful in dealing with arbitrary angles of incidence [47].

Accurate transmission response data can be obtained using two horn antennas and focusing lenses in an anechoic chamber. One horn antenna is used to transmit a focused beam of electromagnetic energy onto the FSS, while the other antenna is placed on the opposite side of the FSS and is used to measure the signal that passes through the FSS [52], [53]. Another method involves the insertion of an FSS sample within a waveguide, but the data obtained from this technique is of limited use because there is no control over the angle of incidence, which changes with frequency within a waveguide. This method is only used for spot checking an FSS performance or for validation of simulation software [54].

1.2.6 FSS Applications

The ability of an FSS to manipulate incident electromagnetic waves has found many uses. FSS are employed in hybrid radomes to reduce the radar cross section (RCS) of antennas in communications and military application [55], [56]. Band-pass FSS surfaces allow only the operating frequencies to pass through to the antenna while reflecting out of band frequencies. By limiting the amount of backscattering produced by the antenna shielded by the FSS, the overall RCS of the system is reduced. Such systems are very important for military applications where onboard antennas are exposed to hostile enemy radar. Figure 1-11

illustrates the basic concept of the operation of a hybrid radome in the nose cone of an aircraft.

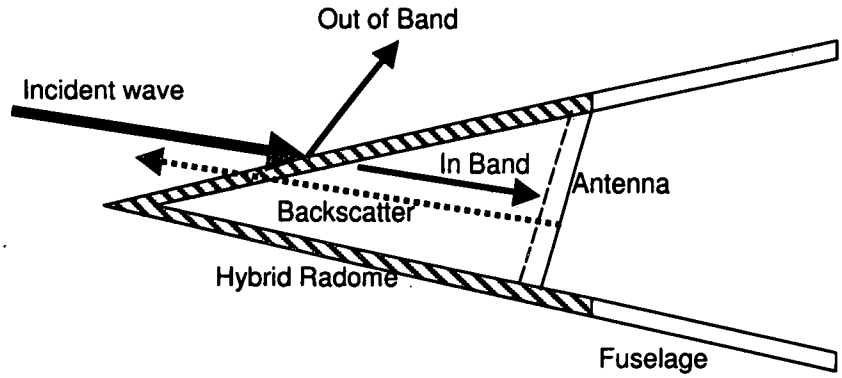


Figure 1-11: Hybrid radome for aircraft nose cone

FSS are used in communication systems to increase channel capacity [57]-[61] as shown in Figure 1-12. By allowing certain frequencies to pass through while reflecting others, multiple schemes have been used where an FSS either acts like a sub-reflector or even as a main reflector for multiple signal sources operating at different frequencies. This method of communication allows for multiple frequencies to use the same main reflector. Dichroic sub-reflectors have been of critical importance for space bound satellites by reducing weight, size, and overall cost (Voyager 77, Cassini).

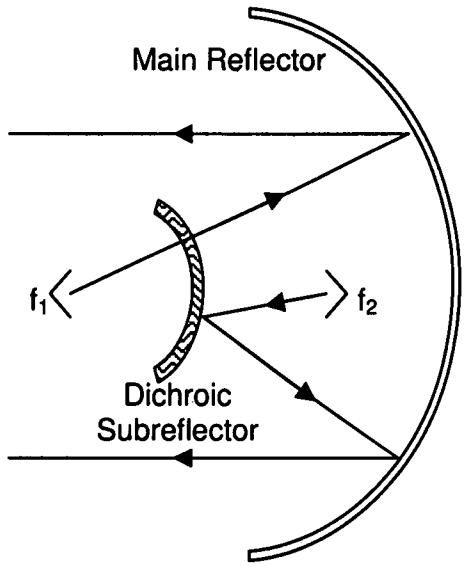


Figure 1-12: FSS used as a Cassegrain subreflector

Typical FSS performance criteria are based on transmission and reflection coefficients. Such FSS are used for radome applications where the magnitude of the transmitted and reflected signal is of primary concern. FSS, when designed with phase considerations, can be used to enhance broad-band antenna arrays [62]. Substrates with a fixed thickness tend to be narrow band structures, limiting the frequency range of operation of antennas printed on them. By imbedding FSS within thick substrates, it is possible to create frequency-dependent substrates or ground planes [50], [63]. Such a technique can help regain the broad-band characteristics of the antenna element. Each successive FSS will act like a magnetic ground plane at resonance, and is placed within the frequency selective volume such that the distance between the antenna and the resonating FSS is quarter wavelength.

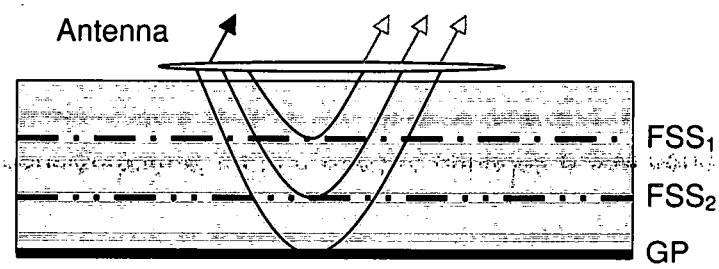


Figure 1-13: Frequency Selective Volume

FSS are also used for spatial filtering [64], side-lobe suppression and beam forming antennas [65]. FSS have been used to enhance microstrip antenna performance [66]. Antenna systems operating at 100-1000GHz have employed FSS for radiometric data collection for use in satellites [67]. FSS have been utilized in solar collectors so that the solar cells operate at their highest efficiency frequency [68], [69]. FSS reflectors in lasers optimize energy consumption during charging [70], [71]. Another application is the use of FSS as a sun shield for space craft antennas; blocking sunlight while RF signals pass through undeterred. Domestic microwave ovens use an FSS to block the 2.45GHz microwaves used to heat food while allowing visible light to pass through so that users can see inside [47]. Microwave power transmission systems have benefited from the use of FSS for suppressing harmonic radiation [72]. Multi-beam dual-frequency imaging antennas for automotive radars have been developed employing lenses made using FSS [73]. FSS made from meander lines can be used to change linearly polarized waves to circularly polarized waves by making appropriate phase shifts to the components of the incident plane wave [1], [51].

1.2.7 Tunable FSS and Meta-materials

FSS are usually designed for a fixed frequency, and one of the main design objectives is to maintain frequency response characteristics over a wide range of incident angles. In some cases it is desirable to have a tunable FSS with a frequency response that can be tuned/switched. Ferrites, diodes, MEMS, and tunable dielectrics can be employed to produce a variable frequency response.

In the past, ferrites substrates have been used for tuning an FSS. The relative permeability (μ_r) of ferrite materials can be tuned by the application of biasing magnetic fields [74], [75]. The complex circuitry needed for applying the bias is costly, and the substrate is lossy. By introducing active elements within an FSS, active grid arrays are formed which have considerably more functionality than its passive counterpart [76]-[81]. Using varactor diodes within a cell structure allows for increased gain and non-linearity. The response of an active grid array can be electronically tuned/switched. The application of non-uniform bias to individual active elements improves beam forming capability. Other active grid array capabilities include oscillation, amplification, and mixing. However, by the introduction of varactor diodes, the active grid suffers form high bias currents, and manufacturing costs increase with the size of the FSS.

MEMS enabled FSS have improved performance by producing high Q tuning elements with very little power consumption. Limiting factors are the speed of operation, and the costly packaging requirements. Q values of greater than 200 have been reported at 30GHz. One method uses MEMS switches for variable loading of FSS elements thus tuning the response of the surface [82]. Another

method uses MEMS to physically change the surface as encountered by a plane wave. UCLA has developed a MEMS based FSS consisting of conducting dipoles connected to torsion beams over a magnetic material [83]. By physically changing the surface the response of the FSS can be tuned by nearly 4.5% while maintaining greater than 20dB rejection in the stop band. The high loss in the silicon limits the level of transmission and tunability. A low-loss dielectric substrate would improve performance.

Another use of FSS is in the formation of analog absorbers, and meta-materials. Traditional absorbers are Salisbury and Juamann absorbers, but they are limited in operating bandwidth [1]. FSS made from lossy materials can be designed to act as circuit analog absorbers which have significantly greater bandwidth. An FSS placed near a conducting ground plane with a dielectric in between shows the properties of meta-materials. Meta-materials are materials showing properties not found in nature, such as negative refractive index [84] - [86]. Through proper design, an FSS can be used to create artificial magnetic conductors and high impedance surfaces [87].

1.3 High Impedance Surface

In many antenna applications, flat conductive sheets of metal are used as either ground planes or as reflectors in order to improve performance and isolation [88]; however, traditional metal sheets as ground planes suffer from two problems when used with antennas. When used as a ground plane, the metal sheet is close to a perfect electrical conductor thus the image currents are in opposite

direction as those in the antenna element. If the antenna is placed too close to the ground plane, it is shorted out, thus limiting how compact an antenna can be. Metal surfaces also support surface waves which are detrimental towards antenna performance. High impedance ground planes are of importance to antenna applications because they show properties of being artificial "magnetic conductors" and they suppress surface waves. Both of these properties enhance antenna performance within a given frequency band.

1.3.1 Surface Waves

The suppression of surface waves is very important for antenna performance. Surface waves are formed of electromagnetic energy traveling at the interface between two dissimilar mediums such as a metal and dielectric boundary [89], [90]. Although these waves are restricted to the interface and decay rapidly into adjacent mediums, they are able to propagate along the interface easily covering a considerable distance. These waves can be radiated into free space when they encounter any interface inhomogeneity such as surface protrusions, edges, and other discontinuities. If an infinite ground plane is used, then surface waves pose little problem because they decay before arriving at any edge from which to radiate; however, in the real world only finite ground planes are used which provide sufficient number of discontinuities from which the surface waves can radiate and couple to incident signals. Multi-path interference occurs and ripples appear in the radiation pattern. Backward radiation also occurs due to surface waves, causing the antenna to couple to areas it was to be shielded from by the ground plane. At radio frequencies, the fields generated by these waves are able

to propagate thousands of wavelengths into the surrounding area. At these frequencies, surface waves are also referred to as surface currents [91].

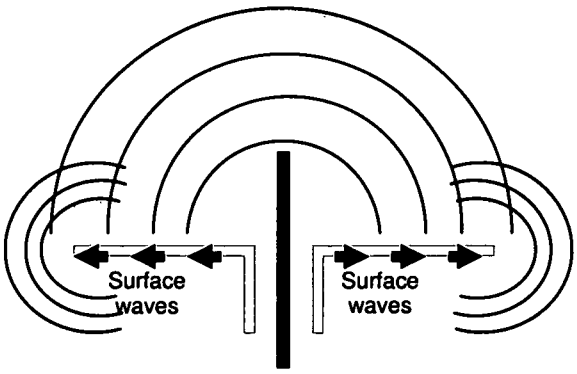


Figure 1-14: Surface wave radiation on normal metal ground plane

1.3.2 Suppressing Surface Waves

Due to the problems caused by surface waves, finding ways of suppressing their propagation can greatly improve performance in the areas of isolation and device size. Textured surfaces have been used to stop the propagation of the waves in limited bands. One method involves the use of a lattice structure of small bumps on the metal ground plane. Depending on the spacing between the bumps, a bandgap is created in which no wave can propagate through the structure [93].

Another popular method is the use of corrugated surfaces which are formed of narrow slots cut into metal. Corrugated surfaces have been extensively studied [89], [90], [94]-[102]. The spacing and thickness of the slots is much less than the operating frequency so that the structure can be treated as a surface rather than individual parallel plates. The depth of the slots actually determines the

frequency at which the bandgap appears. The slots must be $\lambda/4$ so that the short-circuit at the bottom of the structure is transformed into an open circuit at the surface resulting in high surface impedance [89]. Such surfaces have found use in global positioning systems, but due to the $\lambda/4$ limit on thickness, these surfaces are bulky and expensive to manufacture [103].

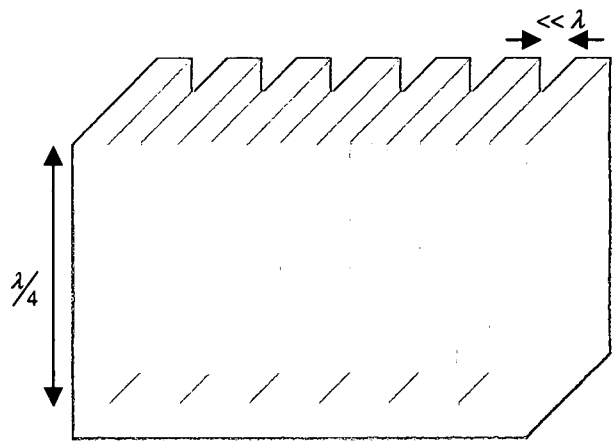


Figure 1-15: Corrugated Surface

1.3.3 High Impedance Ground Plane Properties

Newer forms of surfaces which suppress surface wave have been derived from photonic bandgap (PBG) structures which are also referred to as electromagnetic bandgap (EBG) structures. But typical PBG devices also suffer from the restriction of being at least $\lambda/4$ in size. By extending a corrugated surface in two dimensions it is possible to form lumped element filters extending across a surface which produce a frequency band in which no mode of electromagnetic energy can propagate. As presented in [91] and [92], it is possible to create a

surface with lumped element resonators which produce a large surface impedance at resonance. The structure shown in Figure 1-16 conducts dc currents but restricts ac currents when operating in the bandgap. The high impedance ground plane suppresses surface waves and allows for in-phase reflection.

Figure 1-16: High impedance ground plane, mushroom structure

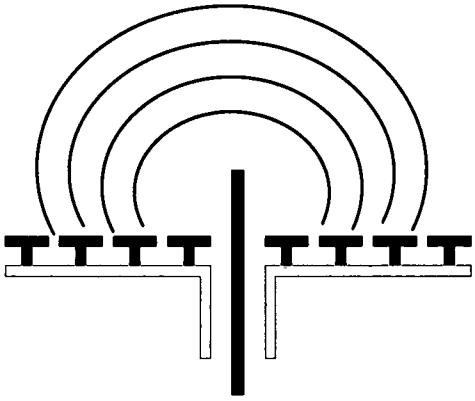


Figure 1-17: No Surface waves when using a high impedance ground plane operating in the bandgap

The mushroom type structures can be formed using traditional printed circuit boards with printed patches on one side and a continuous ground plane on the other, with vias running in between the two metal layers. The vias provide the inductance while the gap between the patches is responsible for the capacitance [91]. When designing for frequencies with much larger wave lengths relative to the dimensions of the texture used, lumped elements can be used to model the surface in order to characterize the surface by a single parameter called the surface impedance Z_s. Z_s is equal to the impedance of the resonant structure

formed by the inductors and capacitors. The values of the inductors and capacitors are found based on their dimensions. The use of lumped parameters to describe electromagnetic structures is valid as long as the wavelength is much longer than the size of the individual feature. As shown in Figure 1-18, the repeated structure can be modeled as a parallel resonant LC circuit. Using basic analysis techniques, it is possible to derive surface impedance as given by (1-11). Spreading these inductors and capacitors on a two dimensional surface creates filter banks cascaded in 2D. The high impedance surface can be considered to be as a kind of two-dimensional photonic crystal which prevents the propagation of surface currents within the bandgap.

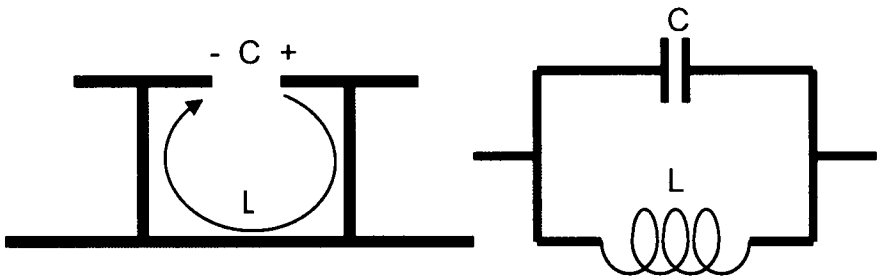


Figure 1-18: Mushroom structure and LC model

$$Z = \frac{j\omega L}{1-\omega^2 LC}$$ **Equation 1-11**

Depending on the frequency, the surface can either be inductive or capacitive. At low frequencies the structure is inductive, while at high frequencies it is capacitive. Inductive surfaces support TM waves, and capacitive surfaces support TE waves. In between these two regions is the resonance frequency

given by (1-12), at which the impedance of the surface is very high. This very high surface impedance is equated to the frequency bandgap.

$$\omega_0 = \frac{1}{\sqrt{LC}}$$ **Equation 1-12**

The effective medium modeling technique may not be able to predict the bandgap, but it is possible to confirm its existence using finite element modeling. In finite element modeling, the device structure is divided by a grid into relatively small finite elements. The electric fields for each element are reduced to a set of Eigen value equations which are solved using matrix operations. Bloch boundary conditions are applied to relate the fields at opposite edges of an element using wave vectors. Through finite element analysis dispersion diagrams of the EBG structures can be produced, predicting the presence of a bandgap [91].

Even though the surface has high impedance within the bandgap, surface currents still exist. These currents flow through the resonant LC structures and produce a phase shift. The phase shift is such that, at resonance, the reflected signal is completely in phase with the incident signal, while away from resonance, the behavior of the surface is similar to a traditional ground plane; i.e. the reflected signal is 180º out of phase with respect to the incident signal. Because the reflected signal is in phase within the bandgap, it reinforces the currents within an antenna element placed on top of the surface. This characteristic has the added advantage that the antenna elements no longer have to be $\lambda/4$ away from the ground plane. When using a high impedance

surface, the antenna elements can be placed close to the ground plane with minimal separation.

1.3.4 Uses of High Impedance Surfaces

High impedance surfaces can be of significant value in the area of portable communication devices which employ a simple monopole antenna. Nearly 50% of the power radiated by a cell phone monopole is absorbed by the user [104]. The signal is directed away from the user by a reflector, the performance of which can be further improved using a high impedance surface. When compared to a traditional reflector, the high impedance reflector has a 1-3 dB gain along the main axis, while reducing backward radiation by 10dB [105]-[108]. The reflector can improve isolation of the antennas and thus the performance. The size of the necessary reflector is also reduced because greater isolation can be achieved with a smaller reflector [103].

High impedance surfaces have another advantage when used as the ground plane for antenna arrays. Due to the suppression of surface waves, multiple antenna elements are able to share the same ground plane with reduced mutual coupling of antenna currents [109], [110]. Four-sector diversity antennas have been developed on a high impedance ground plane for use in vehicular communications [111].

As mentioned earlier, a common method employed for introducing some level of tunability or switchability is through the introduction of varactor diodes into the surface. The varactors are able to change the electromagnetic behavior of the

high impedance metasurface through the application of a bias voltage. Based on the design and geometry, the impedance of the surface and the reflection phase can controlled allowing for an electronically tunable phase gradient and two-dimensional beam steering [112]-[114].

Use of the high impedance ground plane has the advantage of suppressing surface waves and for in-phase reflection within the frequency bandgap. As compared to an antenna using a traditional ground plane, an antenna with a high impedance ground plane has a smoother radiation pattern, less backward radiation power loss, and reduced thickness of the device because the antenna element can be placed adjacent to the ground plane without being short circuited.

Chapter 2 FSS Design

As stated earlier, the main goal for the study is to gain an understanding of the use of BST thin-films for large planar structures such as an FSS or HIGP. The use of BST in such a way has not been well documented, and very little information could be drawn from papers about the application of ferroelectric thin-films in an FSS/HIGP. A rigorous analytical approach that would be recommended for any design cannot be easily applied to this design due to the scarceness of knowledge in this particular area. The work is based on the realization of a simple concept, which just happens to not fall under any single traditional category. Although this does not mean that an analytical approach would not have yielded similar or even better results, but due to the complications that arose during the design process, the attractive nature of a parametric design approach becomes clearer. The design evolved from the basic concept to its final matured shape based on the results of Sonnet simulations. This chapter presents the design evolution in a chronological order, from the initial concept to the final manufactured design, highlighting the findings and the causes for specific deign choices along the way.

This study does not claim to present break through findings, but does attempt to fill (at least partially) a void that exists in the knowledge base of this particular area. The findings of this study may be a stepping stone for future works that will ultimately lead to better performance of microwave devices, or even the creation

of a new class of devices. The structures of FSS, EBG, and HIGP are fundamentally related, but distinctions arise based on their usage and design. The introduction of ferroelectric materials in these structures will impose added demands on design and manufacturing, while opening new criterions for performance such as tunability and device scaling. At the present point, it is not consequential whether the presented device is to be used as an FSS, HIGP, or neither. The structural designs of FSS and HIGP are related and for the purposes of the current study a clear distinction between the two is not necessary.

The ultimate goal is to present a proof of concept that a bandgap can be realized using BST thin-films in a planar structure. The exact levels of pass-bands and rejection bands, and their locations are not as important as their existence. Designs will be compared and analyzed based on their frequency response (in particular S21). In the cases where tunability is not important S21 magnitude response is used for comparison. S11 magnitude is only used in cases where variations are more pronounced in the reflection coefficient. Tunability is measured based on the phase change in degrees per dB of the S21 response or in terms of a frequency shift in the S21 response. Three designs are investigated and one is ultimately chosen for manufacturing and testing purposes. The problems encountered, solutions proposed, and knowledge gained during the design process are presented.

2.1 Design Theory

The basic concept of the device is based on developing a planar structure with a series *LC* resonance. The idea is most closely related to the design of a HIGP as presented by Sievenpiper et al. [91]. In that particular case the HIGP was created with a repeated structure having a parallel *LC* model. A parallel *LC* resonator acts like a band-stop filter, thus the surface will have very high impedance at resonance. The device under investigation uses a series *LC* structure which acts like a band-pass structure, thus the surface impedance is expected to be high except at resonance. The mushroom model of a HIGP is produced again in Figure 2-1, which also shows the repeated structure for the series *LC* design.

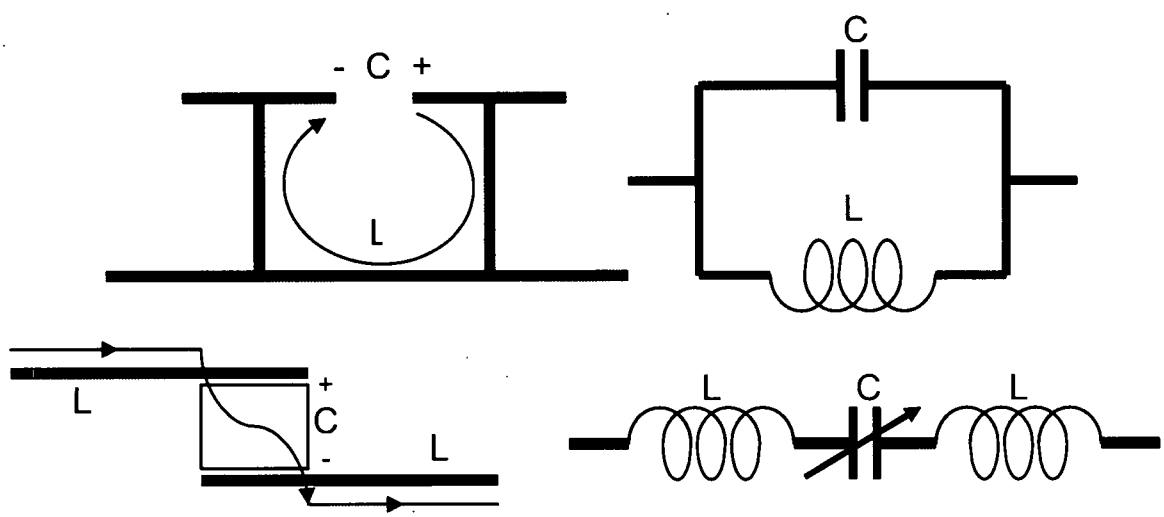


Figure 2-1: Parallel and Series *LC* structures

Due to the inherent ability of ferroelectric materials to change their dielectric constant in the presence of an electric field, the capacitance present within the structure can be changed and the resonance of the design can be tuned. A

simulation setup is created using Sonnet em ® in order to test the degree to which the response of a simple design can be changed by varying the capacitance. The dielectric tunability of the material (BST) is assumed to be 2:1. The tunability of the capacitance is expected to be slightly less than that of the BST itself, and that of the final design may be significantly less.

Sonnet is a finite element simulator which allows for reliable S-parameter simulation for multi-layer designs. The limitation of Sonnet is that is can only simulate transmission lines between defined ports and does not give direct access to the electromagnetic fields. More advanced software suites such and HFSS from Ansoft can provide more detailed simulations of the field effects, but for the purpose of this study the capabilities of Sonnet are sufficient, as will be made clearer later in the work.

2.2 Preliminary Simulations

A layered structure is created in Sonnet for simulating the design of the HIGP. The basic design uses a microstrip to launch the signal, while the series *LC* planar surface acts like the ground plane. The idea is that rather introducing the tuning element (in this case a varactor) in the device formed on top of a ground plane, the tuning element can be introduced within the ground plane itself. The first testing approach uses a microstrip structure formed on a Silicon substrate. The microwave signal is launched along a 50Ω microstrip line. The interaction of the microstrip line with the proposed HIGP will change the performance of the line compared to a traditional ground plane made from a metallic sheet. A

generic model of the traditional microstrip structure and the HIGP structure are shown in Figure 2-2. The S-parameter responses of the line should give insight into the critical design parameters of the FSS/HIGP.

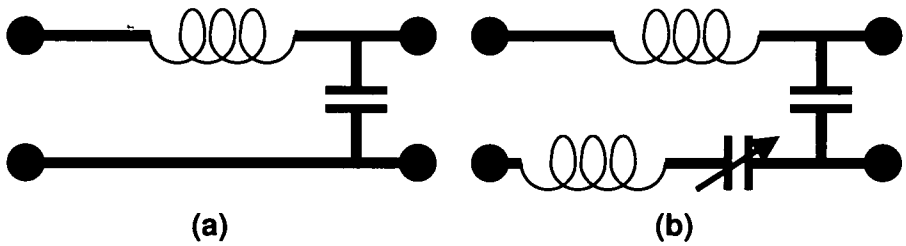


Figure 2-2: Microstrip models (a) traditional ground plane, (b) tunable HIGP

The design uses 508μm silicon substrate with a 0.4μm silicon dioxide insulating layer. On top of the silicon dioxide, 0.5μm gold (metal layer 1) is patterned to form the bottom layer of the HIGP. A 0.3μm BST film is grown on top before pattering a 0.5μm gold layer (metal layer 2) to form the HIGP. 10μm Benzocyclobutene (BCB) polymer is deposited before pattering a 0.5μm gold microstrip on top. The structure dimensions are chosen on the basis of previous design knowledge. Some parameters like the dielectric constant and the thickness of the BST will change throughout the design investigation, while the thickness of the silicon substrate remains constant. The exact values used for the simulations are not as important as the general insight gained from the S-parameters simulation results. Figure 2-3 shows the layer structure that will be used for simulations for the most part. Table 2-1 gives the dielectric layer definitions while Table 2-2 gives some general specifications for the Sonnet geometry.

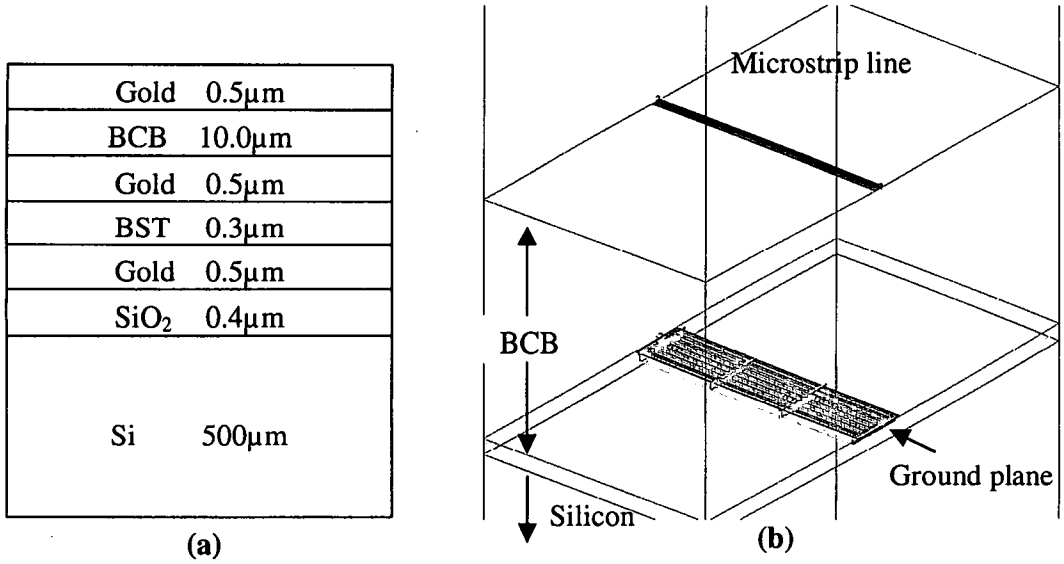


Figure 2-3: Layer layout for simulations (a) layer thickness, (b) 3-D view of microstrip setup

Metal Level	Thickness (microns)	Material Name	Erel	Dielectric Loss Tan	Diel Cond	Mrel	Magnetic Loss Tan
top	500000	Air	1	0	0	1	0
0	10	BCB	2.65	0.001	0	1	0
1	0.3	BST	150	0.02	0	1	0
2	0.4	SiO2	3.8	0.001	0	1	0
3	508	Silicon	11.9	0.01	0.0044	1	0
4	500000	Air	1	0	0	1	0
gnd							

Table 2-1: Dielectric layer definition

Box Size	1600 by 3550 microns (1000519 microns high)
Number of Dielectrics	6 (5 metalization levels)
Metals Used	Gold: Cnd= 4.09e7 T= 0.5 CR= 0 Free Space: Rdc= 376.73 Rrf= 0 Xdc= 0 Ls= 0
Top of box	Free Space
Bottom of box	Free Space
Number of Polygons	18 (all staircase)

Table 2-2: Sonnet geometry settings

For preliminary testing, a 50Ω microstrip line with a 30μm width and 5000μm length is designed for the above specifications. A planar sheet of gold is used as the ground plane for the microstrip line. The final step was to vary the inductive properties of the gold to mimic the effective inductance theoretically produced by the combination of inductance and capacitance in the final design. Sonnet is able to model the resistive and inductive properties of a metal in its analysis. Using the formula given in (2-1) the resistive part *R* of the impedance can be found, where σ is the conductivity of the metal and *t* is the metal thickness. Using the settings shown earlier, the resistance comes out to be 0.02445Ω. For simulation purposes it is assumed that the fixed inductance *L* of the metal is 0.05nH.

$$Z = R + jX_L = \frac{1}{\sigma(1-j)t}$$ **Equation 2-1**

The total impedance for a general metal is given by (2-2). *C* is the variable capacitance due to the ferroelectric material at the overlapping regions. It is proposed that the capacitance can be varied between 2pF to 3pF.

$$X_L = \omega L - \frac{1}{\omega C}$$ **Equation 2-2**

The effect of the fixed inductance L and the variable capacitance C can be consolidated into a single frequency dependent variable L_{eff} as given by (2-3). At resonance the reactive effects of the inductance and the capacitance will cancel each other and the resulting effective inductance will be zero. Above resonance the inductive effect is stronger resulting in a positive value of L_{eff}, while below resonance the capacitive effect can be represented by a negative value of L_{eff}. Using the general metal model available in Sonnet, the inductance value of a metal can be adjusted; however, Sonnet only allows for positive values of inductance, thus only simulations above resonance are valid.

$$L_{eff} = L - \frac{1}{\omega^2 C}$$ **Equation 2-3**

The resonance frequency can be found based on the values of L and C as given by (3-4). With the limitations on the variation of capacitance between 2pF and 3pF, the two resonant frequencies are 15.9GHz and 13GHz respectively.

$$f = \frac{1}{2\pi\sqrt{LC}}$$ **Equation 2-4**

As L_{eff} is a frequency dependent variable, with each frequency point the settings for the metal are changed in Sonnet to reflect the new value of effective inductance. Sonnet simulation results for 2pF are shown in Table 2-3 and those for 3pF are shown in Table 2-4. Figure 2-4 displays the S21 magnitude (dB) and Figure 2-5 shows the S21 phase (degrees) comparisons between the 2pF and

3pF simulation results. The results show that by changing the capacitance value in the ground plane, the response of the design can be tuned.

Frequency (GHz)	L_{eff}(pH)	DB[S11]	DB[S21]	ANG[S21]
16.0	0.5267	-32.0487	-0.80744	216.7
17.0	6.1759	-28.6936	-0.68046	190.4
18.0	10.91	-38.2239	-0.61952	169.59
19.0	14.916	-25.0660	-0.59818	151.55
20.0	18.337	-19.9072	-0.60265	135.28

Table 2-3: Inductive simulation with 2pF

Frequency (GHz)	Leff(pH)	DB[S11]	DB[S21]	ANG[S21]
13.0	0.03886	-28.0677	-0.82922	244.3
14.0	6.9212	-21.3031	-0.69624	217.9
15.0	12.473	-23.0801	-0.62658	197.6
16.0	17.017	-32.1186	-0.57906	179.99
17.0	20.783	-27.9339	-0.56463	163.83
18.0	23.94	-20.6370	-0.57929	148.74
19.0	26.61	-17.2703	-0.60813	134.53
20.0	28.891	-15.5026	-0.63428	121.01

Table 2-4: Inductive simulation with 3pF

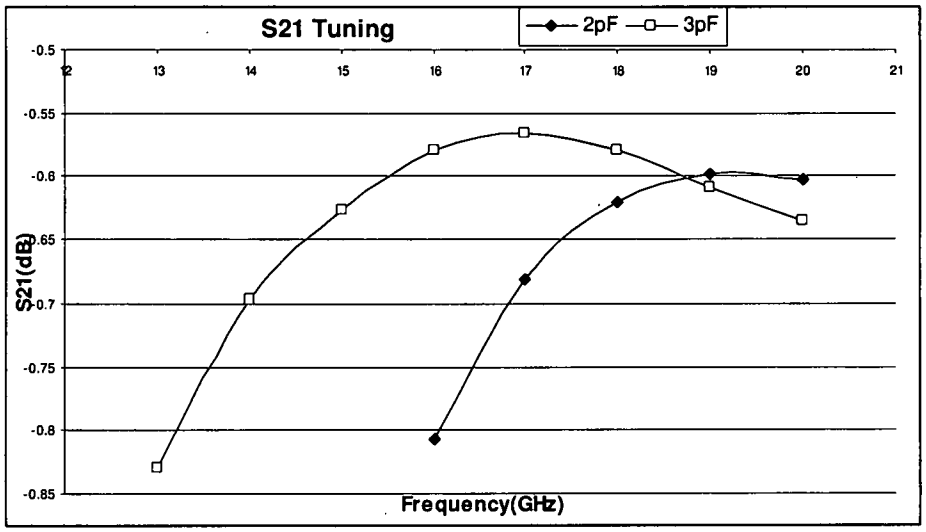


Figure 2-4: Inductive simulation S21 magnitude comparison: 2pF and 3pF

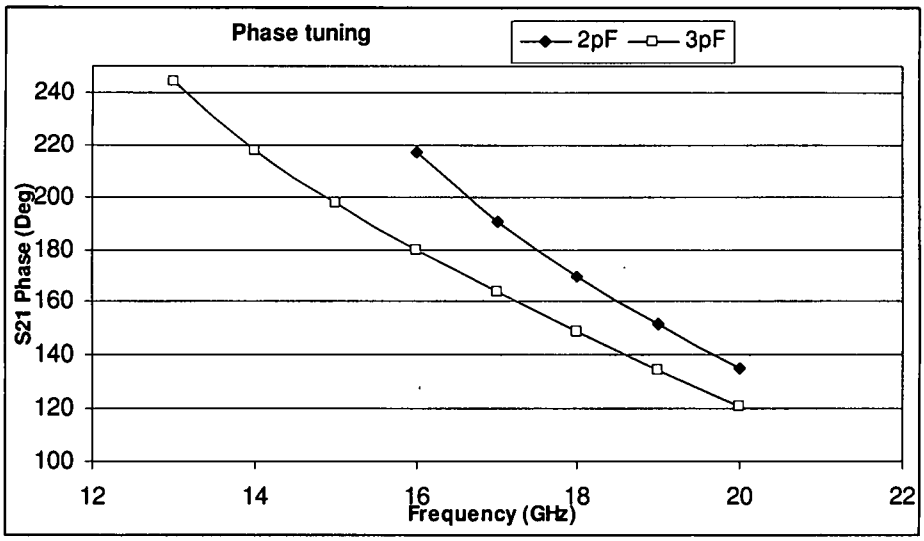


Figure 2-5: Inductive simulation S21 phase comparison: 2pF and 3pF

2.3 Design 1

To create the tunable high impedance surface, a design must fulfill two main requirements, i) lumped element inductors in the form of metallic strips and overlapping regions between metallic layers for capacitors must exist, ii) dc bias paths must be available to tune the dielectric film in the overlapping areas. The first design proposed fulfilling these requirements consists of a plane horizontal microstrip line for the first layer acting as a signal source, and then a patterned gold layer forming the top part of the ground plane. The patterning design for the second layer of metal determines the resonance of the structure. The third layer of metal forms the bottom of the ground plane and is there primarily for the formation of the varactors. A lumped element model of the ground plane is shown in Figure 2-6. The dc pathways are shown which are necessary for the device to be tunable

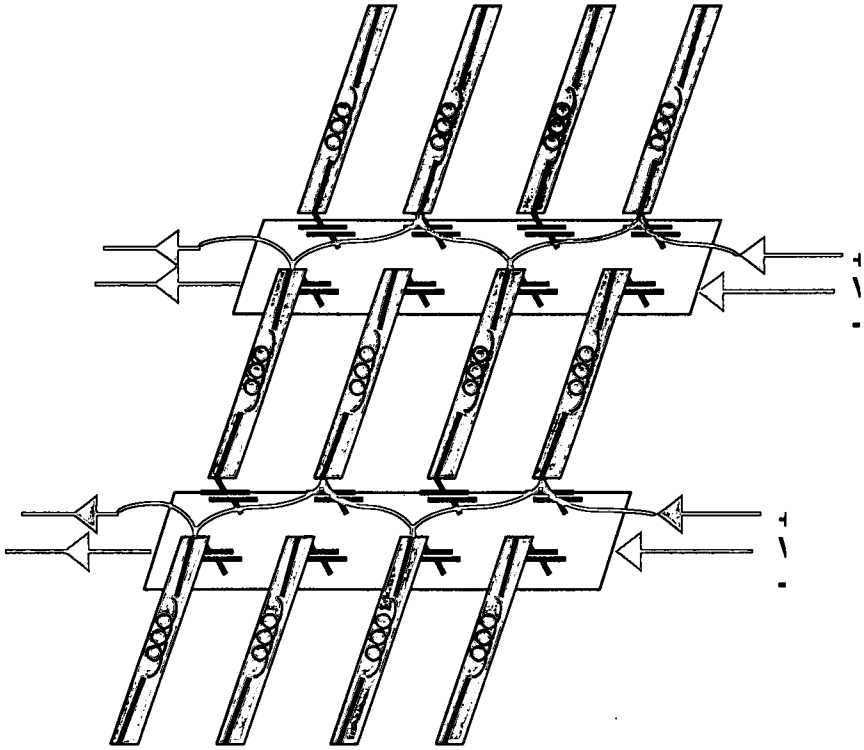
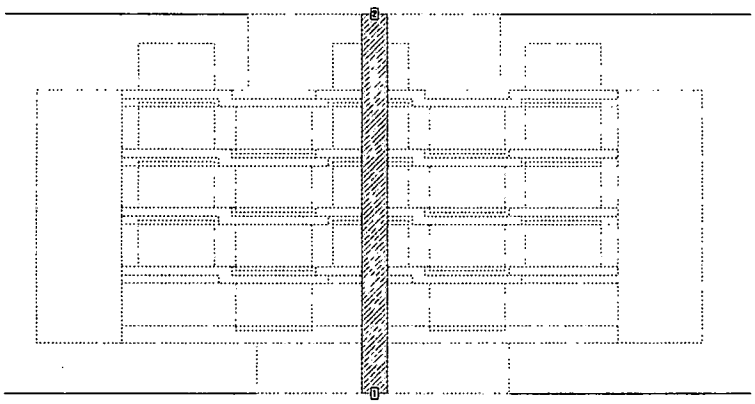


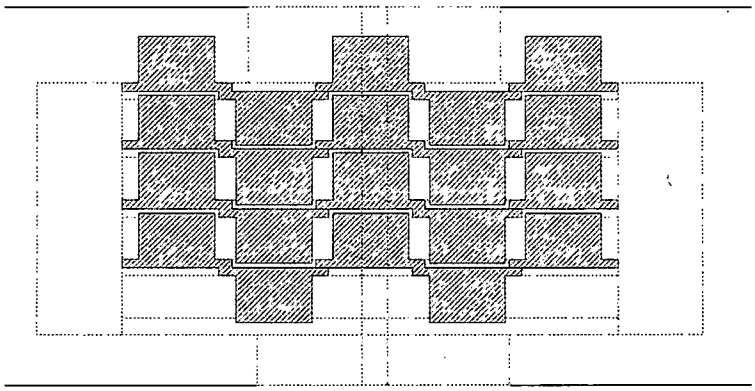
Figure 2-6: Design 1, lumped element model

The BST layer has a relative dielectric constant of 150 which can be altered down by 30 to 40% by applying an electric field to it. For simulation purposes it is assumed that the relative dielectric constant can be reduced down to 100. Brick material is used to simulate the localized changes in the dielectric constant. The original proposed design had dimensions of 2000 by 5000μm, but due to the excessive memory requirements for simulating such a large circuit, the size had to be significantly reduced. The simulated circuit with the layout shown in Figure 2-7 has dimensions of 790 by 450μm. The S21 magnitude(dB) response under biased and unbiased conditions, and the difference in S21 phase angle(degrees) obtained from the two simulations are shown in Figure 2-8. Based on the design

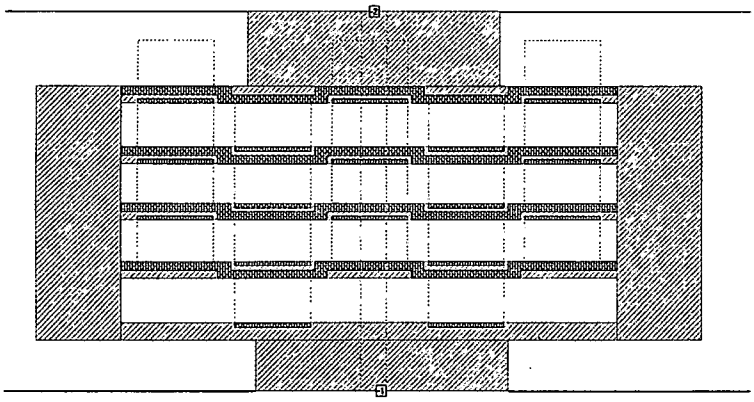
dimensions the expected resonances were to be in the region of 16GHz. As calculation were made from crude approximation the resonance shown by the simulation results is not exactly where it was expected but it is in the region. Some rejection is observed accompanied by phase change between the two simulations. The figure also displays the phase differences produced due to the application of bias to the ferroelectric film.



Top Layer with microstrip line



First layer of patterned metal forming top of ground plane



Second layer of metal forming bottom of ground plane. The overlapping regions are shown

Figure 2-7: Design 1, Sonnet Layer layout

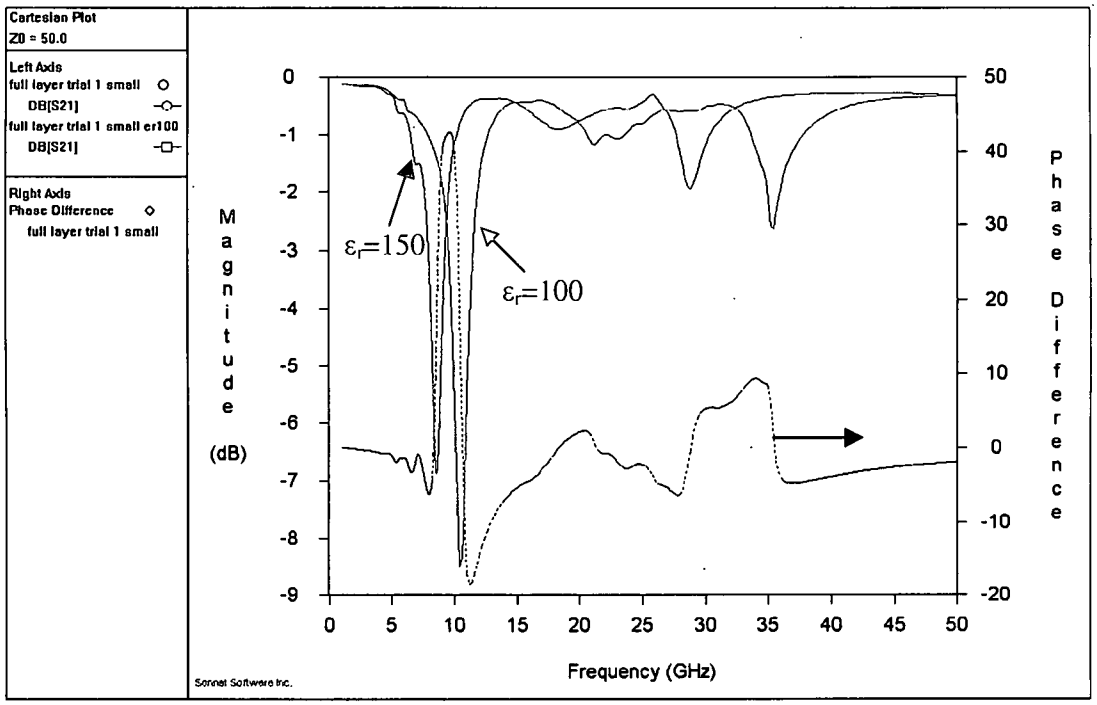


Figure 2-8: Design 1 simulation results

The series resonances are designed to exist parallel to the microstrip line, forming a band-pass response, but due to the periodicity of the design, parallel resonances are setup within the ground plane which will open up rejection bands in the frequency response. The existence of multiple pathways for dc further

complicates matters because depending on the path the resonance changes. Although a band-pass response was hoped for, due to multiple pathways, the signal is able to pass over a wide frequency range. The band stop regions are due to the inherent parallel resonances that exist within the device. Although these preliminary simulation results do not conform to initial theoretical expectations, the response of the device shows interesting features which require further study.

As can be understood from the above discussion, the problem becomes a lot more complicated than the simple concept the idea originated from. The addition of the bias requirements introduces complicated resonances that are very difficult to model, and predict. As will be shown later, the problem is further complicated by additional variables that initially had been assumed to be constant such as the individual strip inductance. The periodic nature of the design makes it difficult understand the electrical behavior of the circuit. Design 1 was simulated as a very small test case, and it is predicted that complication will only increase as the ground plane increases in area.

2.4 Design 2: Meander Lines

2.4.1 Meander Layout

Due to the complexity of Design 1 and the limited ability with which parameters could be varied, a new design is proposed which fulfills the requirements of having lumped elements and bias lines while at the same time allowing for larger ground plane sizes to be simulated, and providing greater freedom in parameter

variation. The meander line design consists of alternating meander lines on both the top and bottom layers of the ground plane. The metal of the meanders provides the inductance while the overlapping of the lines provides the capacitance. The layout model for the meander design is shown in Figure 2-9.

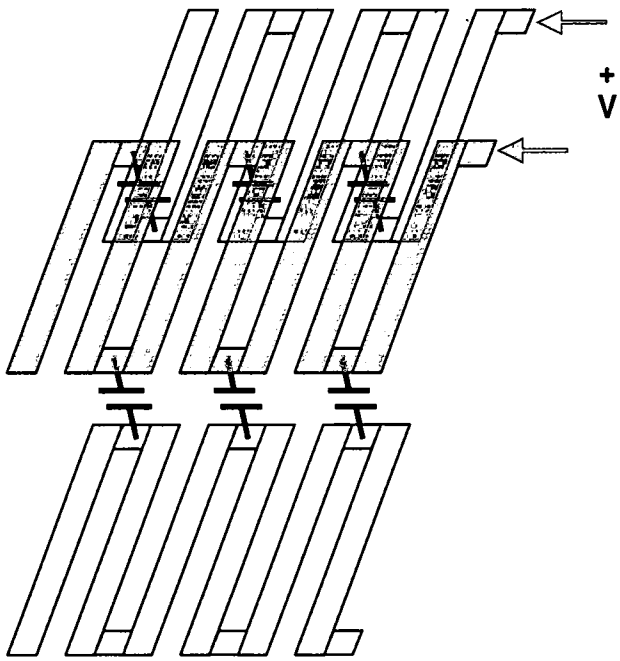


Figure 2-9: Design 2, Meander model

Between the alternating sets of meandering lines are sets of floating lines which should help to reduce the losses. The addition of the floating lines increases memory consumption, but at the current stage of simulations the added memory demands can be tolerated. Figure 2-10 shows the patterning of the two planes of metal. The microstrip line is still at the very top layer. Only one section of the layout is shown. For the full design, the structure is repeated continuously to cover the entire ground plane.

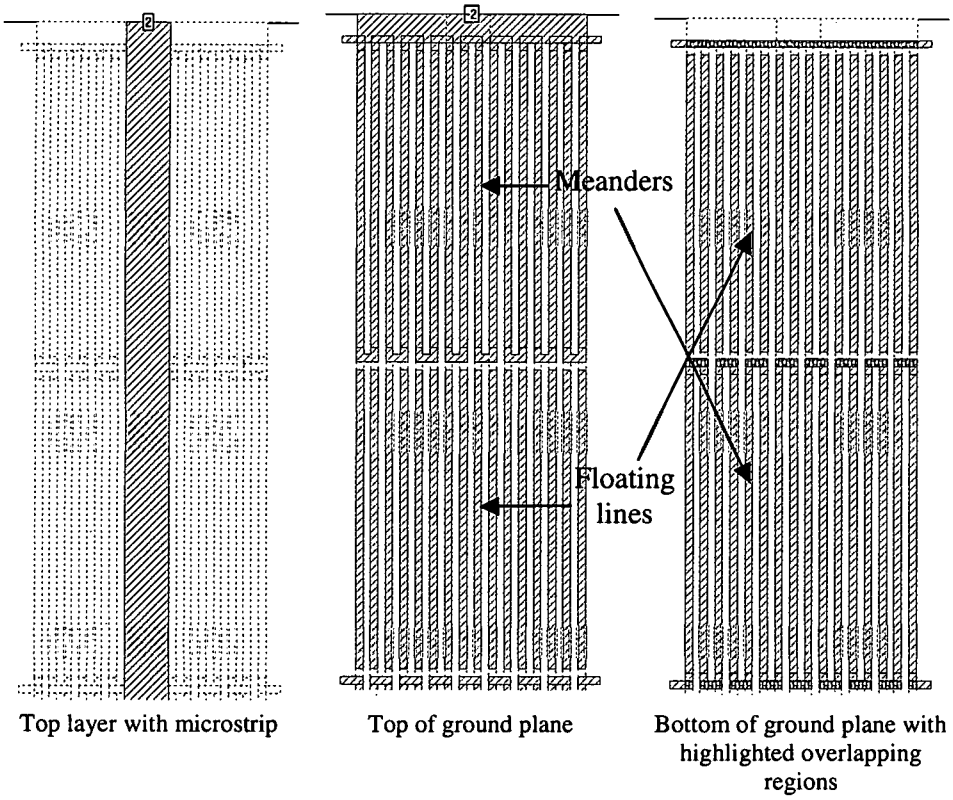


Figure 2-10: Design 2, Sonnet layer layout

The metal is modeled in Sonnet em tools using a thin metal model which requires the current ratio for the top and the bottom of the metal electrodes, which can only be accurately determined through physical experimentation. For simulation purposes a default value of 0 allows Sonnet to form its own estimation of the losses.

The smallest dimension used within a design places a limitation on the largest cell division used by Sonnet for finite element analysis. The greater the number of cells used to analyze a design results in greater accuracy however at the cost of excessive memory usage. In most cases presented in this work, the smallest dimension is 5μm, which is used as the cell size. With the 5μm cell size

restriction, all dimensions are integer multiples of 5μm. The gap *g* between the meander lines, the width of the meander lines, and the floating lines is 5μm, while the length *l* of the meander lines is 200μm. The overlap area for the capacitors is 75μm^2. The dimensions for the meanders are displayed in Figure 2-11; all dimensions are in micrometers.

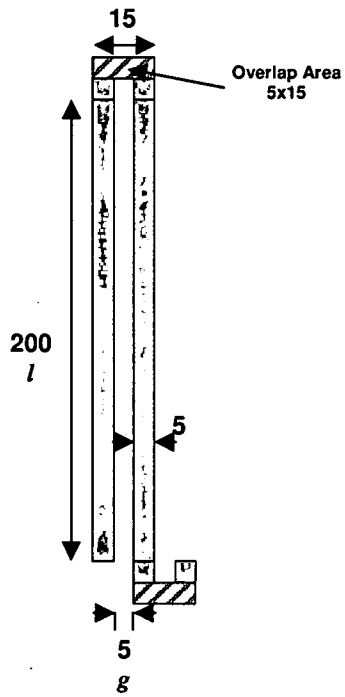


Figure 2-11: Design 2, basic meander dimensions

In the following case three cells of meander lines are used which gives the ground plane a length of 680μm and a width of 175μm. Each cell contains 8 meander lines (2 parallel lines forming one meander). The cells at the ends are capacitively coupled to the device ports. Three simulations were conducted for this particular device design. One simulation was with the dielectric constant of the BST set to 150. The second simulation was done with the dielectric constant

of the BST layer set to 100. The third simulation was conducted using brick material of 100 embedded in a layer of 150 to represent localized change in the dielectric constant of the BST where the metals of the two layers overlapped. The simulation results for a full layer of BST or the use of a brick layer of BST are very similar, thus an exclusive simulation using brick material is not necessary. Brick material requires extra memory for simulation and provides a more realistic model, but only limited knowledge is gained through its use. Figure 2-12 displays the results for the simulations for the design. The band stop regions are attributed to parallel *LC* resonances. Some tunability is observed for the narrow bands. The reduction of the dielectric constant causes the frequency response to be shifted to higher frequency. The phase difference due to the change in the dielectric constant of the BST layer is also shown. The existence of pass bands and stop bands are the expected responses. Had a traditional flat metal sheet been used for the ground plane, all frequencies would be passed through the transmission line structure, without producing the frequency response shown in Figure 2-12. At high frequencies the device response resembles that of a traditional ground plane with added losses. At lower frequencies the resonances caused by the circuit elements create the features seen in the response. DC current is unable to flow through the structure because of its capacitive nature. A parallel resonance sets up a rejection band near 17GHz, breaking the general high pass behavior.

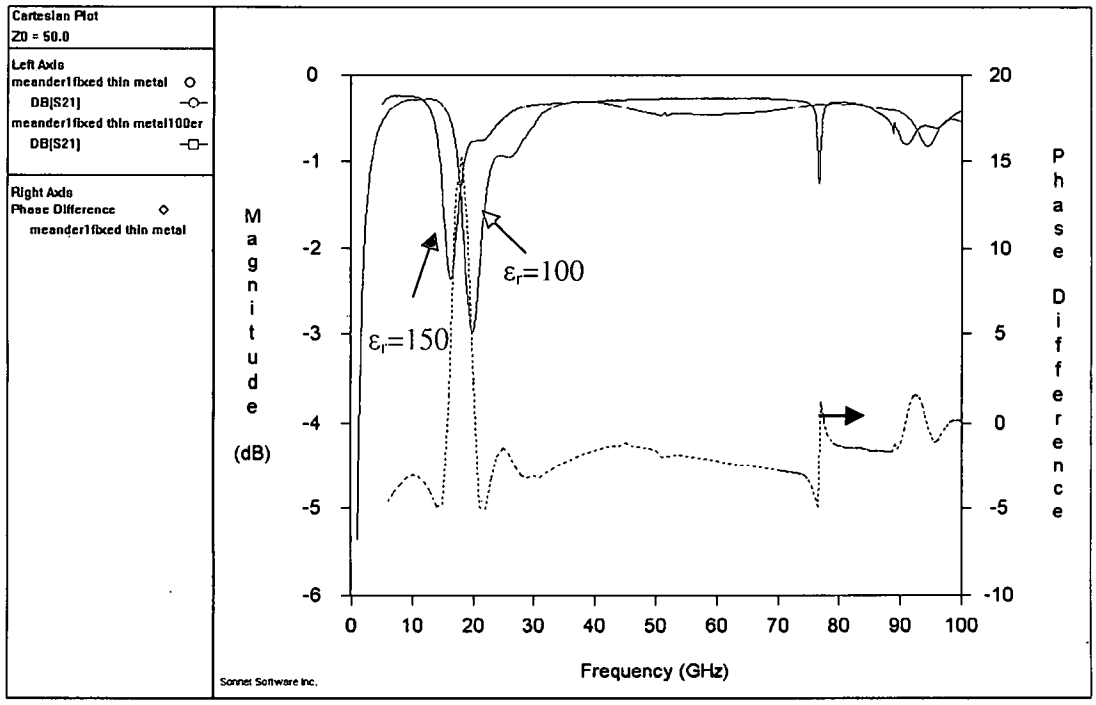


Figure 2-12: Design 2, Simulation results for meander lines

2.4.2 Unit Cell Modeling

A unit cell is needed to model the behavior of the larger system. Having a unit cell makes understanding the performance and the problem of optimization much simpler. A smaller circuit representing the larger systems allows for quicker simulations and convenient parameter manipulation. Figure 2-13 illustrates the layout of a possible unit cell. The cell shown is the simplest possible cell but it may or may not be complex enough to represent the multiple interactions that take place in the larger system. Based on the performance of the unit cell, attempts are made at creating a lumped element model to represent the system. It is important to note that the microstrip line must still exist. The microstrip acts as a relative ground plane to the unit cell whereas in the actual system

collections of unit cells act like the ground plane to the microstrip line. It is currently not clear what will be the effect of the relative distance between the microstrip and a particular unit cell's performance in the larger system. A unit cell directly underneath the microstrip behaves differently than one displaced further away in the HIGP.

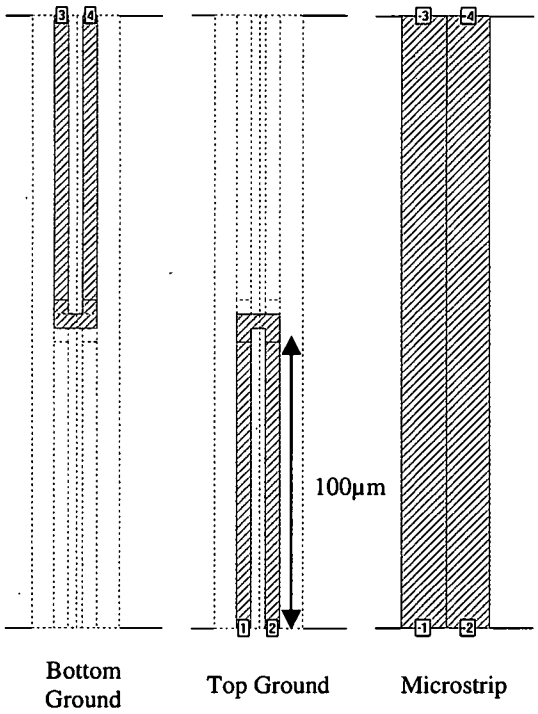


Figure 2-13: Design 2, unit cell layout

Figure 2-14 displays the S-parameters obtained through simulations. The behavior does not directly resemble the results shown in Figure 2-12. Assuming that this particular unit cell represents the layout shown in Figure 2-10, then the discrepancy may be attributed to the interactions between cells in the larger system.

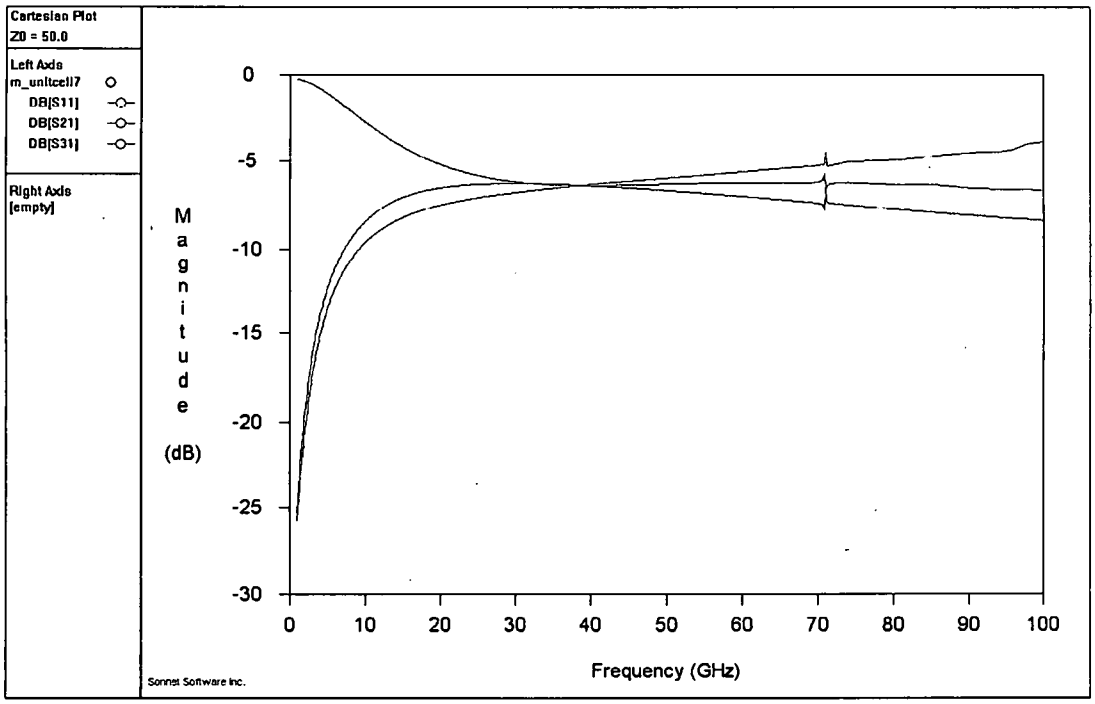


Figure 2-14: Design 2, unit cell layout simulation

Figure 2-15 shows a possible lumped element model for the unit cell shown in Figure 2-13. Estimates for the inductance and capacitance are made first using Sonnet simulations of individual components of the unit cell (inductive strip, parallel plate capacitor), and then modified to best fit the results shown in Figure 2-14 using optimization routines available in Sonnet. It is found that the inductance due to one 100μm inductive strip is approximately 0.066nH. The capacitance of the parallel plate capacitor is found to be around 0.322pF. It must be noted that the inductance value found through matching of layout and model results is approximately half as predicted through the rule of thumb (1nH <=> 1mm) because of the presence of the ground plane in the form of the microstrip on top of the cell. The close proximity of the microstrip to the unit cell makes it

difficult to apply rules of thumb to achieve even approximate results. Initial matching was difficult due to additional parasitics that had not been accounted for. S31 parameter could be easily matched, while adjusting the parasitic parallel capacitance helped match the S11 curve. Figure 2-17 shows the simulation results for the unit cell layout and the lumped element model. In general the resistive components in the model have been ignored. The small resistors shown in the model are meant for port isolation only. At this point there are elements of the circuit that are not clear and thus cannot be predicted with confidence.

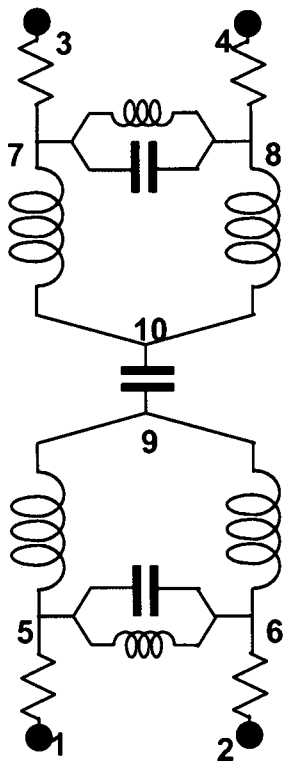


Figure 2-15: Design 2, Unit cell lumped element model

```
RES 1 5  R=1.0
RES 2 6  R=1.0
RES 3 7  R=1.0
RES 4 8  R=1.0
IND 5 9  L=0.066
IND 6 9  L=0.066
IND 7 10  L=0.066
IND 8 10  L=0.066
CAP 9 10  C=0.322
IND 5 6  L=0.04
IND 7 8  L=0.04
CAP 5 6  C=0.05
CAP 7 8  C=0.05
DEF4P 1 2 3 4 Net Main Network
```

Figure 2-16: Design 2, Unit cell lumped element net list

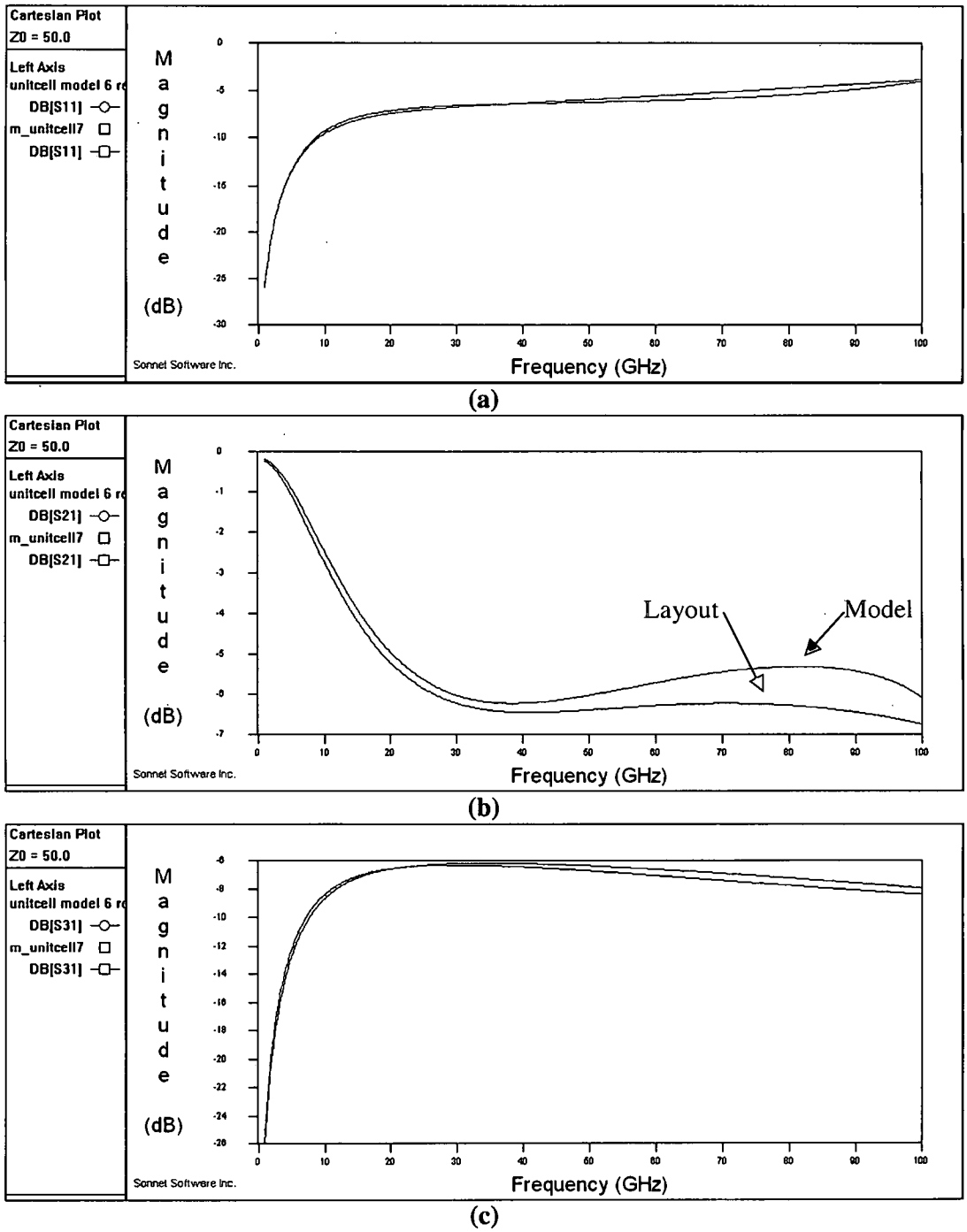


Figure 2-17: Design 2, Unit cell layout and model comparison, (*a*) S11, (*b*) S21, (*c*) S31

Although a decent match between the unit cell layout and the lumped element model was achieved, it still does not solve the problem that the unit cell itself is

having highly complex interactions within the ground plane. Attempts were made to create a larger unit cell which would be a better representation of the system; however, the complexity of the unit cell increased dramatically and a lumped element model could not be easily found for the larger unit cell. The complexity arises from the variations of observed inductance and capacitance. The inductance and capacitance values are not only a function of their dimension, but are also affected by their relative distance from the microstrip line. Without a better understanding of the system, a unit cell at this point does not appear to be feasible. With the absence of a simple unit cell and its model, complete systems must be simulated which not only take longer time to simulate, but the results generated are difficult to interpret.

2.4.3 Variations in Observed Inductance and Capacitance

It is already understood that the proximity of the inductive strips to the microstrip line changes its properties. The microstrip acts as a relative ground plane to the two dimensional structure made from parallel strips and varactors. Using Sonnet simulations, a measure of the variation in observed inductance and capacitance can be determined. Simulations are conducted with isolated strips and capacitors, and their distance from the microstrip is varied. Using Y parameter values from simulated data, Sonnet uses (2-4) to determine the series inductance (in nH) that exists between ports, assuming a PI-model. The capacitance is also found in a similar manner using (2-5). Although such calculations may not be fully reliable, they do provide a picture of the change associated with the proximity of the strips to the microstrip line.

$$L = \frac{-1\times10^{9}\, imag\left(\frac{1}{[Y_{21}]}\right)}{2\pi f}$$

Equation 2-4

$$C = \frac{1\times10^{12}}{2\pi f \times imag\left(\frac{1}{[Y_{21}]}\right)}$$

Equation 2-5

Figure 2-18 shows how the inductance increases as the distance between the inductive strip and the microstrip is increased. The greater distance reduces the capacitance between the two strips and also affects the inductance of the strips. As only isolated strips were experimented with, the effects of mutual inductance are not observed. The separation distances chosen for this investigation are those present in a design having a gap width of 10μm. The distance is measured from the center of the microstrip line to the center of the inductive strip. The minimum distance is when the inductive strip is directly underneath the microstrip, and the maximum distance simulated is 105μm. There probably exists some analytic technique through which this behavior could be explained. Once a mathematical frame work for inductances and their mutual coupling to the microstrip and to each other is available, a unit cell can be created.

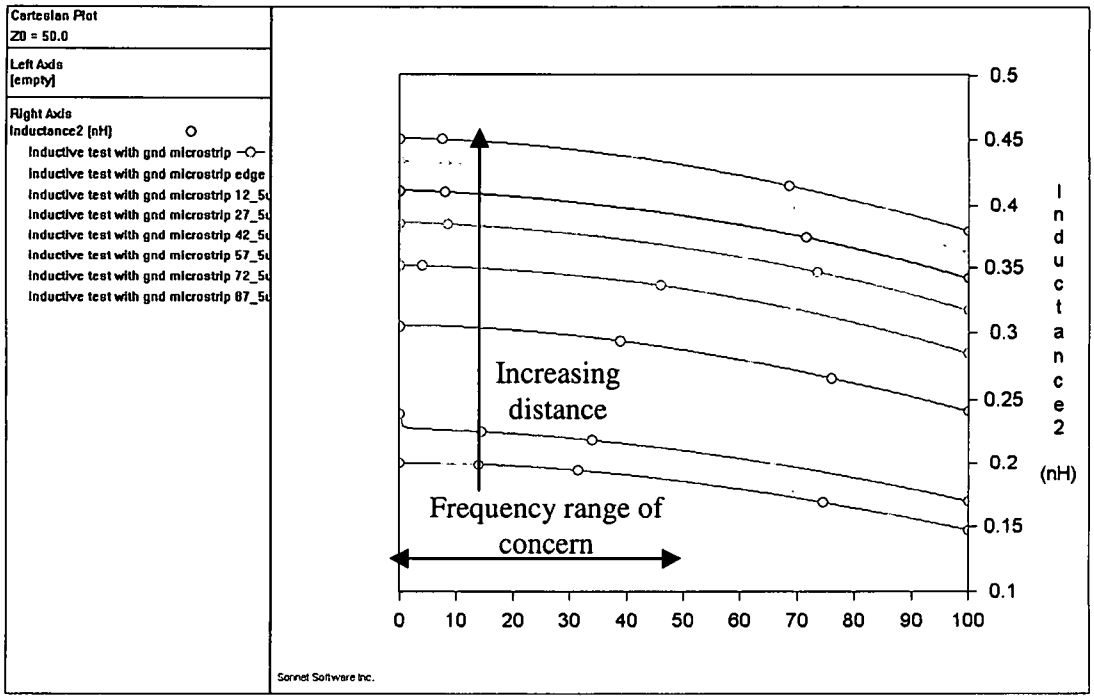


Figure 2-18: Inductance variation due to proximity to microstrip line

The change in capacitance with distance is suspected to be minimal, which is confirmed in Figure 2-19. The separation distance for the capacitor experiments ranged from 0μm (directly underneath microstrip) to 120μm. The capacitance observed at DC is the same in all cases but the deviation is much greater at higher frequencies. For the frequency range under consideration for this work (1-50GHz) the variation in capacitance is not substantial. Variation in inductance is significant and is suspected to be the main cause of the multi-resonant performance. The general approximation used for the inductance in this study has been 0.2nH for a 300μm strip directly below the microstrip at DC, while the capacitance is 0.114pF for the same conditions.

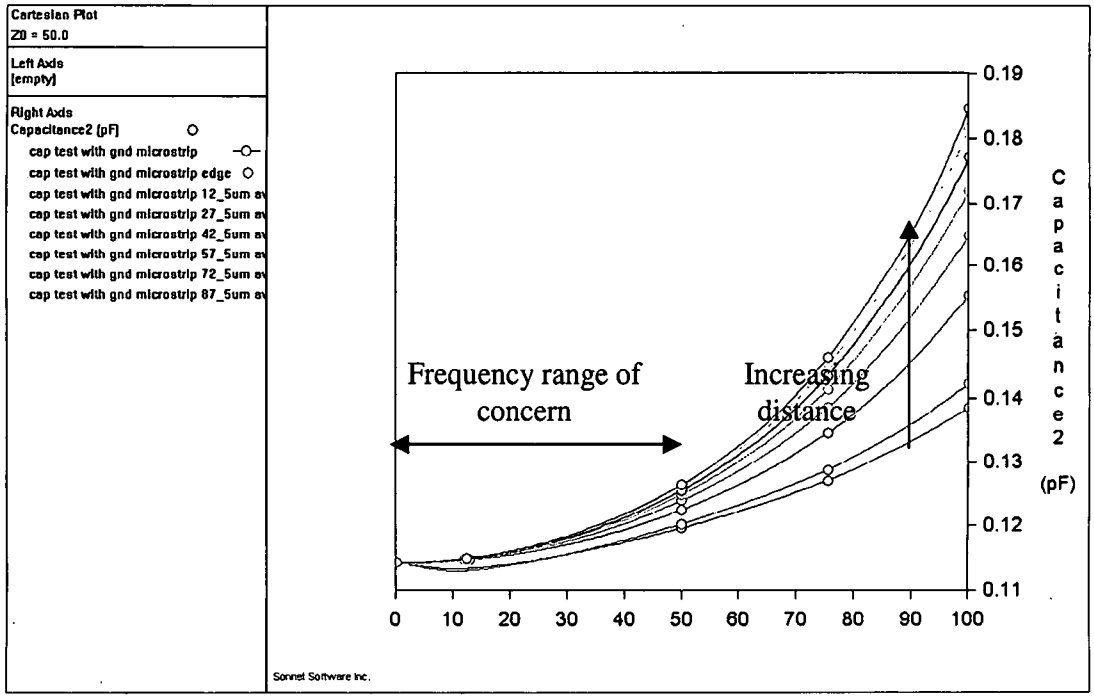


Figure 2-19: Capacitance variation due to proximity to microstrip line

2.4.4 Meander line with Stub

A second design for the ground plane is created based on the basic meander design shown in Figure 2-10. An additional stub of inductance is added to the design and the capacitance is reduced to a third of its previous value by reducing the overlap area from 75μm^2 down to 25μm^2. Most design parameters remain the same as before except that the length of the ground plane is increased by a small amount due to the added stubs. Figure 2-20 shows the meander with the additional stub and Figure 2-21 displays the simulation results for the design with and without the applied bias. The phase difference is also shown along with the result for the meander design without the additional stub. The reduction in the capacitance had the effect of shifting the band stop resonance higher in

frequency, as was expected, and the rejection is also deeper than with the simple meander line design. The increase in inductance increases the depth of rejection, as expected in a parallel resonant circuit.

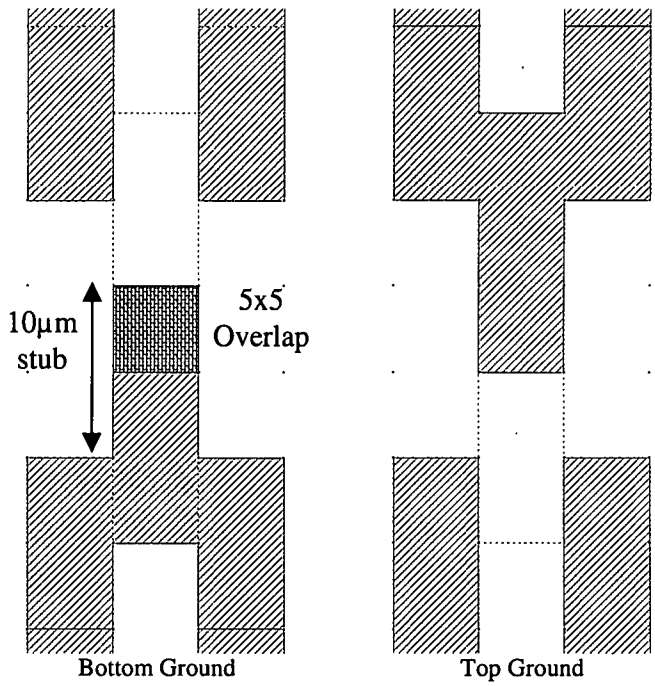


Figure 2-20: Design 2, Meander with 10μm stub layout

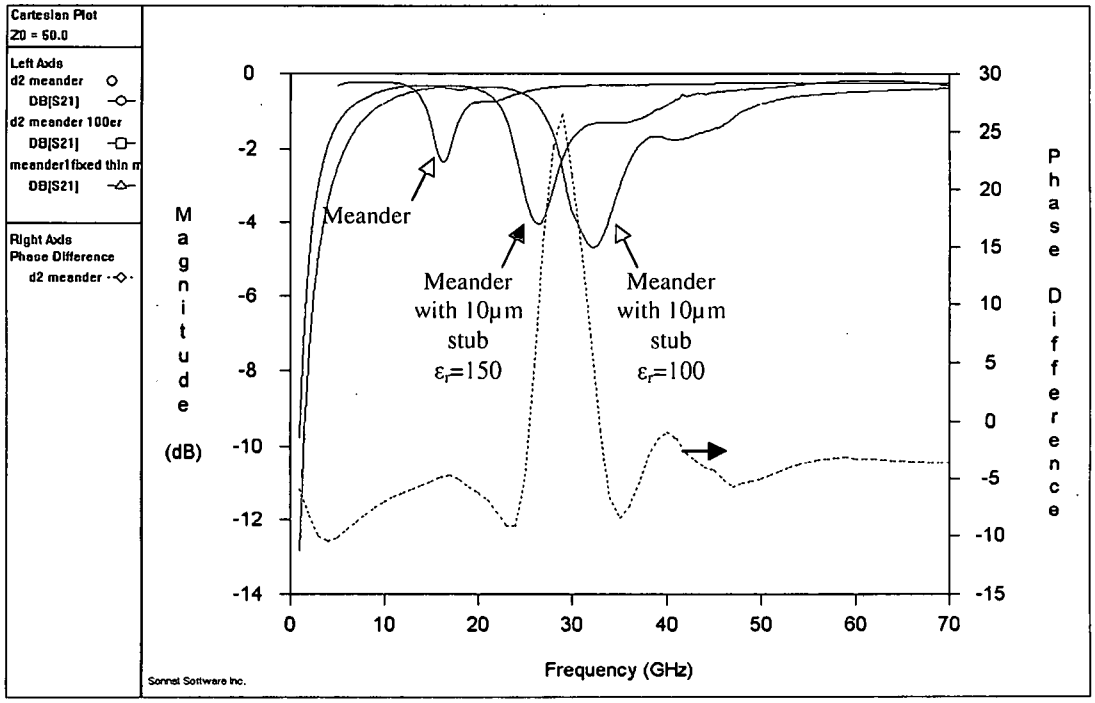


Figure 2-21: Design 2, Meander with 10µm stub simulation results

Another design is created with a 50µm stub in order to isolate the effect of the stub. As expected the resonance is shifted lower due to the additional inductance. The inductance also plays a direct role in the parallel resonance. Figure 2-22 displays the results of the simulation and compares the result with the 10µm stub design. The addition of the 50µm stub increases rejection but the overall response remains similar to the 10µm stub design. At different frequencies different elements of the design may dominate the response. The meander line with the 10µm stub appears to show the most promise and will be used as the design for further investigation into other parameters and design enhancements.

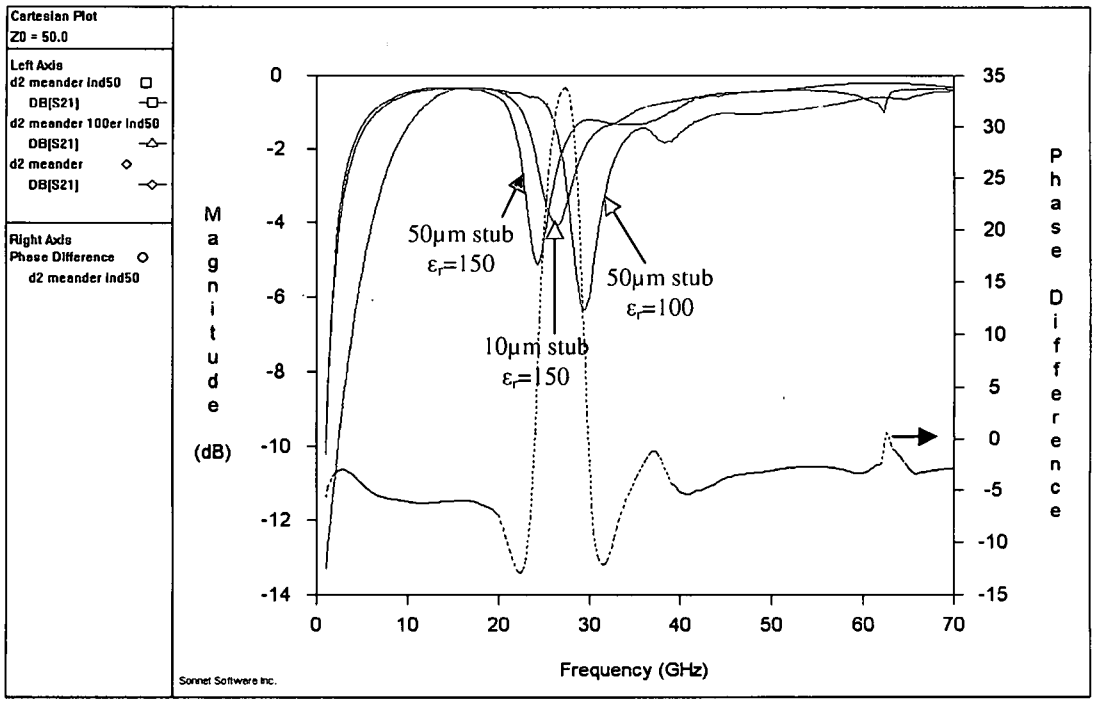


Figure 2-22: Design 2, Meander with 50µm stub simulation results

2.4.5 Meander lines with added strip

The design shown in Figure 2-23 attempts to increase the amount of parallel inductance in hope of controlling the depth of the rejection band. To accommodate the additional strip within the meander line design, the gap between lines had to be increased from 5µm to 25µm. Figure 2-24 displays the simulations results for layouts with no added strips, 5µm wide strips, and 15µm wide strips. The length and width of the inductive strips was changed; however, no major change was produced in the response of the system. No conclusion can be drawn other than that an additional strip in such a configuration will only have negligible effects on the results. The differences observed in the results

shown in Figure 2-21 and those shown in Figure 2-24 may be attributed to the changes in the gap between the meanders.

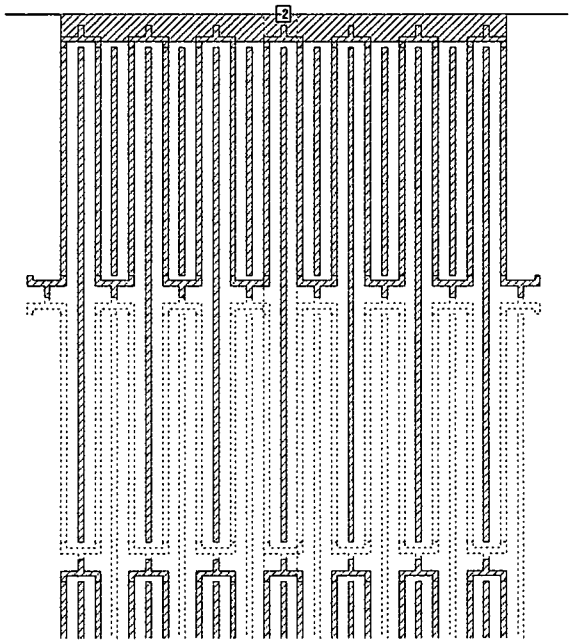


Figure 2-23: Meander with added strips layout

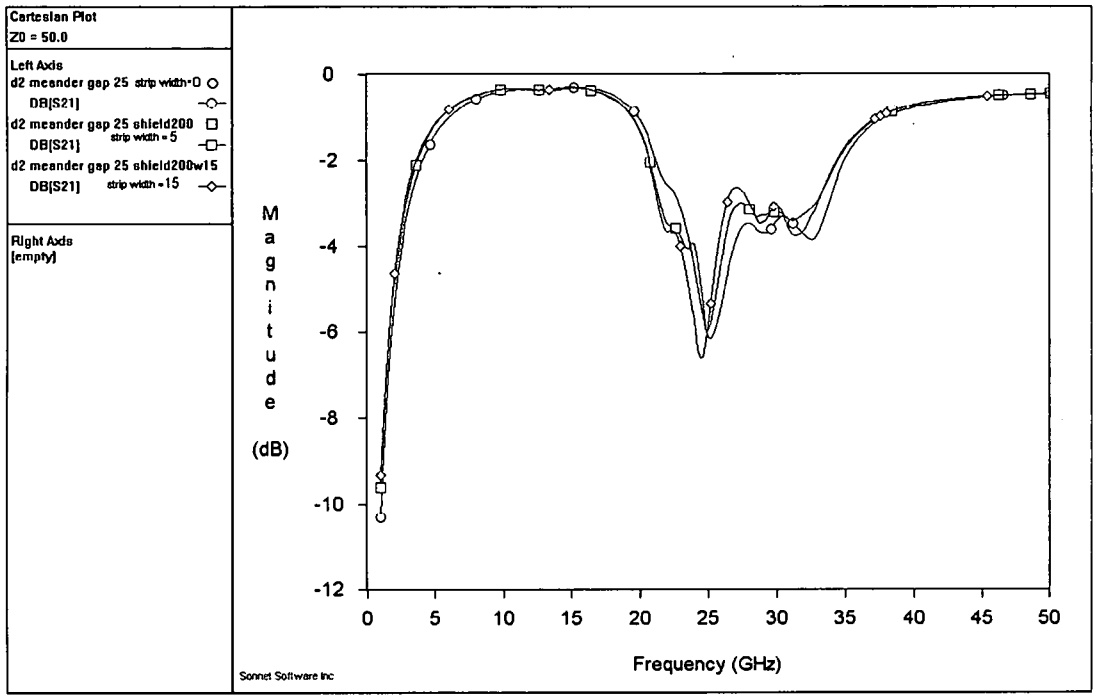


Figure 2-24: Meander with varying added strip width

2.4.6 Meander: Gap Variations

Due to the changes observed in the simulations results shown in Figure 2-21 and Figure 2-24, the effects of the gap between meander lines is explored next. Several simulations are conducted in which the gap is varied between 1μm to 25μm. These are a set of simulations where the 5μm cell size is changed in order to accommodate the smaller dimensions and to maintain symmetry in the design. The number of meanders is kept constant by keeping the number of capacitive couplings between the first and second cell limited to 8 overlapping regions. As the gap is increased the overall width of the ground plane is also increased because each meander occupies a greater width.

Figure 2-25 displays the S21 result of the simulations. The resonances are seen to shift to lower frequencies as the gap width is increased. Figure 2-26 shows the S11 results in which the changes are more pronounced. At present it is not clear whether this shift is due to the gap itself or the fact that the ground plane is increasing in width. To increase the gap width additional metal is added in the stub area which might be adding to the inductance and therefore lowering the observed resonances in frequencies. The other thought is that by increasing the gap the meanders are pushed further away from the microstrip line. Based on the observations made concerning the variation of effective inductance with distance from the microstrip, the result would be to shift the resonances to lower frequencies. A gap width of 20μm produces the greatest rejection but in order to maintain symmetry a cell size of 2.5μm is needed which would increases memory requirements. A gap width of 25μm has slightly less rejection, but the

advantage of a larger cell size reduces the constraints on memory needed for simulations. Increasing the gap further may improve rejection but the lower pass band would deteriorate. Additional investigation concerning the gap and its effect on the response are needed.

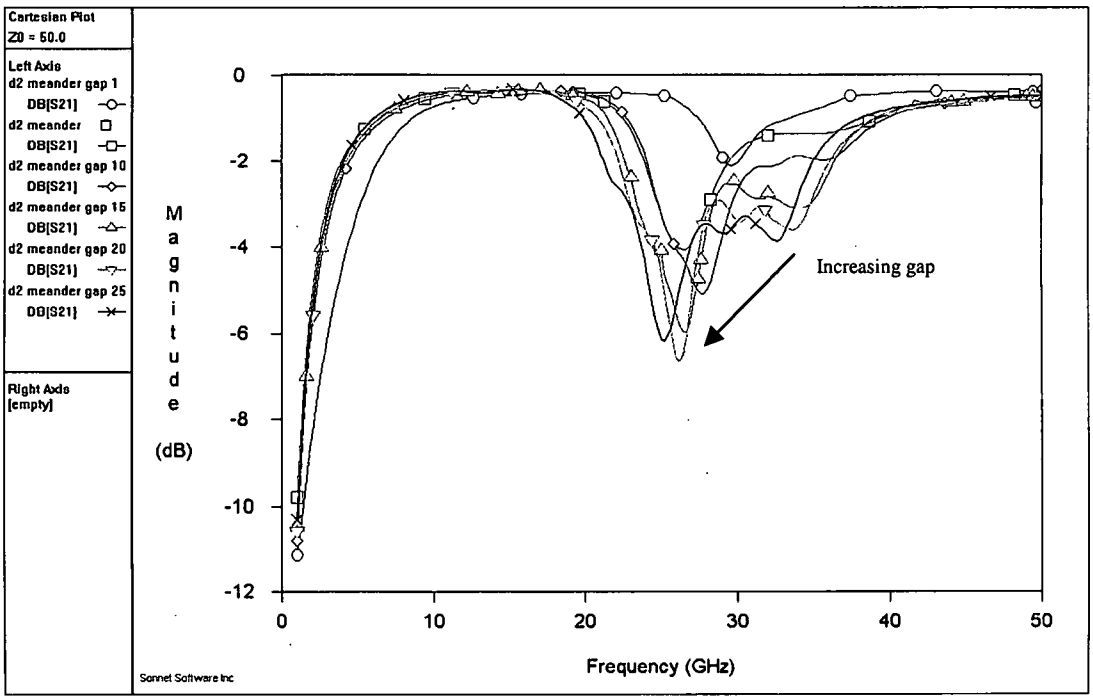


Figure 2-25: Meanders with varying gap width simulation results

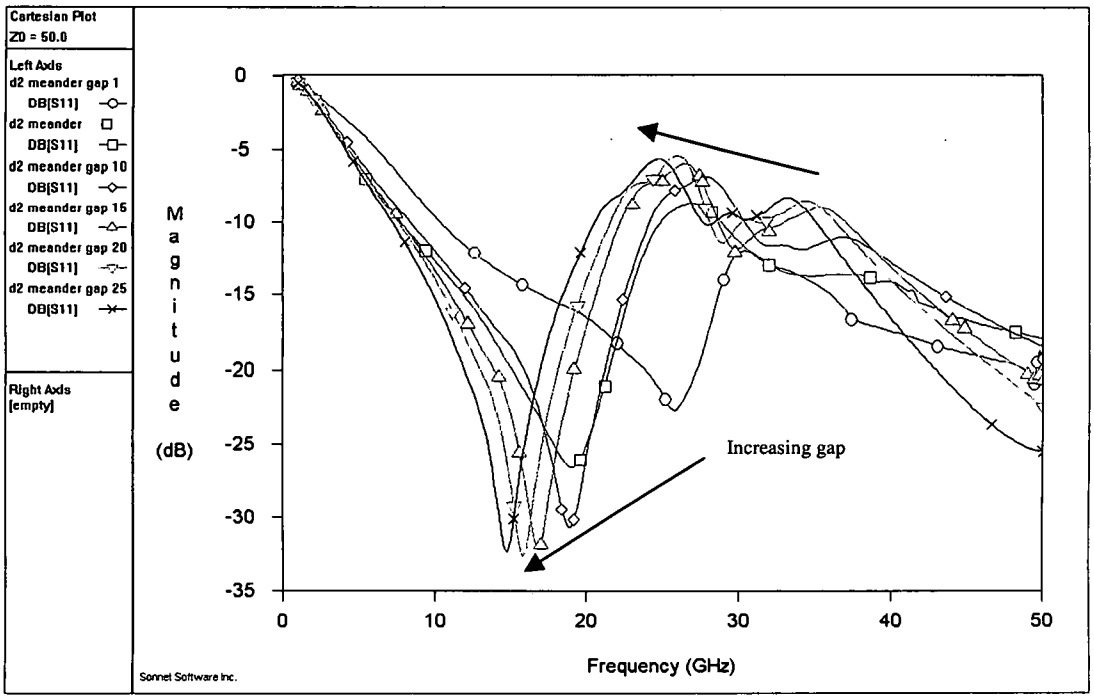


Figure 2-26: Meander with varying gap width S11 results

2.4.7 Meander: Number of Cells

Using a gap width of 25μm and 8 sets of meanders per cell, the effect of increasing the number of cells is investigated. With a gap width of 25μm between meandering line, the overall width of the ground plane is 445μm. As the number of cells is increased in the series direction (along the length of the microstrip line) the length of the ground plane increases from 730μm with 3 cells, to 3550μm with 15 cells. Figure 2-27 shows the results for increasing the number of cells. The general trend is that the rejection is getting deeper with the number of cells in series. There are two clear pass bands around the main rejection band. The curves shown are for 3, 7, 11, and 15 cells in series. Increasing the number of cells further increases the depth of the rejection band but a deterioration of the

first pass band is observed. The meander design with 15 cells shows promise and is later used as a design base for manufacturing purposes.

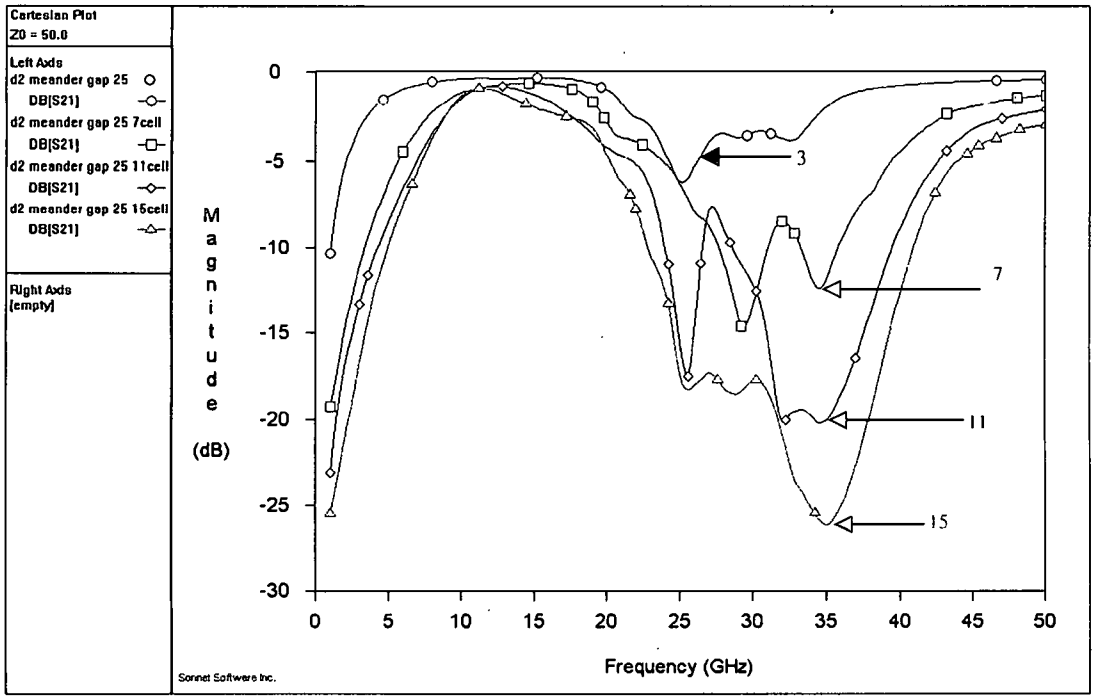


Figure 2-27: Meander with gap 25 and varying number of cells in series

2.5 Design 3: Simple Parallel Strip

The meander design has produced a decent frequency response, but the design is still quite complicated and it is difficult to adjust single parameters. The meanders are also difficult to manipulate because a lot of time and energy is needed even for minor alterations. To solve (or mitigate) the problems associated with the design and analysis of the meander design, a simpler design is needed which can be readily manipulated for parametric analysis. A simplified design along similar lines is created with minor alterations. The advantage that the

meander design has is its inherent dc pathways. A simpler strip design is created that closely resembles the initial concept but with added bias strips perpendicular to the inductive strips. Figure 2-28 shows the basic layout of the structure in the three layers starting from the top.

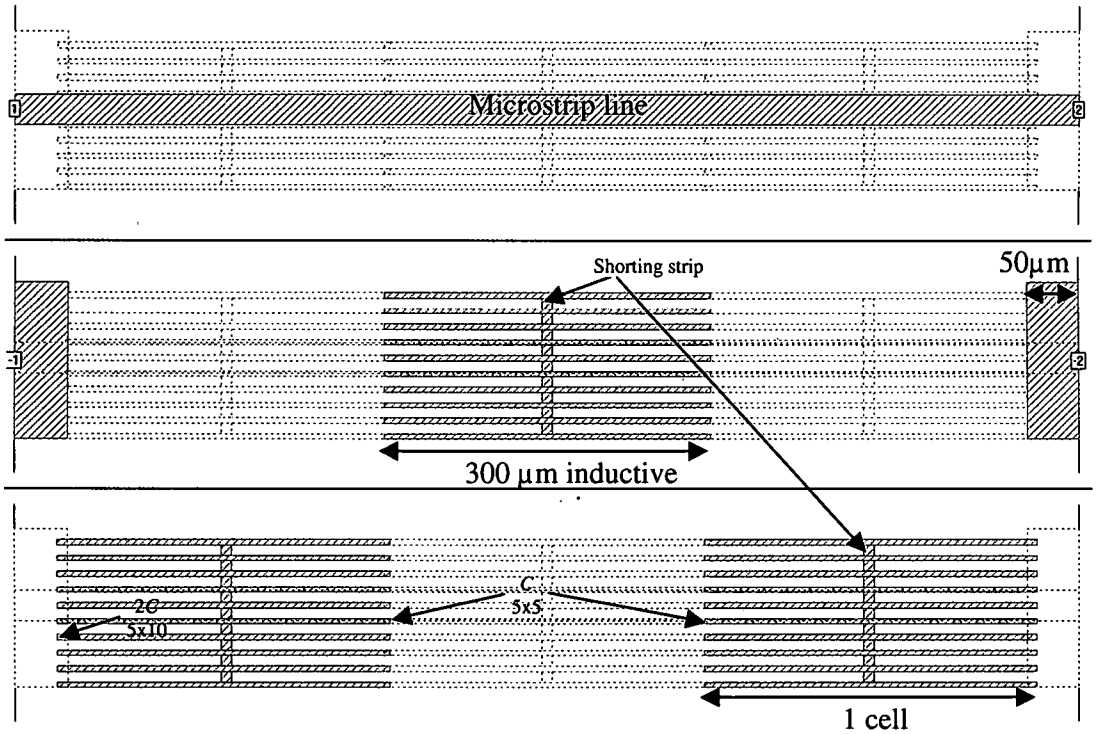


Figure 2-28: Parallel strip layout

Although the designs are very similar, and so is the expected performance, the simpler design allowed for greater manipulation of the layout in order to fully understand the electrical performance of the structure. The number of strips could be easily varied and the gap between them could also be manipulated without hindrance. The layout shown has three cells with 10 5µm strips in each cell. The width of the strip lines is kept constant at 5µm throughout the design process. The length of the strip lines is 310µm; 300µm is for the inductance while

the remaining 10μm is for 5μmx5μm capacitors between strips at each end. Both the length of the inductive strips and the capacitor overlap area is fixed for analysis. The effect of the gap *g* between the strips, the number of strips within one cell, and the number of cells in the ground plane is explored. The influence of the substrate and the shorting strips is also investigated. As before, the cells at the ends of the ground plane are capacitively coupled to the ports. A point of note is that the coupling capacitors at the ends are twice that used between strips, as indicated in Figure 2-28. This is done mainly to maintain symmetry of the unit cell but it is not a fixed parameter. For analysis purposes the S11 curves will be of primary concern because S11 parameters tend to have pronounced variations due to changes. The purpose of the simple parallel strip design is to provide insight into the effects of the various parameters under consideration. S21 response is not of primary concern because this design is not headed towards manufacturing.

The meander structure was designed to have a series *LC* resonance at approximately 33GHz. The simpler parallel strip design was created for a series *LC* resonance of 27GHz. These calculations were done using (2-4) and rules of thumb approximations. In both cases it was found the expected results did not match with the results produced through simulations. As in the case of the unit cell analysis, it was found through simulations that due to the close proximity of the microstrip (10μm) from the ground plane structure, the rules of thumb for inductance do not properly apply. Under the microstrip the inductance of the strips forming the ground plane have an inductance close to half of that expected

by the rule of thumb. Taking into account this change the new series resonance is expected to be approximately 35GHz. The simulation results confirm this resonance. As mentioned earlier, the exact relationship between the strip length and the location of the resonance is not of concern, but the fact that the resonance can be adjusted using the length of the strips into a certain frequency band is enough for the purposes of this work.

2.5.1 Number of strips

Figure 2-29 shows the S11 simulation results with increasing number of parallel strips while keeping the gap constant at 10μm and the number of series cells fixed at 3. A wide range is used for the number of strips; starting from a minimum of 1, up to 45. The S1 plots for 2, 3, 6, 10, 15, and 45 parallel strip designs are shown. Several key observations can be made based on the simulated data. As the number of parallel strips is increased the series resonance tends to shift down to lower frequencies. This may be caused by the increased observed inductance as the strips in the ground plane are moved away from the microstrip. The higher inductance paths resonate at lower frequencies thus producing pass band regions. Devices with large number of strips provide alternate paths for the signal to flow at different frequencies. S21 results for 2 parallel strips and 45 parallel strips in Figure 2-30 clearly show the shifting of the resonances to lower frequencies with the increase in the number of strips.

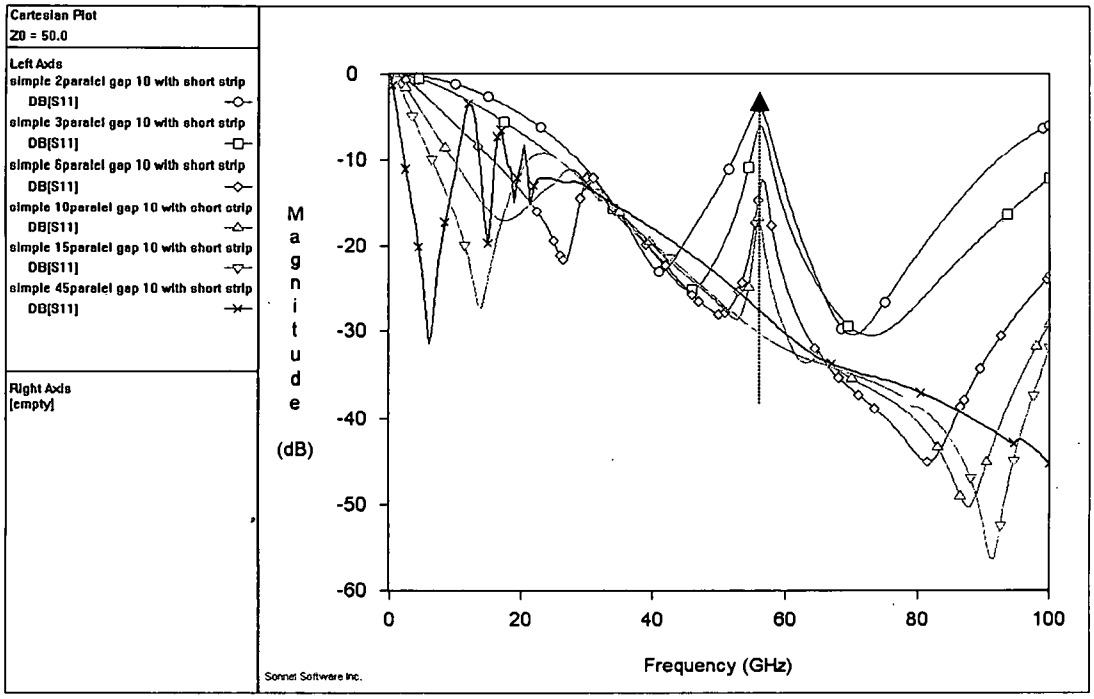


Figure 2-29: Parallel strip, S11 simulation, Variation of number of parallel strips

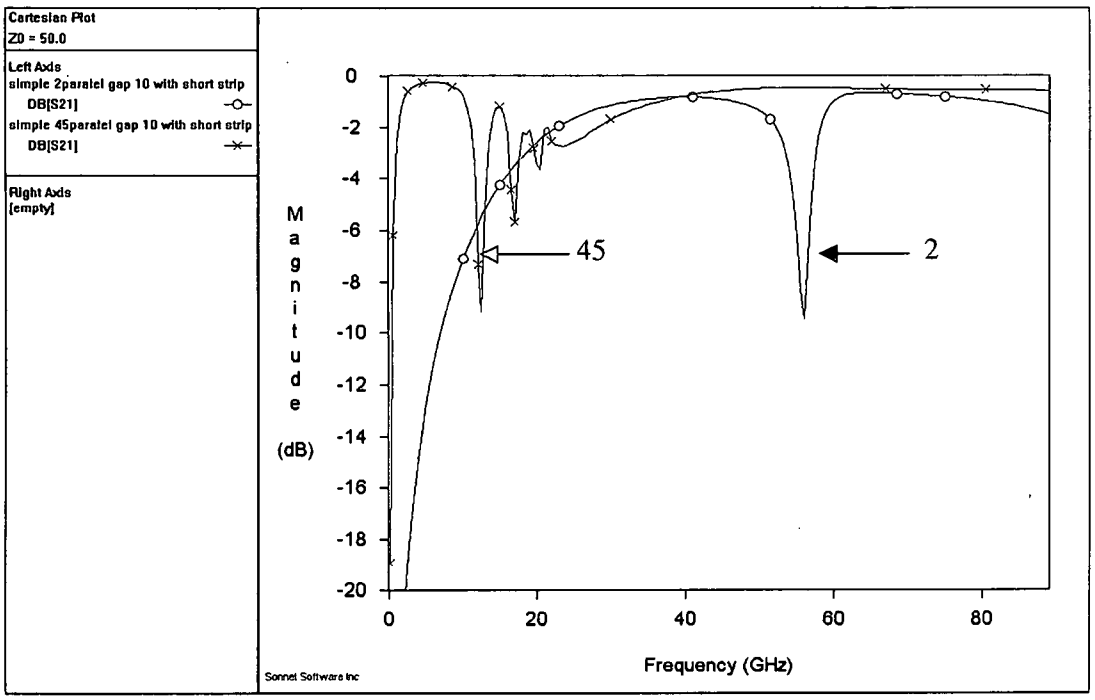


Figure 2-30: Parallel strip, S21 simulations, 2 and 45 parallel strips

The resonance observed at 56GHz in Figure 2-29 remains fixed until the number of strips is greater than 10. This particular resonance is a result of substrate and box resonance. With only a small number of strips shielding the silicon substrate, the microwaves are able to penetrate the substrate. The resonance observed at 56GHz is a result of the resonance of the silicon substrate itself. The resonance frequency of the substrate is partly dependent on the dimensions of the substrate, and in the case of Sonnet simulations, the box size. The box size used for most of the simulations was fixed except for the structure with forty-five strips, for which the box size had to be increased. In general the ground plane must be five to seven times wider than the microstrip for it to provide effective shielding of the substrate. Figure 2-31 displays the S_{11} simulation results for a 2 parallel strip structure, with and without silicon substrate. The series *LC* resonance in both cases remains fixed near 42GHz, but the resonances observed at 55GHz and 70GHz disappear once the silicon substrate is removed. For the case without silicon, the maxima observed at 65GHz may be attributed to the quarter wavelength resonance between the ports. The two curves are well matched below the *LC* resonance.

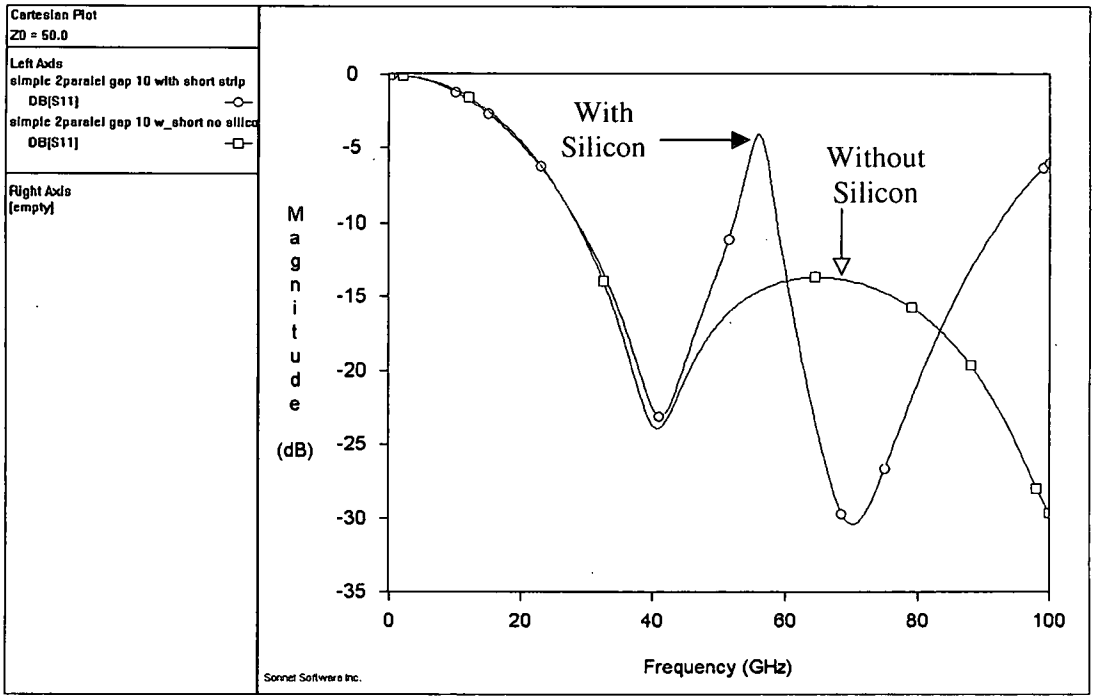


Figure 2-31: Parallel strip, S11 simulation, 2 strips with and without silicon substrate

As the presence and absence of the substrate has significant effect on the response of the device, simulations were conducted again without silicon. Figure 2-32 displays the simulations results for the same devices as shown in Figure 2-29 but the silicon substrate has been removed. As expected, the resonance at 56GHz has been eliminated. The absence of the substrate has also changed the responses slightly but the results are still comparable. Another observation is that a series resonance located at around 40GHz for a 2 parallel strip structure, moves to higher frequencies as the number of strips is increased. Above resonance mainly inductive effect is observed and the capacitors appear as approximate shorts; however, as the number of strips in parallel is increased, the over all inductance is reduced due to parallel combination, thus pushing the resonance into higher frequencies. Increased positive mutual inductances and

added parasitics may also have a greater impact with the increased number of parallel strips.

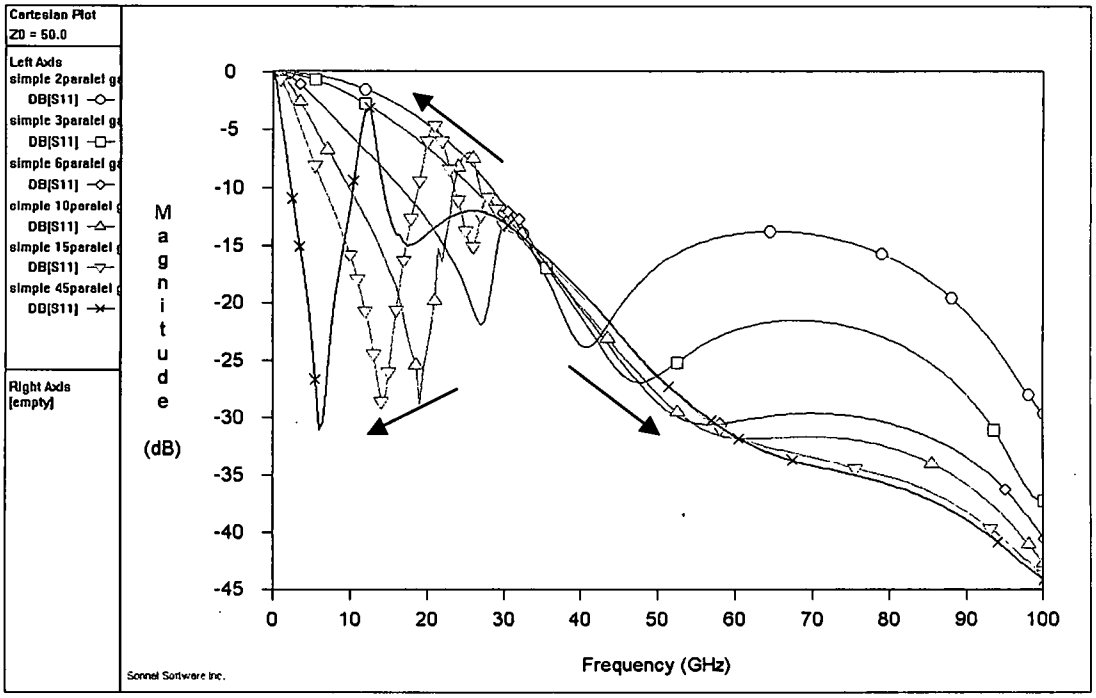


Figure 2-32: Parallel strip, S11 simulation, Variation of number of parallel strips without silicon substrate

2.5.2 Gap between strips

The spacing between the parallel strips also has some effect on the function of the device. Figure 2-33 displays the S11 simulation results for a 2 parallel strip structure limited to 3 cells in series. The results are for devices with gaps of 5, 10, 15, 20, 25, 30, and 35μm between the parallel strips. The simulations were conducted in the presence of a silicon substrate and without shorting strips. As the gap width is increased the series *LC* resonance behaves in a very peculiar manner. With increasing gap size the resonance first moves to higher

frequencies, from an original resonance at 38.5GHz with a 5μm gap, to a maximum of 42.5GHz with a gap of 15μm. With further increases in the gap spacing the *LC* resonance shifts down to lower frequencies. The position of the strips below the microstrip and the proximity of the strips to the microstrip may have a direct effect on the response of the structure. With only 2 parallel strips, changes in the gap size significantly effects the relative positions of the strips underneath the microstrip. Simulations were conducted again for the same structures but with the absence of silicon substrate and the presence of shorting strips. The same phenomenon as before is observed in the behavior of the series *LC* resonance. The S11 simulation results for gap widths of 5, 10, and 30μm without silicon substrate are displayed in Figure 2-34.

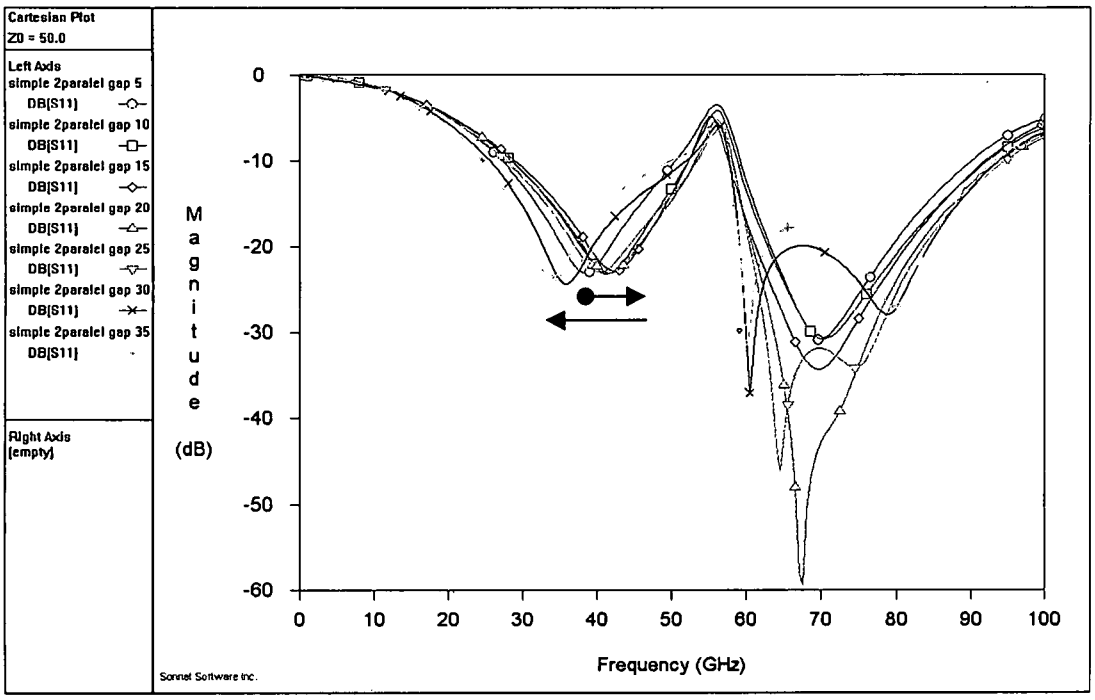


Figure 2-33: Parallel strip, S11 simulations, 2 parallel strip device with gap variation, no shorting strips

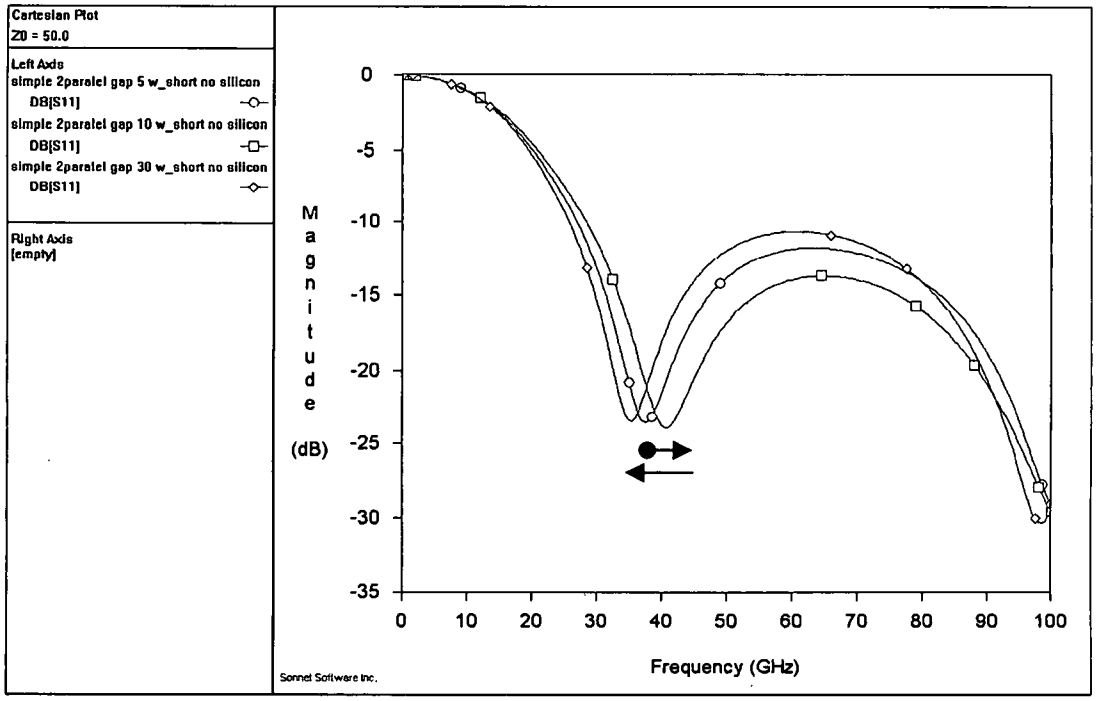


Figure 2-34: Parallel strip, S11 simulations, 2 parallel strip device with gap variation without silicon

To further observe the effect of the gap, simulations were performed as before, but with the number of strips increased to 3. The number of series cells is still limited to 3 cells, with shorting strips used, and the silicon substrate removed. In the previous experiment when only 2 parallel strips were used, an increase in the gap altered the position of the strips directly under the microstrip. Using 3 parallel strips limits the effect of position change as the central strip will always lie directly beneath the microstrip. Figure 2-35 shows the S11 simulation results for gap widths of 10, 30, and 60μm. More simulations at smaller intervals are needed in order to verify if similar behavior as that shown in Figure 2-33 and Figure 2-34 is observed. A general observation is that the response is directly dependent on the

width of the ground plane. Increasing the gap while maintaining the number of parallel strips causes the width of the ground plane to increase in direct proportion to the increase in the gap.

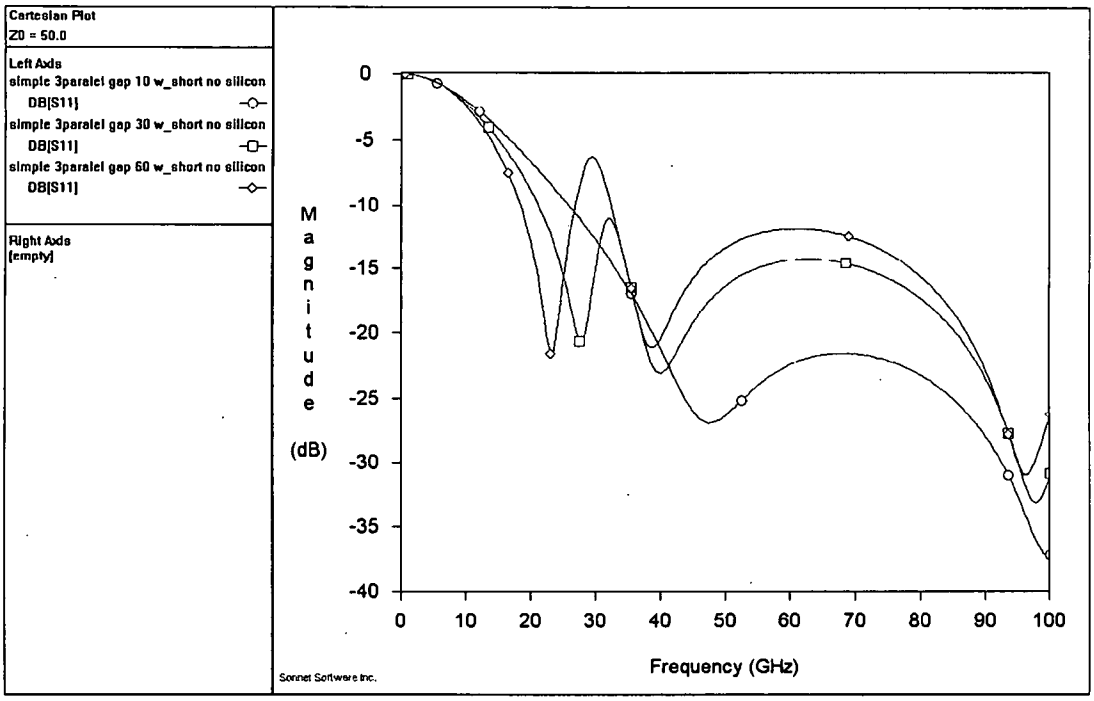


Figure 2-35: Parallel Strip, S11 simulation, 3 parallel strip device with gap variation without silicon

2.5.3 Shorting strips

The effect of the shorting strips is expected to be minimal, especially when the number of parallel strips is small. The shorting strips should play a greater role when much larger numbers of strips are used. Figure 2-36 displays the S11 simulation results for a 6 parallel strip structure. Of the three curves shown, one design is without shorting strips, the second with only one shorting strip per cell, and the final design is with three shorting strips per cell. As expected, the

deviations between no shorting strips and one shorting strip per cell are minimal. Only at much higher frequencies are the differences between the two curves more noticeable, but still negligible. The excessive shorting produced by using three shorting strips alters the behavior of the structure. These results show that the addition of one shorting strip per cell for designs with a small number of parallel strips should not significantly alter the performance of the device. In all three simulations the gap width is 10μm with 3 cells in series, and in the presence of silicon substrate.

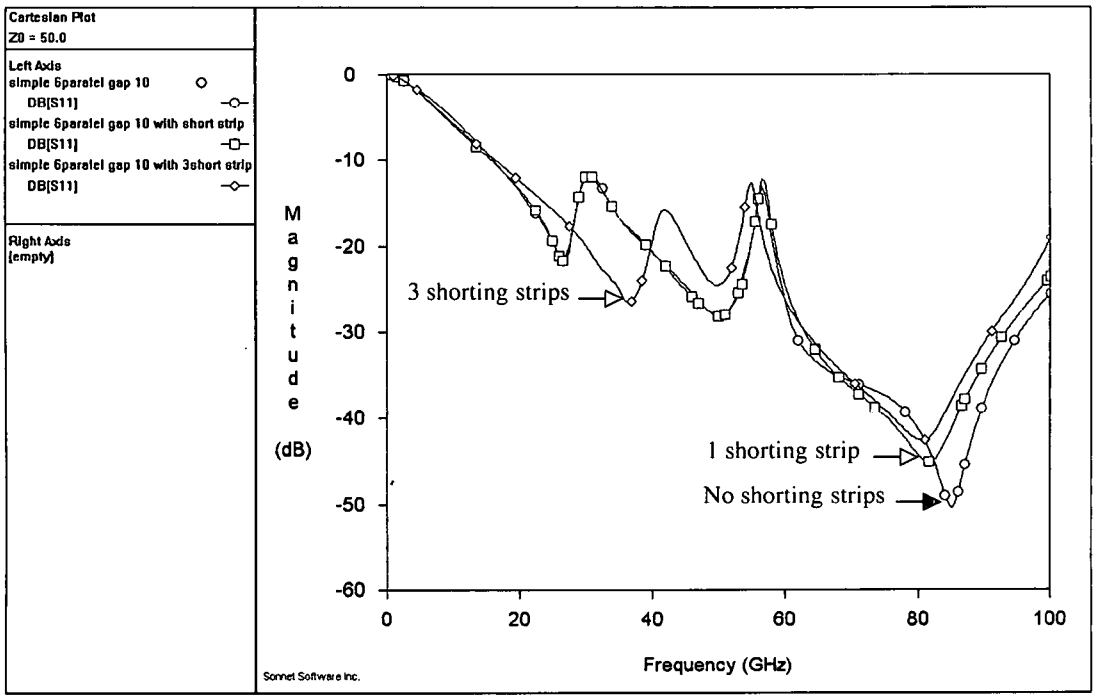


Figure 2-36: Parallel strip, S11 simulation, 6 strip design with shorting strip variations

The effect of the shorting strips on designs with a much larger number of strips is observed in the S11 simulations results shown in Figure 2-37. The S11 simulation results are for a single cell of 45 parallel strips without silicon

substrate. One structure has no shorting strips while the other has only one main shorting strip running down the center of the device, the third device has three equally spaced shorting strips. With the higher number of parallel strips the presence of the shorting strips significantly alters the performance of the design at lower frequencies. Addition of more shorting strips suppresses some of the smaller resonances that appear at lower frequency. A minimum of one shorting strip is necessary to allow DC biasing of the ferroelectric film in the overlapping regions. The shorting strips may be responsible for setting up parallel *LC* resonances which may account for the rejection bands at the lower frequencies. Parallel *LC* resonances may prove beneficial in setting up deeper rejection bands. The effect of the position of the shorting strips has not been fully explored. The location and the number of shorting strips is one of many factors that influence the performance of the system. Dissecting the structure and understanding the complex interactions of these factors requires an in depth study. The full breadth of factors cannot be duly explored due to the limited scope of the present study.

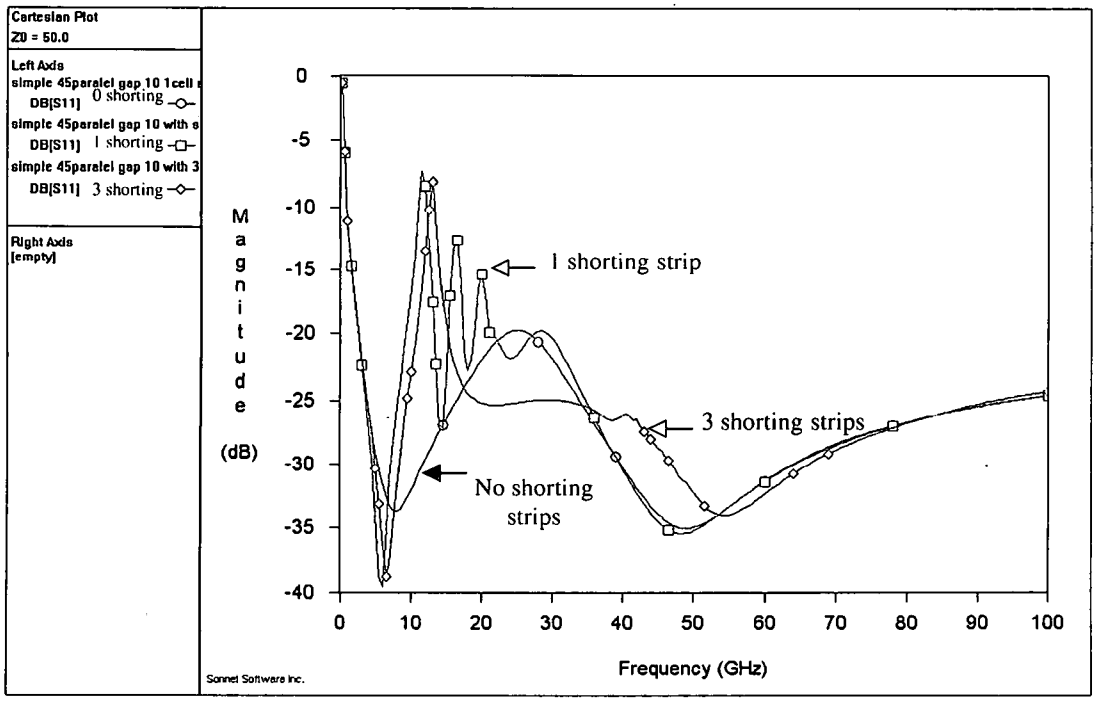


Figure 2-37: Parallel strip, S11 simulation, 45 strip design with shorting strip variations

2.5.4 Number of cells

Figure 2-38 displays the S11 simulation data for 2 parallel strip devices with increasing number of cells in series. The devices were simulated with one shorting strip per cell without a silicon substrate and a gap of 10μm between strips. The results shown are for 1, 3, 6, 9, and 11 cells in series. In all cases the series *LC* resonance appears to remain stationary in the region of 40GHz. Other resonances move to lower frequencies as the number of cells is increased. These resonances may be attributed to the quarter wave length, half wave length, and their multiples which resonate at lower and lower frequencies as the number of cells is increased due to the greater line length. The length of the line

is only 400μm with 1 cell, and 3450μm with 11 cells. The sharpness of the dip in the S11 curve also increases with the number of cells in series.

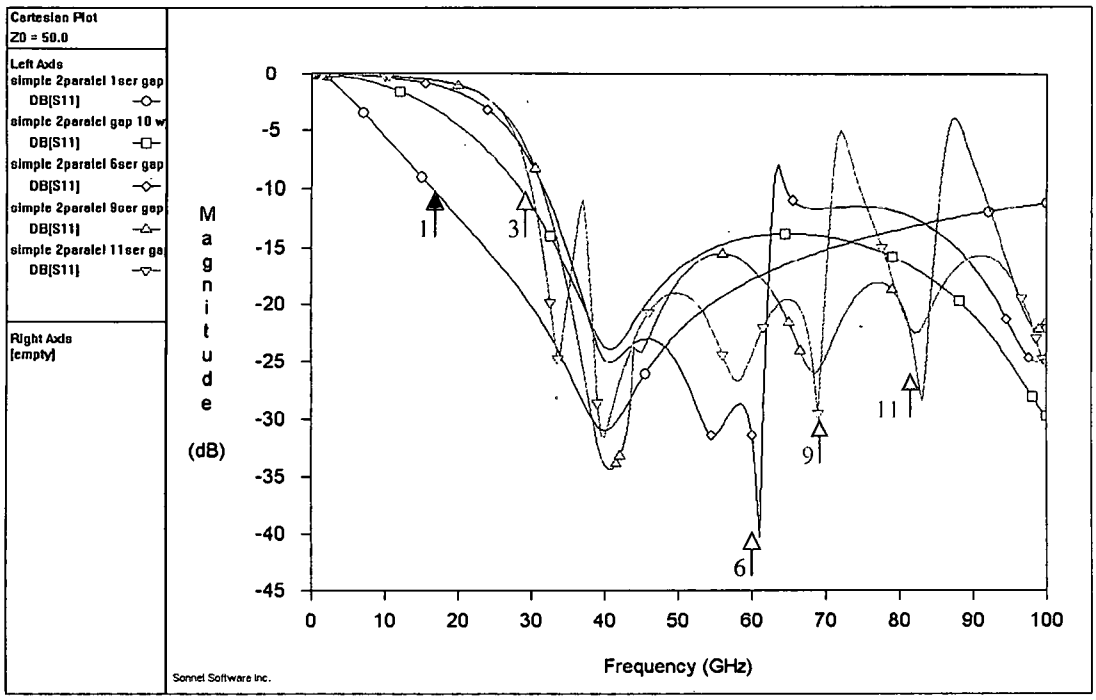


Figure 2-38: Parallel strip, S11 simulation, 2 strip design with number of cell variation

A similar set of simulations as above is conducted but the number of parallel strips is increased to 45. The gap between strips is kept fixed at 10μm and the silicon substrate is absent. As expected, the rejections are made deeper by increasing the number of cells in series. The number of resonances observed is also increased. Figure 2-39 displays the S11 simulation results for 45 strip devices using 1, 3, 4, 7, and 9 cells in series. Figure 2-40 displays the S21 curves for the same set of designs and shows the increase in the rejection level with the number of cells used. S11 simulations results for 2 and 5 cells produced anomalous results and are shown in Figure 2-41. A 6 cells simulation, also

shown in Figure 2-41, shows a response similar to both groups. At present no explanation has been found for the behavior presented. More simulations need to be conducted in order to find some pattern in the effect of the number of cells on the response of the device. The odd behavior may be caused by parasitics or by the setup of an unaccounted resonant structure.

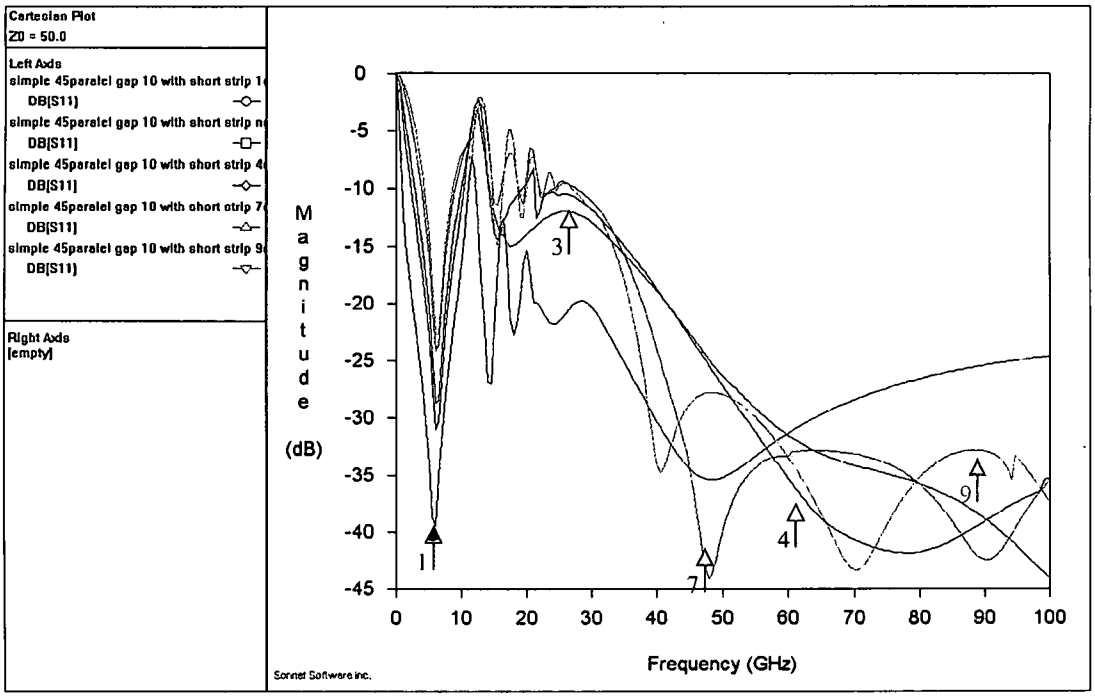


Figure 2-39: Parallel strip, S11 simulation, 45 strip design with number of cell variation (1, 3, 4, 7, 9)

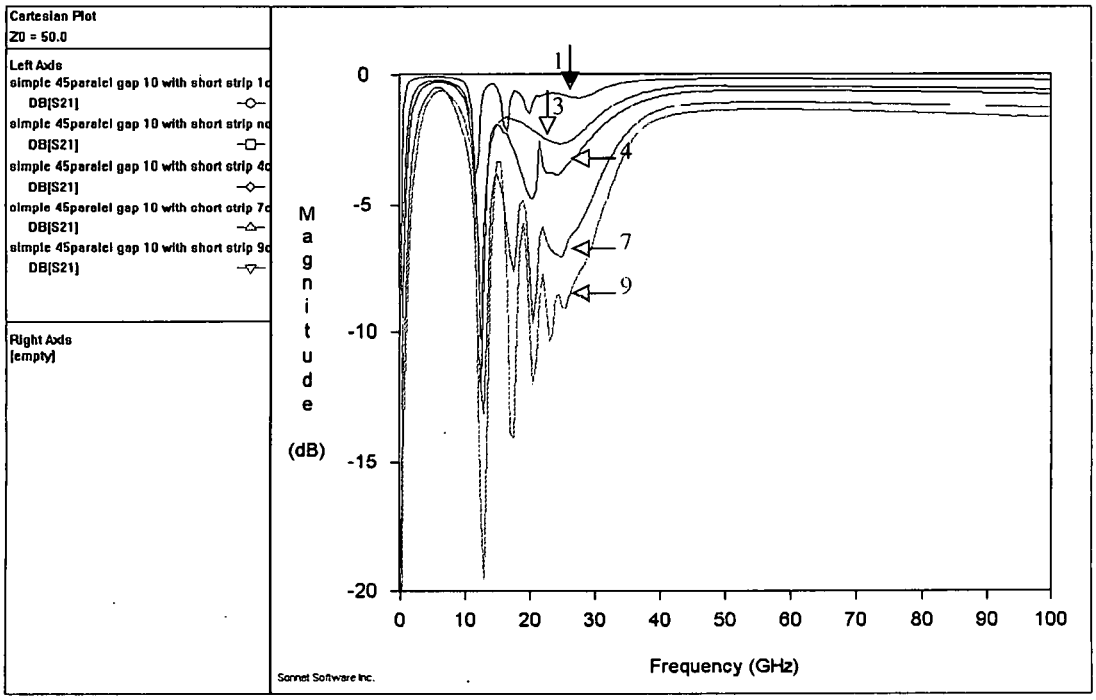


Figure 2-40: Parallel strip, S21 simulation, 45 strip design with number of cell variation (1, 3, 4, 7, 9)

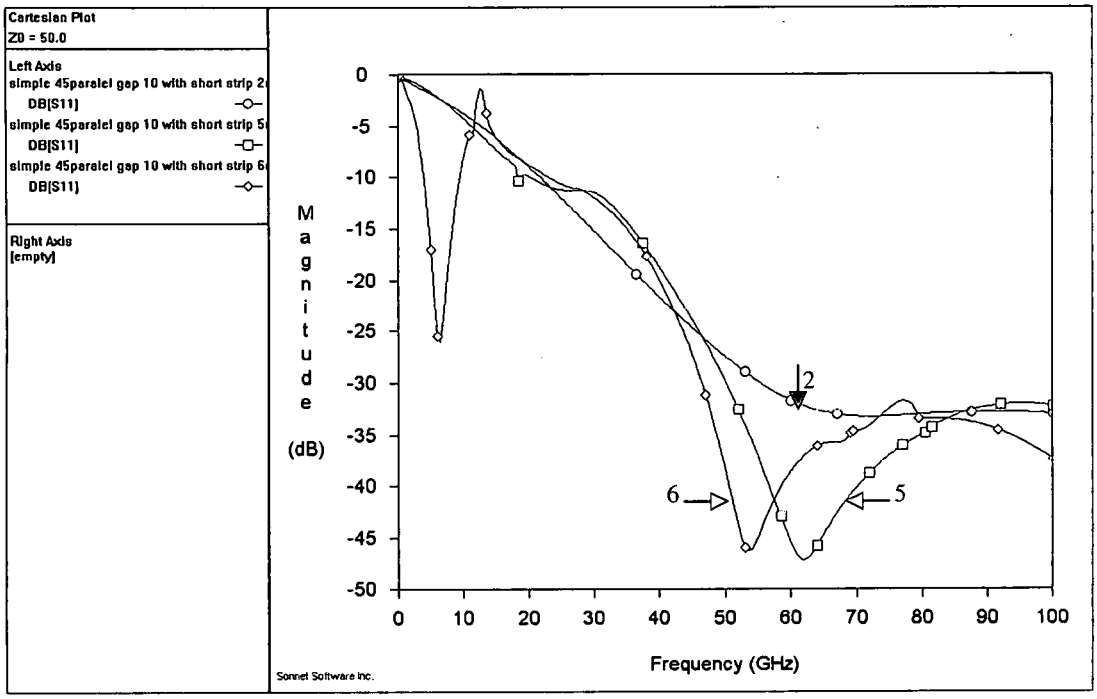


Figure 2-41: Parallel strip, S11 simulation, 45 strip design with number of cell variation (2, 5, 6)

2.5.5 Ground plane width

Up till now both the gap width and the number of strips have been viewed as primary parameters in the analysis; however, alteration of either of these parameters has the consequence of altering a secondary parameter, namely the width of the ground plane. A possible hypothesis is that ground planes of similar width should behave in similar manners. Using combinations of gap size and the number of strip, several variation of the parallel strip design can be formed while keeping the width of the ground plane approximately the same. Figure 2-42 shows the S11 simulation results for four devices having the ground plane width ranging from 125μm to 140μm, while using different combinations of gap width and number of strips. The designs were simulated with one shorting strip per cell, for three cells, and without silicon. All four simulations display similar responses with resonance at the lower frequencies only deviating by 4GHz at the most. The performance levels of the simulations are better matched than with just gap or number of strip variation alone. The effects of the parasitics cannot be controlled or removed; therefore some deviations are to be expected. The results in Figure 2-42 do support the theory that the width of the ground plane is a contributor to the response of the device. The overall performance is determined by a complex contribution of effects from the gap and the number of strips, making it difficult to isolate the effect of the individual parameters.

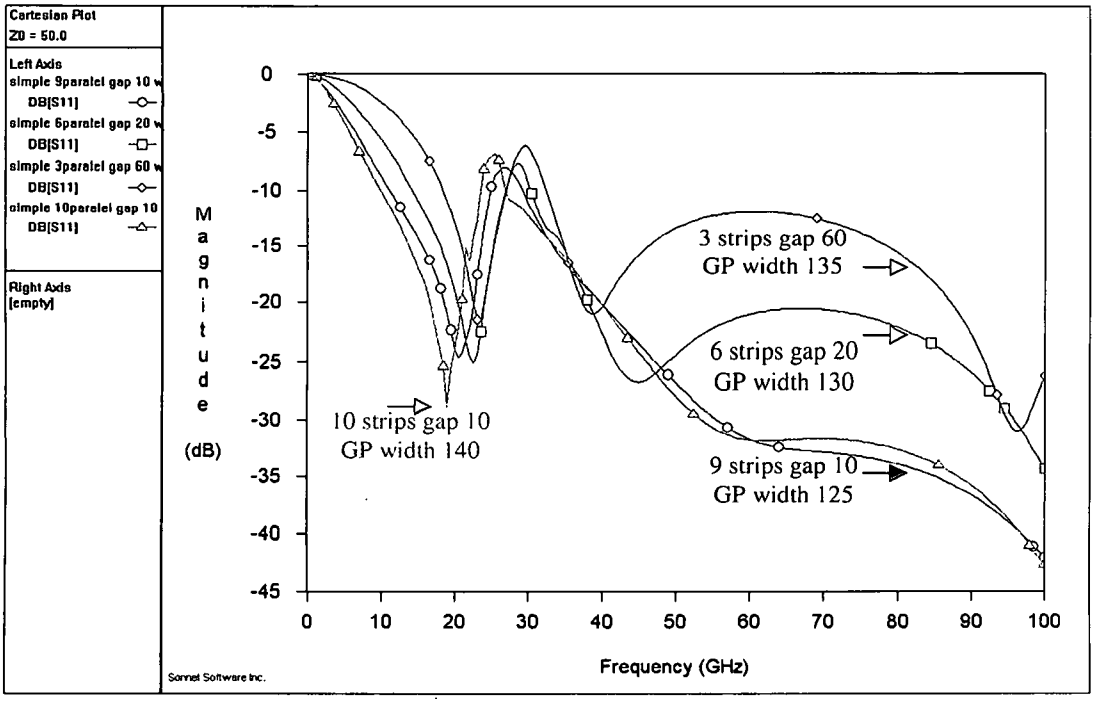


Figure 2-42: Parallel strip, S11 simulations, maintaining ground plane width

Further simulations need to be conducted to fully understand the effects of the gap, and the number of parallel strips. Figure 2-43 displays the S11 simulation results for devices with only one cell and no silicon. In one case the gap is 10μm and the number of strips is 45, while in the other case the gap width is increased to 20μm. To keep the width of the ground plane approximately the same in both cases, the number of strips had to be reduced to 28 for the design with the 20μm gap. A third case is shown in which 28 strips are used with a gap spacing of 10μm; however the width of the ground plane is reduced. The results are not conclusive, but do add to the available information. At lower frequencies a change in the response is observed due to the number of strips used. The deviations are small and it is unclear whether it is caused by the variation in the number of strips or is just a result of varying parasitics. A similar change is

observed at higher frequencies, but this change appears to stem from the variation in gap and not the width of the ground plane. Table 2-5 attempts to organize the variation in the designs and compares them to the effect at low and high frequency; i.e. below and above the main *LC* resonance. The 'X's mark areas where two designs share the same attribute. From the table it appears that the width of the ground plane is only a secondary factor, while the number of strips and the gap width are primary contributors to the behavior of the device.

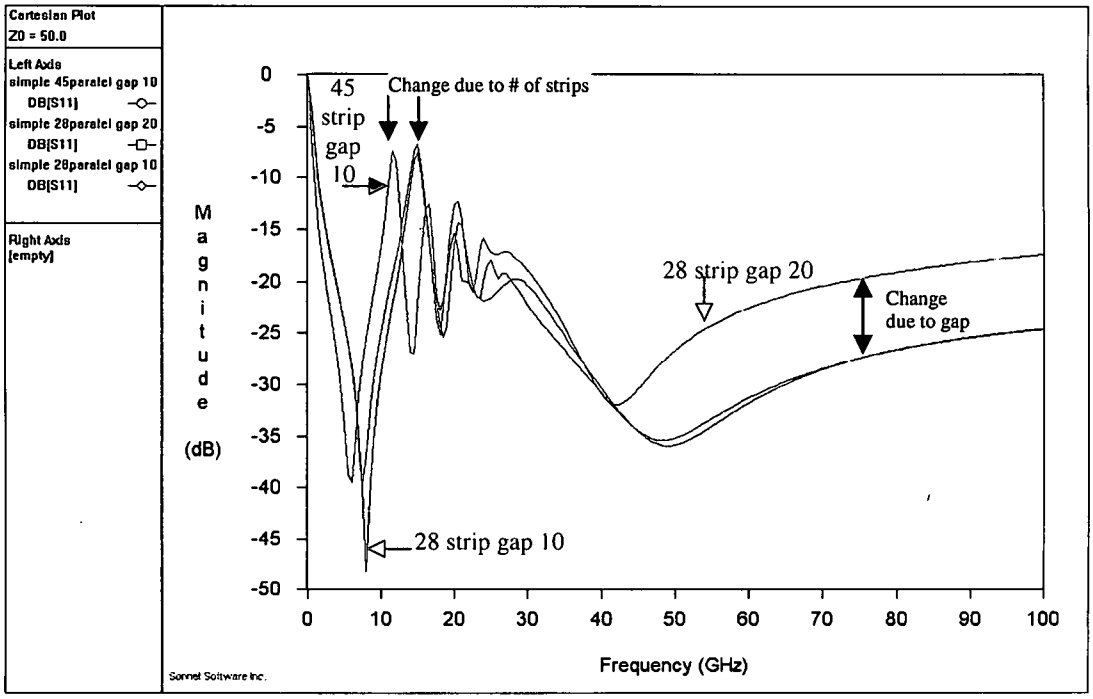


Figure 2-43: Parallel strip, S11 simulation, variation of gap and number of strips

Design	Width of Ground plane	Number of strips	Gap size	Low frequency	High frequency
45 strips gap 10	X		X		X
28 strips gap 20	X	X		X	
28 strips gap 10		X	X	X	X

Table 2-5: Summary of results for variations of gap size and number of parallel strips

More simulations are conducted, exploring the effect of gap and the number of strips. In Figure 2-44 are the simulation results for a design in which the gap is sequentially changed between 10μm and 20μm. The result is compared to previous responses of 45 parallel strips with a gap of 10μm and 28 parallel strips with a gap of 20μm. The new design has the same over all ground plane width as the other two results shown but is comprised of 35 parallel strips. The same conditions as for the simulations shown in Figure 2-43 are used. Similar behavior is observed at low frequencies. The larger number of strips pushes the lower resonances lower in frequency. The same deviations in results is seen at higher frequencies as those shown in Figure 2-43. No conclusive result is found and no generalization can be clearly supported. Further experimentations with gap width, number of parallel strips, and ground plane width are needed.

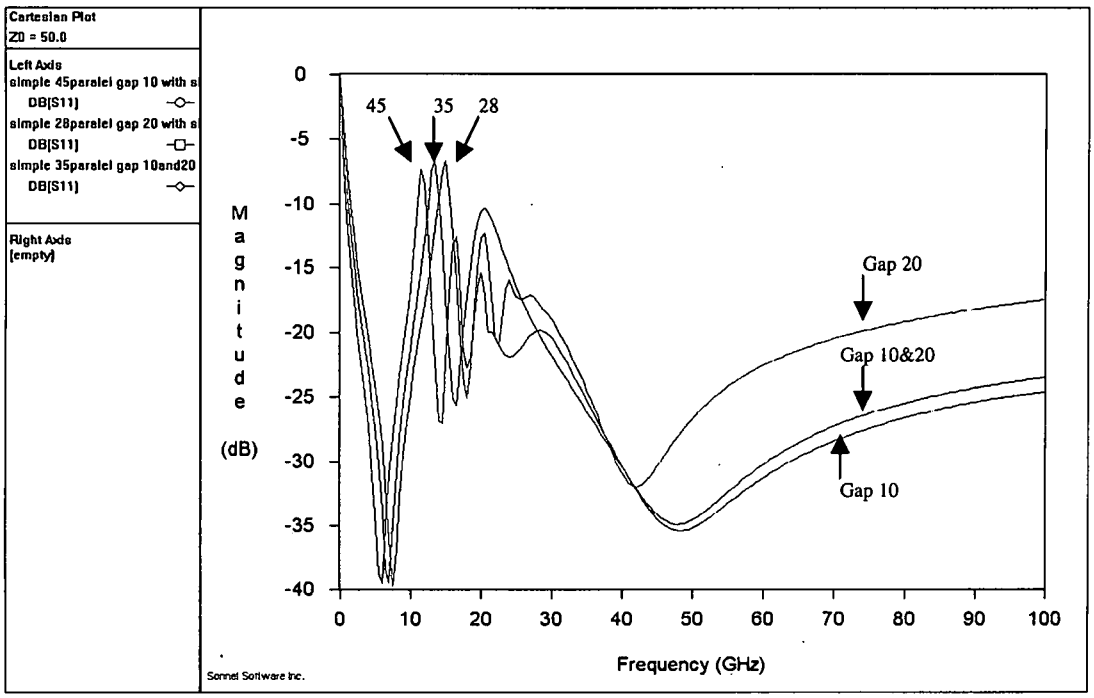


Figure 2-44: Parallel strip, S11 simulation, maintaining ground plane width

2.6 Discussions on the Simulation Results

The purpose of the parallel strip design was to provide further insight into the parametric design and to isolate the contributing factors. The results from the simulations show that the problem is quite complicated and conclusive results are difficult to obtain. It does make one appreciate the complexity of the problem and how various factors can contribute to generate an overall response. All three proposed designs stemmed from the same initial design and for general purposes, generated similar response features. These features could be controlled to a certain extent by altering the design dimensions. In this section an attempt will be made to explain the generalized frequency response observed. The meander line design has shown the best results and therefore will be used for explanation purposes. Although a unit cell that represented the entire system could not be found, an attempted unit cell can be used to explain the simulated electrical response. It is clear that different aspects of the design contribute to the response depending on the frequency. Although resistive losses exist at all frequencies, for the purposes of this explanation they will be neglected and the effects of the inductance and the capacitance will be focused on.

According to the original theory the surface should have had high impedance at low frequencies due to the presence of the capacitors, while at high frequencies the inductance would be responsible for low transmission. At resonance the inductive and capacitive contributions to the impedance would eliminate each other, and assuming no resistance, there should be perfect transmission through the device. The results show that the situation is not as simple as initially

predicted. Such a static analysis cannot deal with the broad range of frequencies being considered. Bearing in mind that different aspects of the design contribute to the performance at different frequencies; the response can be broken down into five areas as shown by Figure 2-45.

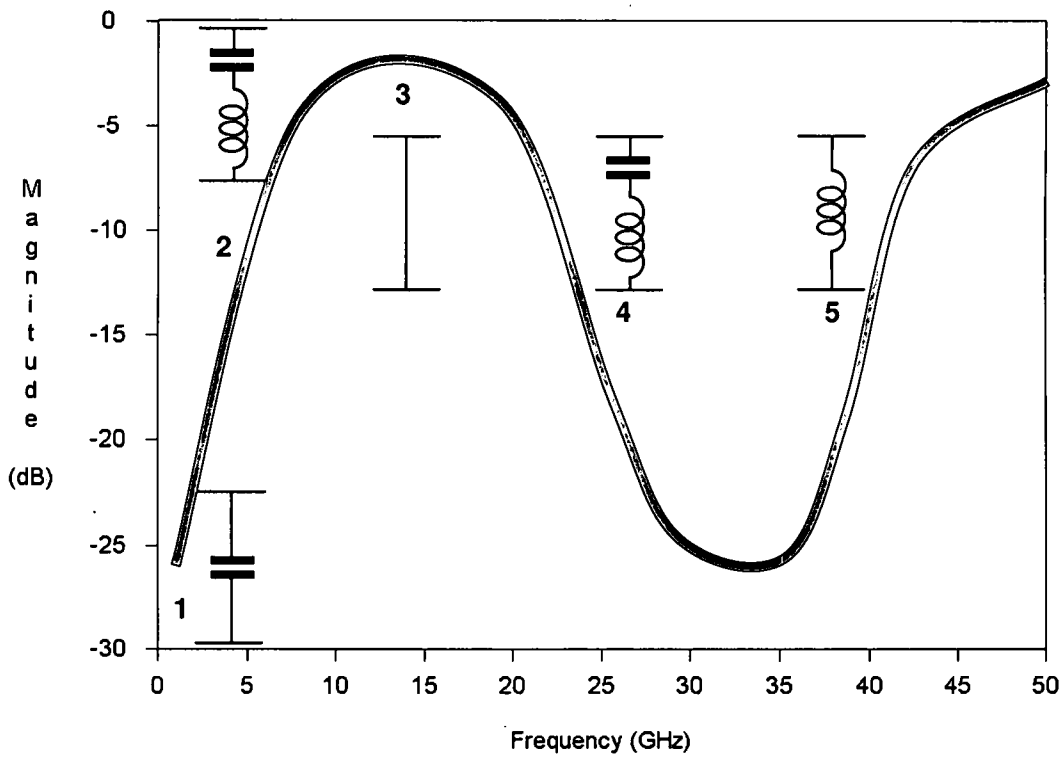


Figure 2-45: Generic S21 frequency response explanation

1. At dc and very low frequencies the capacitor appears as an open circuit or as a very high impedance element causing the transmission of the signal to be low.

$$Z = \frac{1}{j\omega C}$$

2. As the frequency increases, the impedance contribution of the capacitor decreases. Inductive impedance also appears which further reduces the overall impedance. The frequency response transitions from a stop band to a pass band.

$$Z = j\omega L + \frac{1}{j\omega C}$$

3. The structure begins to resonate as the capacitive and inductive impedances cancel each other and pass band performance is achieved.
$Z = 0$

4. Beyond resonance, the inductive contribution to the impedance begins to dominate. Capacitive impedance is still present; however, its contribution tends to decrease with increasing frequency and the response transitions to a stop band.

5. At higher frequencies the inductive effect increases further, but the capacitor appears more and more like a short. With increased parallel combinations of the inductors the overall inductance is decreased and the performance of the ground plane tends towards a traditional metallic sheet.

The original concept had accounted for region 1 thru 4. The pass band transition at the higher frequencies, although not originally expected, is understandable. The existence of the pass band and stop band regions gives confidence that a band gap exists in the simulation results and verifies the original concept.

2.7 Meander Line Design Mask Set

2.7.1 Microstrip Design

The device will be manufactured using standard lithography techniques. Masks will have to be created for each patterned layer. Although the design consists of a microstrip line with the HIGP as its ground plane, a network analyzer will be used to obtain the S-parameter response of the device using CPW probes. Contact with the HGP will me made from the top through the BCB layer using vias. Microstrip devices require specially tailored test structures because the ground plane is below the substrate, but CPW devices can be directly probed.

The meander line design with 10μm stub, 8 meanders, 25μm gap, and 15 cells has shown the best bandgap so far. Figure 2-46 shows the layout of the meander

design which other devices will use as a base. Figure 2-47 shows its frequency response with a clear pass band and rejection band. Before it can be manufactured for testing purposes, certain issues concerning the biasing scheme must be resolved. A bias network must be set up in order to take advantage of the tunable properties of BST. Had tunability and biasing not been a factor, this concept would have readily fallen into a typical FSS category, for which considerable work already exists.

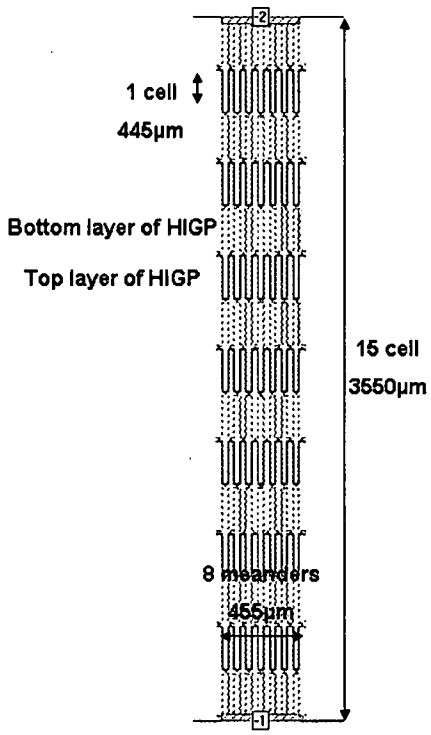


Figure 2-46: Meander design layout, 15 cell, 8 meanders, and 5x5 capacitors

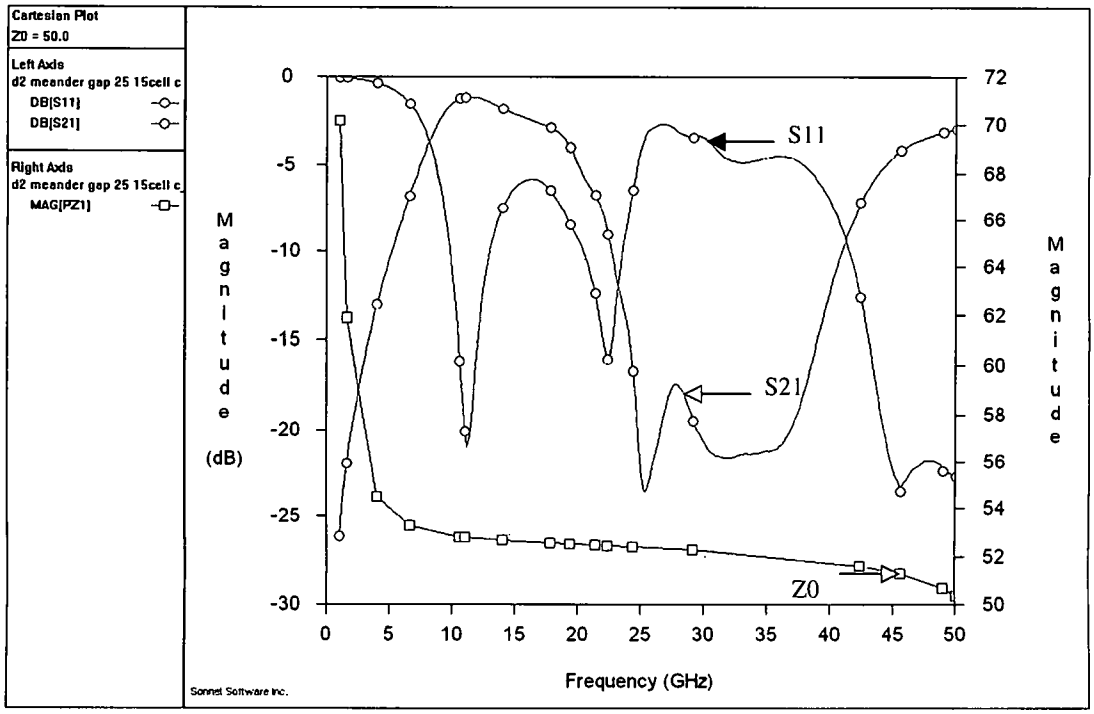


Figure 2-47: Meander design, S11 - S21 – Z0 simulation, 15 cell, 8 meanders, and 5x5 capacitors

Each varactor must have dc paths leading to it for both the top and the bottom plate of the capacitor. The meander lines provide a dc path to all the varactors formed at its overlap with neighboring meander lines in the other layer. This simplifies the problem somewhat, but still requires that a dc path exist for each meander. The top layer of the HIGP will be set to one dc voltage while the bottom layer will be set at a different voltage so that a voltage bias can exist between the two layers at the overlap regions. The dc voltage will be supplied by dc probes that are able to physically contact with the circuit so that the bias can be applied. These probes will make contact with a dc contact pad which will then connect to each meander line on that layer. To achieve this, the BCB layer must be etched away enough to expose the dc pads formed on top of the BST layer. To apply

bias to the bottom layer of the HIGP the BST layer would also have to be etched away. A technique around this is to form a dc pad above the BST layer and one directly below it forming a massive capacitor. Like all capacitors there is some parasitic shunt resistance which allows dc current to flow. In most cases the parasitic resistance is very large and very little dc current is able to flow. In the case of such a large capacitor, the dc resistance becomes very low due to parallel combinations, and the two pads are effectively shorted. This scheme allows the bottom layer of the HIGP to be biased without etching the BST layer, saving time and money.

The dc pads must be isolated from the ac signal for the device to work properly. The dc pads provide a low impedance path which would cause the signal to bypass the HIGP and flow through the dc pads. To avoid this situation RF chokes are constructed between the dc pads and the FSS meander lines. The RF chokes are low impedance at dc but appear as very high impedance to high frequency ac signals. Theoretically a large inductor should suffice as an RF choke. Other types of chokes which are of higher Q factor can possibly be employed, but as this work is concerned with broad band performance of the device rather than localized narrow band performance, a simple inductor was chosen. Figure 2-48 displays the layout of an FSS design and its bias network without RF chokes. The absence of these chokes severely alters the response of the HIGP. Figure 2-49 shows the S21 simulation response of the isolated meander design and compares it to the same design with a biasing network but without RF chokes. The response is significantly altered and a current analysis

using Sonnet showed that most of the current flowed through the dc pads rather than HIGP. At high frequencies the deviations in response are less because the energy remains close to the signal line, while at low frequencies the energy spreads out reaching the dc pads

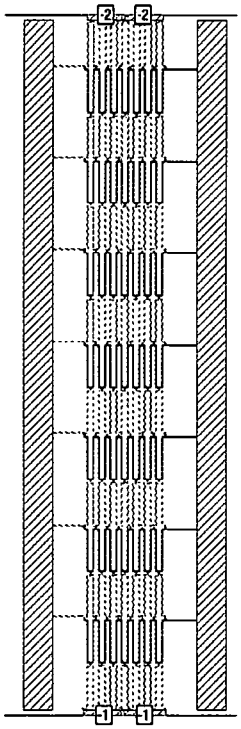


Figure 2-48: Microstrip FSS with dc pads and no RF chokes

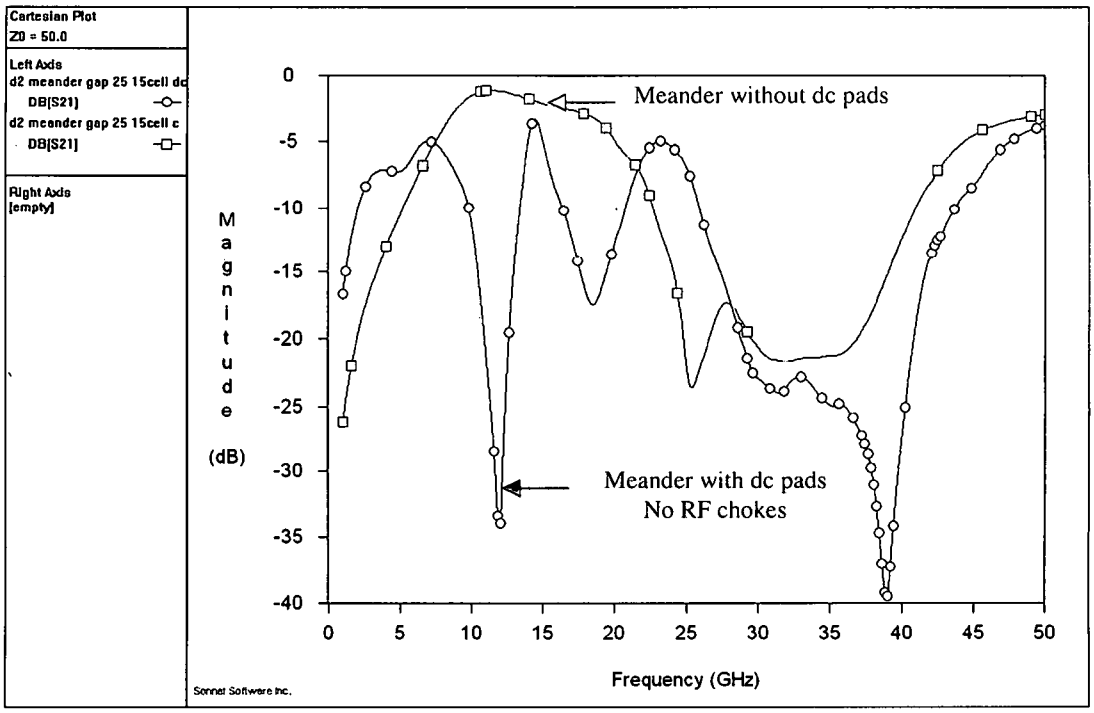


Figure 2-49: Meander design, S21 simulation, 15 cell design with and without dc pads and no RF chokes

The final design created for manufacturing is shown in Figure 2-50, which displays the HIGP. The RF chokes are made from 8 meanders 310μm long, with a gap width of 10μm and a line width of 5μm. The dc pads are 205μm wide and 3340μm long. The microstrip is placed above the HIGP with BCB in between. Figure 2-51 and Figure 2-52 give a more detailed view of the top and bottom layers of the HIGP.

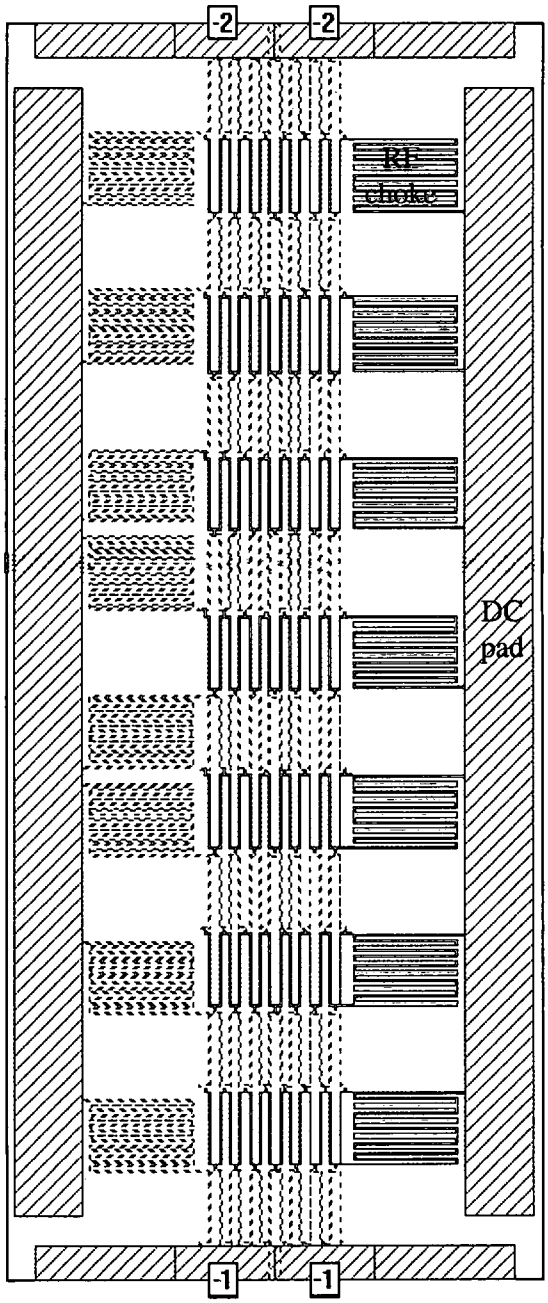


Figure 2-50: Microstrip HIGP based on meander design layout

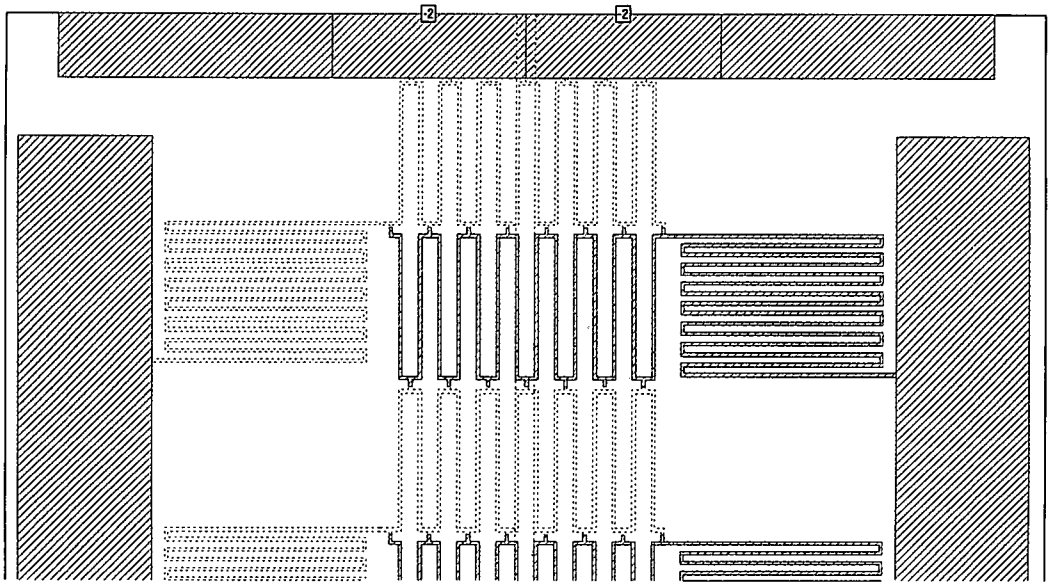


Figure 2-51: Top metal layer of ground plane

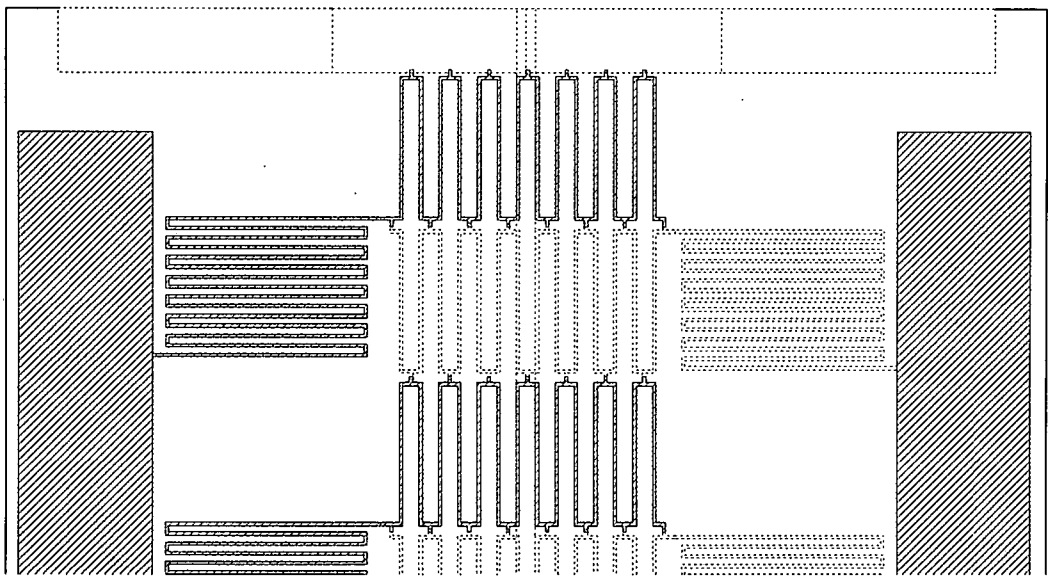


Figure 2-52: Bottom metal layer of ground plane

Figure 2-53 displays the S21 simulation results for the final microstrip design layout as shown in Figure 2-50. By tuning the BST from 200 down to 100 by the application of a bias, considerable change in the response is observed. Some

unexpected resonances are created; however, the main rejection band has been tuned from a center frequency of 30GHz, up to 45GHz, which is a significant level to tunability. Some deterioration in the pass band has occurred, primarily due to the bias network.

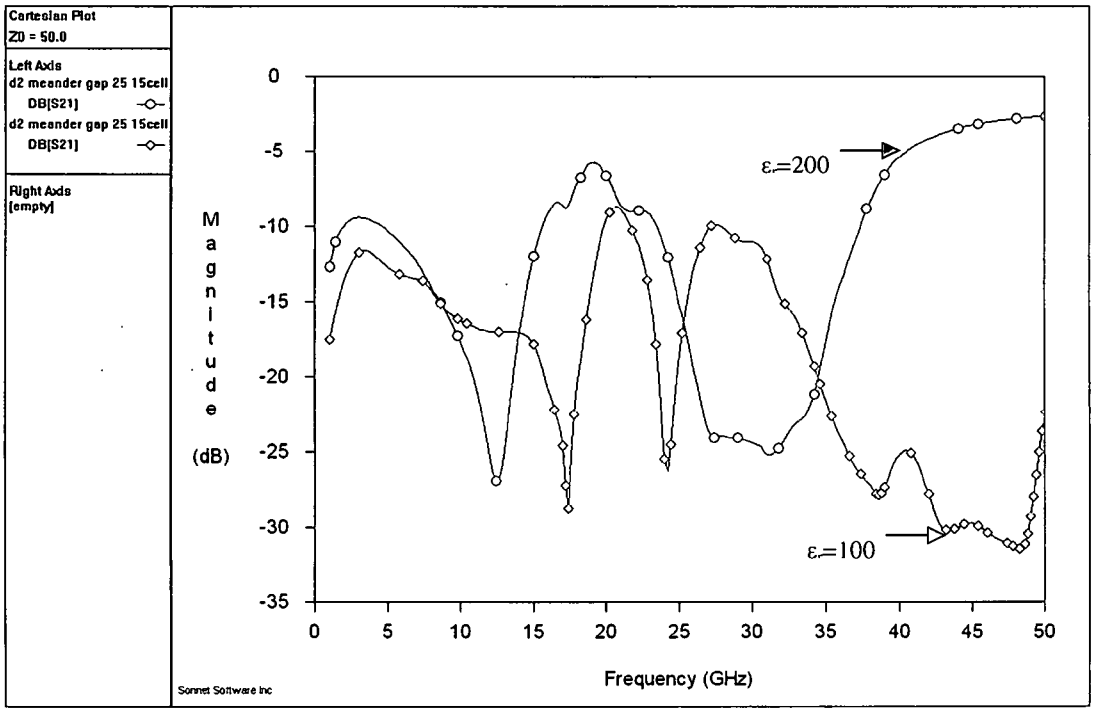


Figure 2-53: Final microstrip design, S21 simulation, with tuning

2.7.2 CPW Design

The work presented to this point was done at the Chalmers Institute of Technology, Sweden, under the auspices of Professor Spartak Gevorgian. The MC2 facility at Chalmers is able to manufacture complicated multi-layered devices. At the University of Dayton under Dr. Guru Subramanyam, the HIGP design had to be altered so that it could be manufactured at Air Force Research

Labs (AFRL) at Wright Patterson Air Force Base. The microstrip design required three metal layers, along with vias, and selective etching of the BCB. By splitting the FSS ground plane in half and placing it on the same relative layer as the signal line, a CPW structure is created which has much fewer manufacturing demands. The CPW structure has only two layers of patterned metal and no selective etching of the dielectrics is necessary. The dielectric properties of the BST films produced by AFRL are also different than those produced by Chalmers. Typical dielectric constants are 500 which can be tuned down to 150. The loss tangent of the film is 0.02 with a typical thickness of 300nm. As before, for simulation purposes the exact film parameters like dielectric constant, loss tangent, thickness, and tunability are not as important as the resulting shape of the response. These parameters are varied throughout the investigation of the CPW design and attempts are made to make them as close to the expected manufactured device parameter as possible.

Figure 2-54 shows the basic design for the CPW structure. The signal line width had to be adjusted to 65μm with a gap of 15μm between the signal line and the FSS ground plane/line in order to have a 50Ω design at the ports. The width of the FSS on each side is 185μm. From the knowledge gained from previous designs it is expected that even with good matching with the 50Ω port impedance there is considerable internal mismatch within the device which will result in internal reflections. The internal mismatch is caused because of the bias dependent dielectric properties of the BST layer, and the by the narrow inductive strips. Figure 2-55 displays the S21 simulation results for the CPW design with

the dielectric tuned from 500 to 350, and displays the same basic features as those shown by the microstrip design. Tunability is somewhat less than the microstrip design. The shift in the frequency band is due to the higher ε_r values used for the CPW design. Although without the presence of a bias network tunability is difficult to achieve, it is possible that electric field from a dc voltage applied to the signal line might produce some level of detectable tunability.

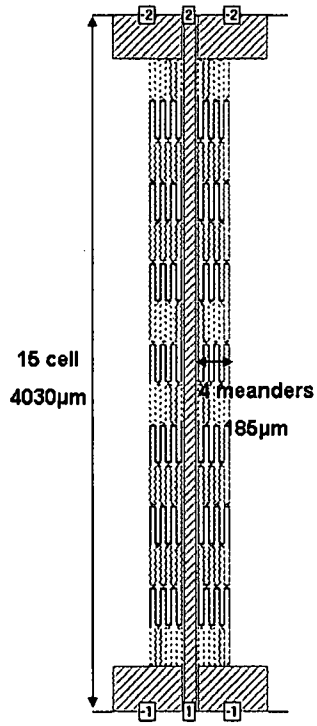


Figure 2-54: CPW Narrow FSS design

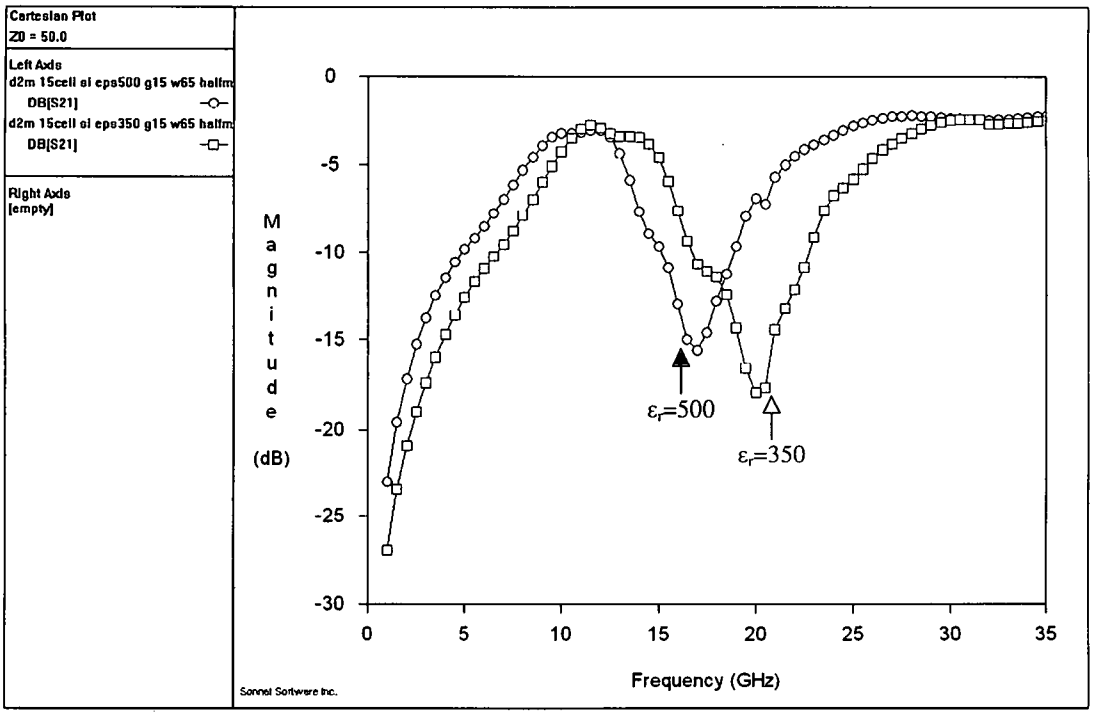


Figure 2-55: CPW Narrow FSS, S21 simulation, with dielectric tuning

Other designs were created for manufacturing but with the same basic CPW structure as the device shown in Figure 2-54. The purpose of the additional designs was to explore the effect of increasing the width of the FSS and variations of bias schemes. The layout shown in figure has a meander design which extends much further than the one shown in Figure 2-54. The main features are the same as those observed in the simulations of the narrow FSS, but an additional resonance is seen at 10GHz, and the overall level of rejection is reduced. It must be noted that this design is without a bias network. The narrow FSS constricts signal flow thus having a higher rejection while the wide FSS allows for better current flow and has less loss. The fact that the rejection band

still exists even with the wider ground plane shows that the meander design clearly has influence over the response of the circuit.

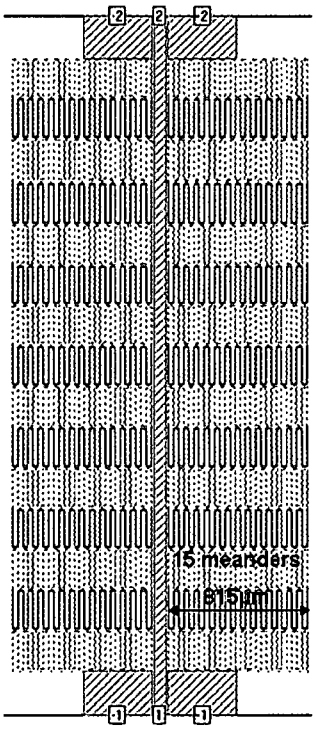


Figure 2-56: CPW Wide FSS, 15 meanders

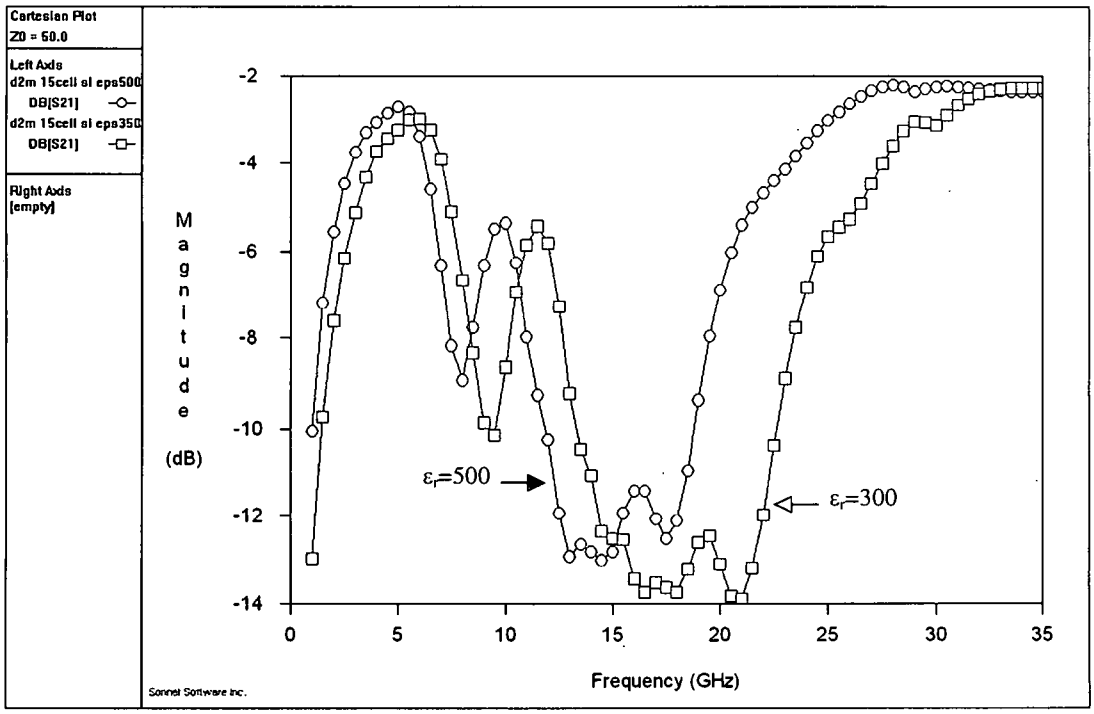


Figure 2-57: CPW Wide FSS, S21 simulations, 15 meander with tuning

Two additional designs are created based on the narrow FSS design, which are concerned with the biasing network. For these designs the RF chokes are made much larger than the ones used for the final microstrip HIGP design to improve the isolation of the dc pads. The chokes are made from 11 1000μm long meanders using gap width and line width of 5μm. The biasing network also grew in complexity for the CPW structure when compared to the microstrip design. The microstrip design could apply voltage to the meanders from one side for each layer; however, in the CPW design, bias must be applied from both sides because the FSS is split in two by the signal line in the center. Twice as many dc pads and RF chokes are required for the bias network of the CPW design. The dc paths at times overlap each other which can possibly compromise the

network. These overlaps had to be minimized in area as much as possible, but could not be avoided altogether.

The two schemes proposed for biasing the FSS are similar in design of the bias network but differ in the voltages used. One uses two non-zero dc voltages to bias the varactors (bi-polar bias technique, with a positive and a negative voltage), while the other attempts to use only one dc voltage and the bias is with respect to ground (Unipolar bias technique). Figure 2-58 shows the layout of the FSS design with two bias voltages. The Sonnet simulations of the design are shown in Figure 2-59, which display similar effects as those observed with the microstrip design with the bias network. The pass band has deteriorated slightly due to the poor isolation of the network at the lower frequencies.

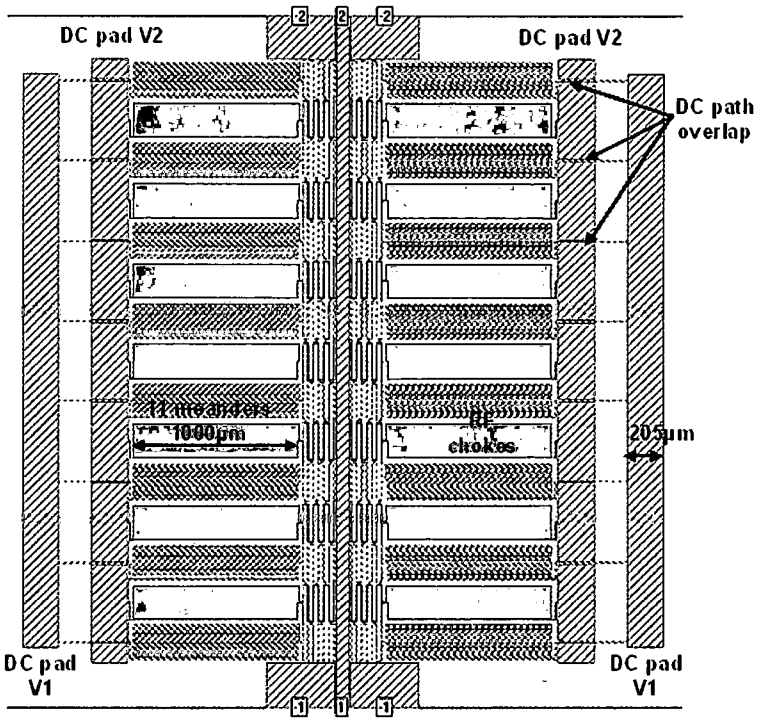


Figure 2-58: CPW FSS Bi-polar bias design layout

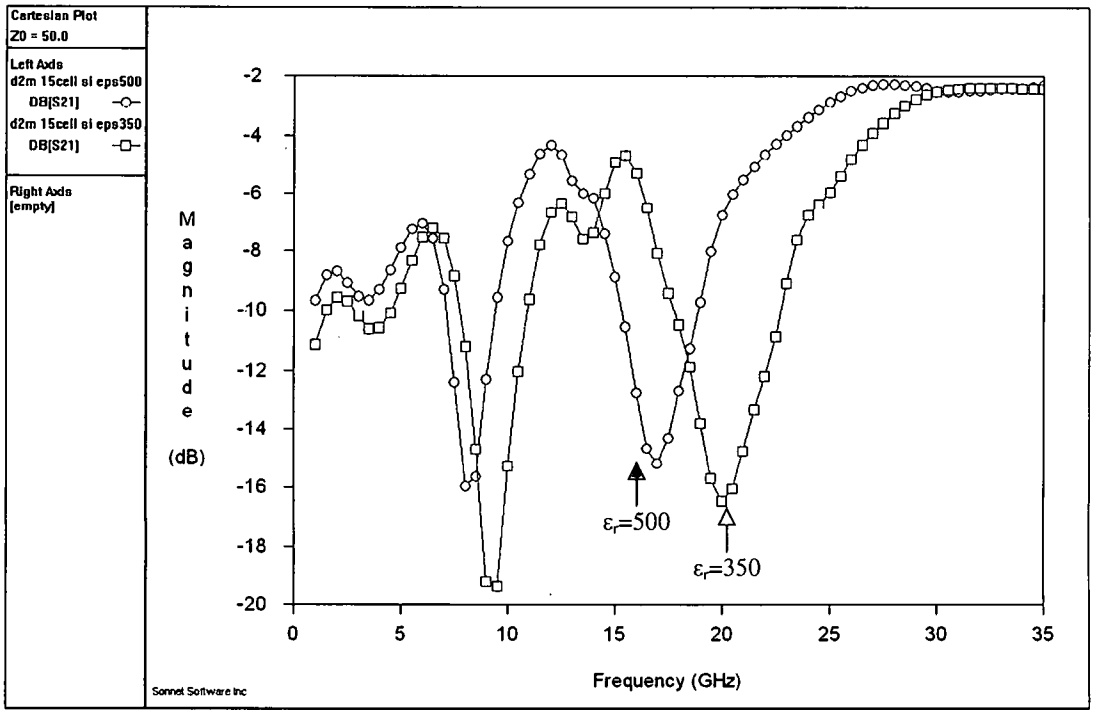


Figure 2-59: CPW FSS Bi-polar bias, S21 simulation, with dielectric tuning

Figure 2-60 shows the design layout of the second bias scheme which uses ground as one of the bias voltages. If this bias scheme is effective, only one external dc source will be needed. Figure 2-60 displays the Sonnet S21 simulation results for the layout, which shows considerable deviations from the results obtained for the other designs. The pass band is encroached upon by other resonances which make it very narrow. The rejection band has been stable throughout the design process. The bias network is clearly affecting the response of the device. Such problems must be taken into consideration when developing large systems with complex bias requirements. Sonnet's current density simulations of the designs provide some insight into the behavior of the devices but the results are not always easy to interpret.

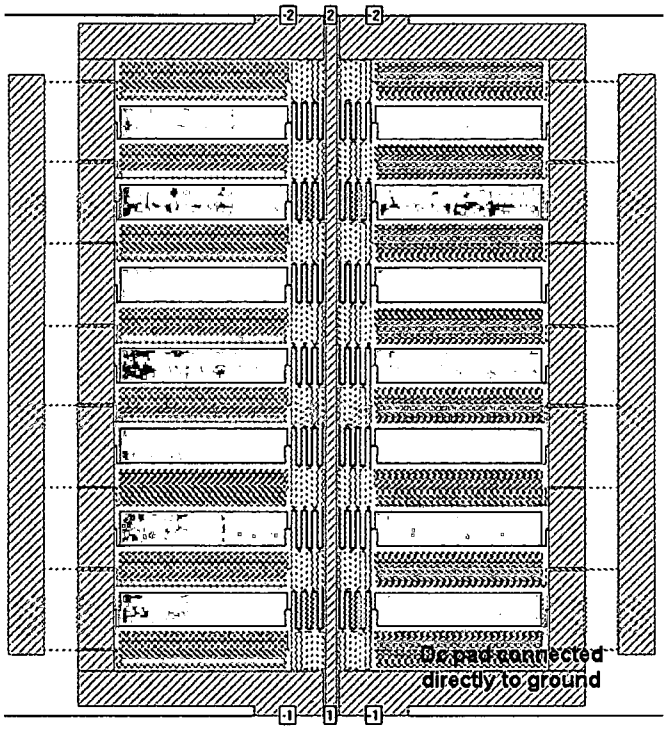


Figure 2-60: CPW FSS Uni-polar bias design layout

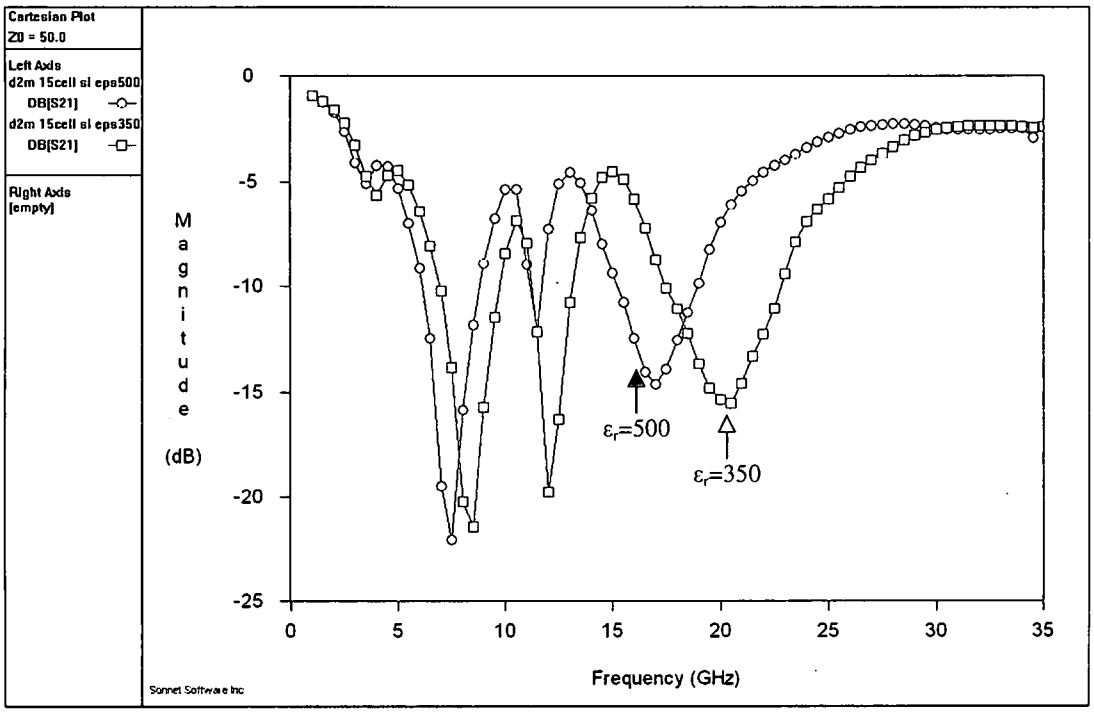


Figure 2-61: CPW FSS Uni-polar bias, S21 simulation, with dielectric tuning

Some final modifications were made to the design so that they are testable. Figure 2-62 shows an image of the bi-polar bias FSS with the additional dimensions of the bias network. All the large dc pad lines are 205μm wide. The connection between the large dc pad and the small dc probe contact is approximately λ/4 and is of length 200μm and width 10μm. Figure 2-63 shows the grounding pad where the actual CPW testing probes must be placed. The distance between the signal line and the ground lines must be able to accommodate the available probe pitch size. Probe pitch is the distance between the tips of the signal and ground contact points.

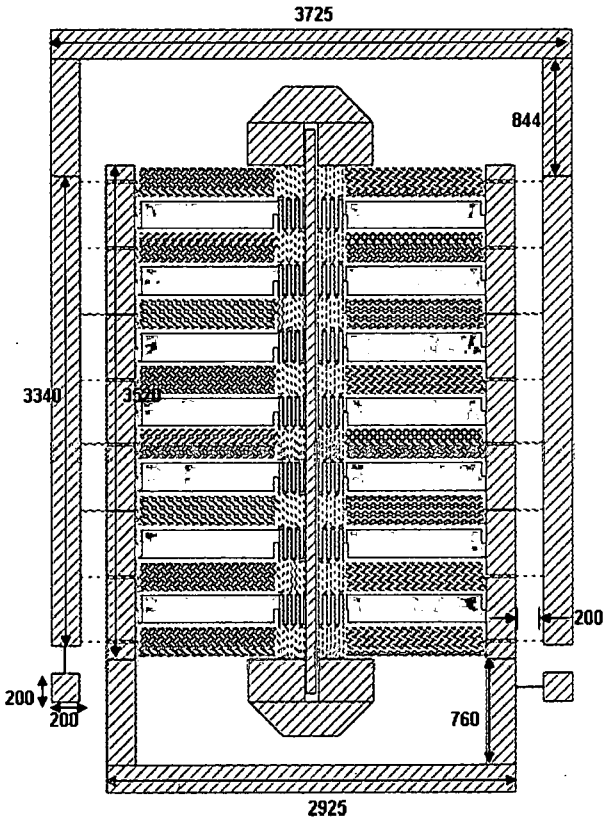


Figure 2-62: Bi-polar bias FSS with added dimensions in μm

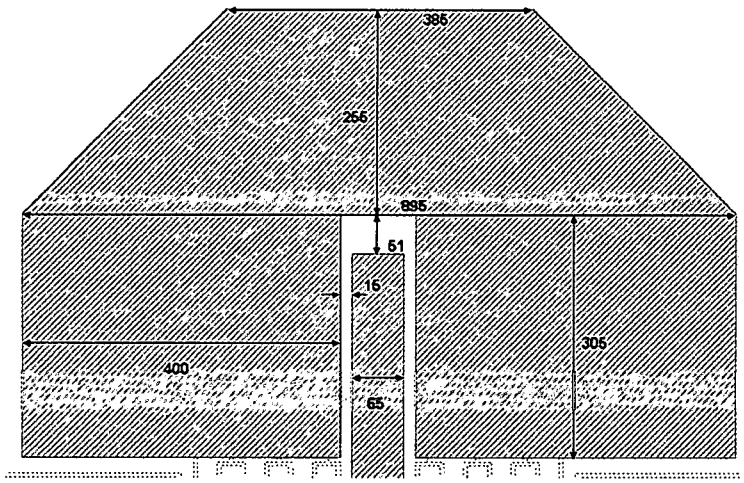


Figure 2-63: Probe contact area with dimensions in microns

2.8 FSS as Ground Plane

The simulations up till now demonstrate that although the structure has some amount of loss associated with it, there may be several beneficial properties of the surface. One property found specific to the meander based FSS is its anisotropic behavior. The response of the circuit is dependent on the orientation of the FSS below it. Depending on whether the microstrip is placed parallel, perpendicular, or at an angle to the meander lines, the simulated response changes. The other useful property is the tunability of the response of the HIGP. Devices which are traditionally not tunable can have a variable response by using the HIGP as the ground plane.

2.8.1 Anisotropic Behavior

The anisotropic property is demonstrated by changing the angle of placement of a microstrip line with a 1650μm by 1715μm section of FSS as shown in Figure 2-64. This particular dimension for the FSS was chosen because it was an

approximate square and because larger sections could not be simulated due to the excessive memory demands. Using the direction of the meander lines as the main axis, the angle of the microstrip with the meander lines θ, is simulated for 0º, 30º, 60º, and 90º. The ports connecting to the FSS move along the perimeter of the ground plane following the microstrip ends. The length of the microstrip line tends to be longer when θ is 30º and 60º than at the extremes of 0º and 90º. The 0º response is the one that has been seen throughout this work. The rejection is not as large because only 7 cells are used.

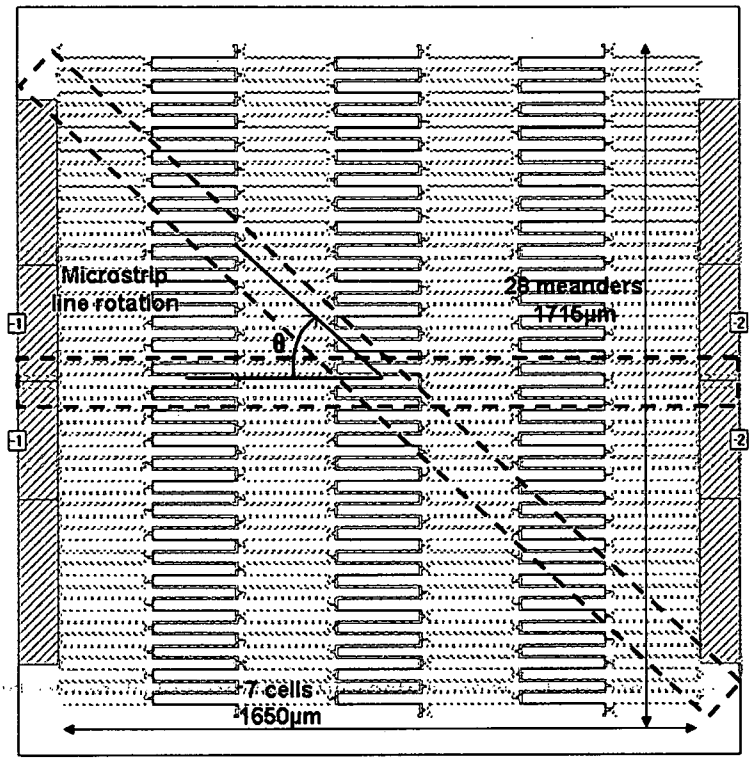


Figure 2-64: Microstrip design using square portion of HIGP

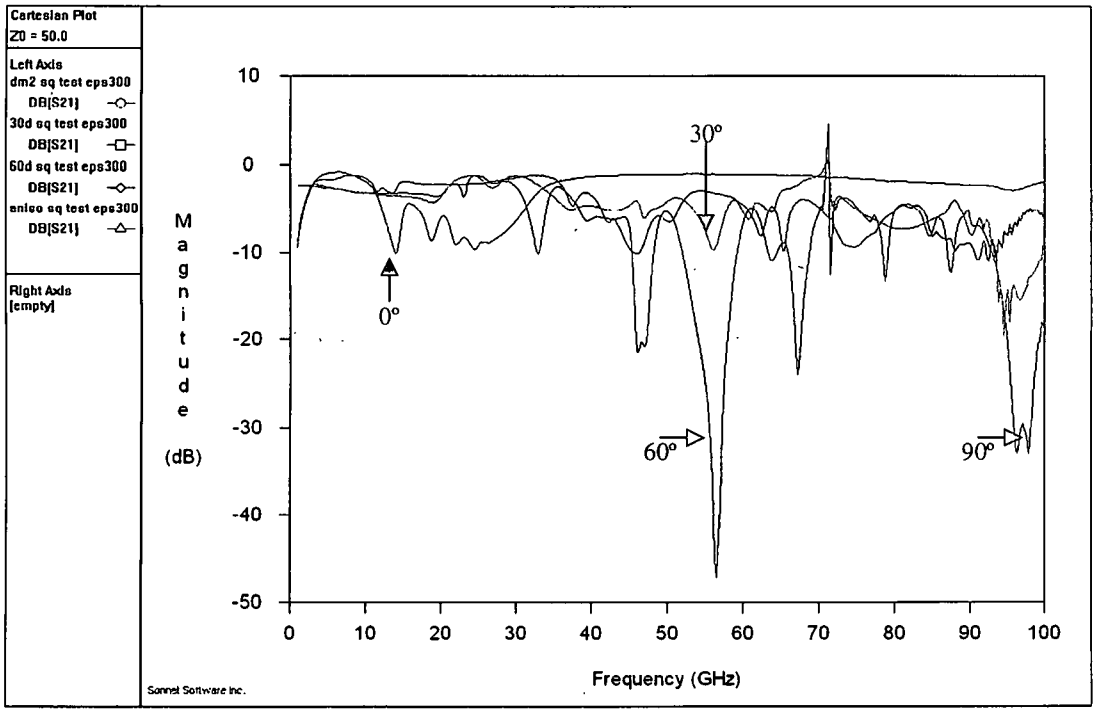


Figure 2-65: Microstrip design, S21 simulation, anisotropic behavior demonstration

The considerable variation in the responses with the change in θ clearly demonstrates the anisotropic behavior of the surface. Sonnet results beyond 50-60GHz are not as reliable as the results for low frequencies but the change in response is observed at all frequencies. The anisotropy may be a result of the one dimensional orientation of the meander lines. The presented surface was designed from a circuit point of view using lumped inductors and capacitors. From traditional FSS point of view, the dimensions of the repeated element are critical to the response of the system. In the case of the meander lines, the length is much greater than the width of the repeated element. It is possible that the asymmetry in the repeated element is the source of the anisotropic behavior. Similar arguments can be made using a circuit analysis method where the

inductance and capacitance values change due to orientation. The results presented are not sufficient to arrive at any particular solution other than that anisotropy exists and must be kept in mind when designing the repeated element. In radome application such anisotropic behavior could prove disastrous to the design; however, such properties are very useful when developing spatial filters.

2.8.2 Device Tunability

Using the tunability of the HIGP, the response of a device created on top of it can be varied. Due to the complex internal interactions of the HIGP, coupled with the anisotropic nature of the surface, predicting the exact response of device created on it can be very difficult. The feasibility of such a method is not fully explored but the effectiveness is demonstrated using a split-ring with the HIGP as the ground plane.

The behavior of a split ring is well understood and can be modeled readily using lengths of transmission lines. Depending on the size of the ring, a band gap appears due to the multiple reflections that occur within the structure. Due to constructive and destructive interference, the ring resonates and signal is reflected by the discontinuity in the ring. For simulation, a single-layer layout shown in Figure 2-3 is used except that the meander based HIGP is expanded to accommodate the ring. Based on the ring dimensions shown in Figure 2-66, the resonance frequency is 42GHz for a ring using a traditional ground plane placed below the BST layer.

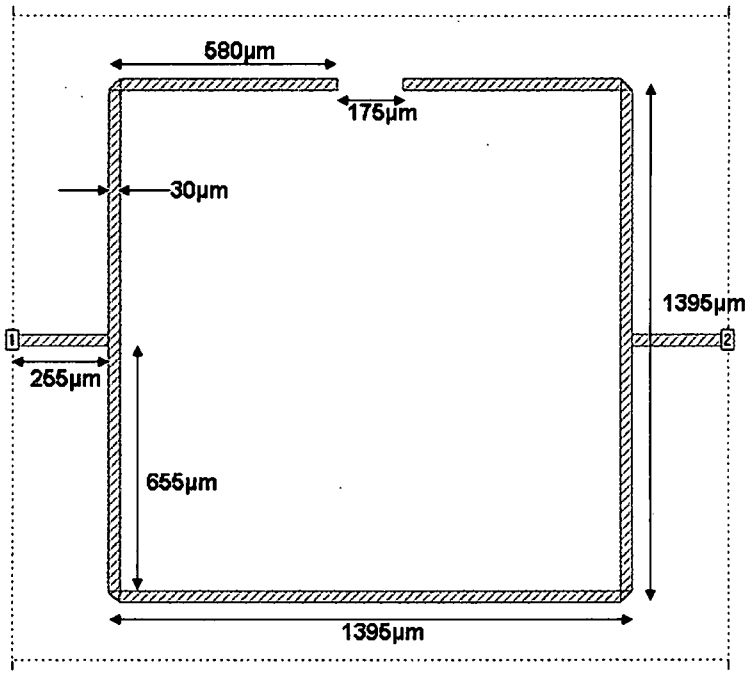


Figure 2-66: Split ring on traditional ground plane

Figure 2-67 displays the effect of replacing the metallic sheet with the HIGP with the BST having a dielectric constant of 500. For simplicity the bias network is not included. The presence of the HIGP does alter the response of the device but the main resonance, though shifted in frequency, is clearly identifiable.

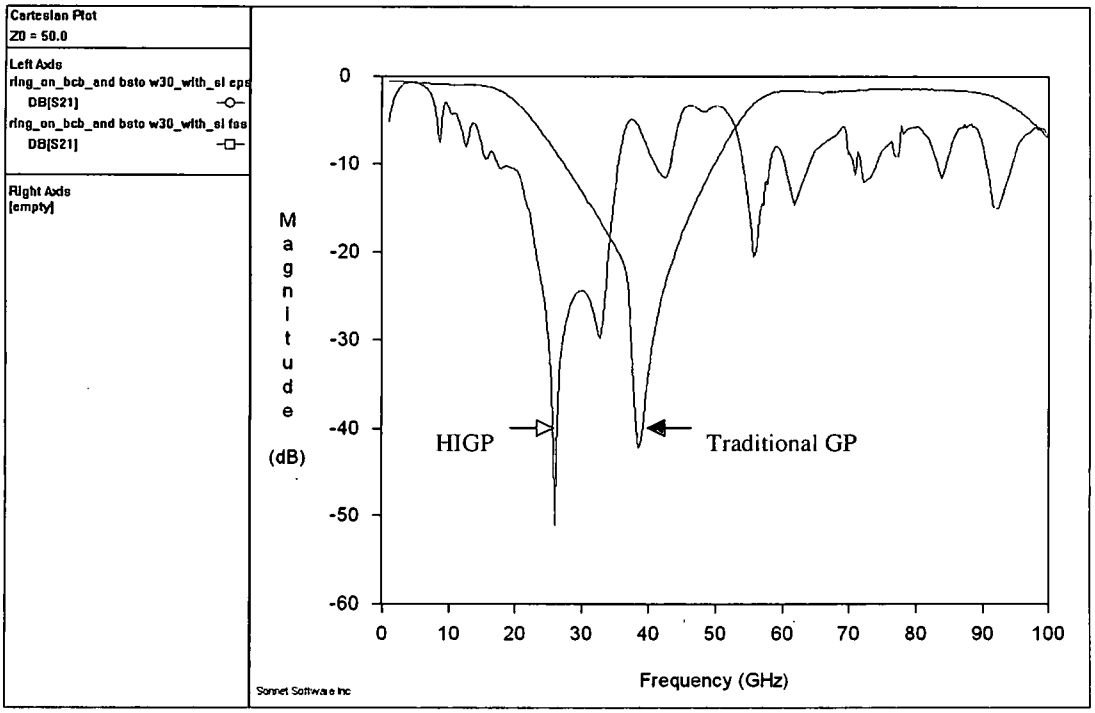


Figure 2-67: Split ring on traditional ground plane and HIGP

For demonstrative purposes the dielectric constant is tuned even though a bias network is not being simulated. A very interesting response is found in the phase change of S21 when the dielectric constant is tuned from 500 to 200. Figure 2-68 shows the S21 magnitude and unwrapped phase response for the ring circuit on the HIGP. A very large phase change is observed in the phase response. Phase change per dB is often used as a figure of merit for comparing device performance. Figure 2-69 shows the worst case transmission loss at ε_r of 500 and 200, and the resulting phase difference in the S21 response. At low frequencies the observed phase change is minimal, but it radically increases within the band gap before stabilizing after exiting the band gap. By dividing the phase change by the worst case loss, a maximum of 252º/dB is achieved at 49GHz as shown by Figure 2-70. When a traditional ground plane is used

instead, very little phase difference is obtained. Although this may be a numerical anomaly and the results may not be physically realizable, it does show that the HIGP can not only introduce tunability into designs, but can also enhance performance in certain aspects. The results presented are for un-optimized design observed over a large frequency range. Theoretically, performance can be further improved by application specific optimization over a narrow frequency band.

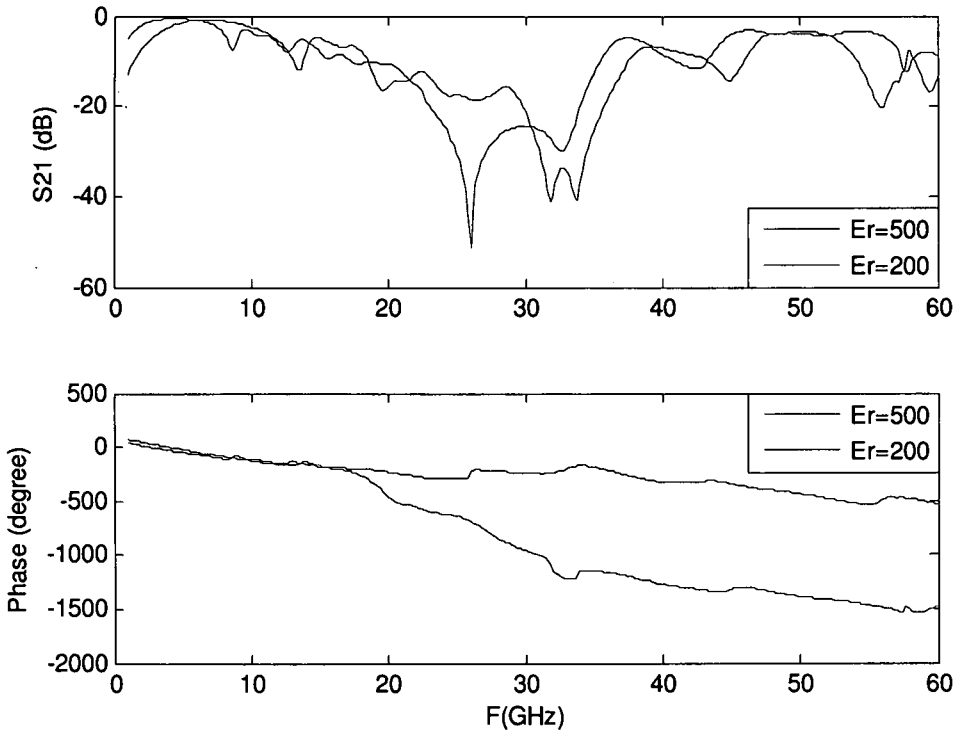


Figure 2-68: Ring on HIGP S21 simulation response

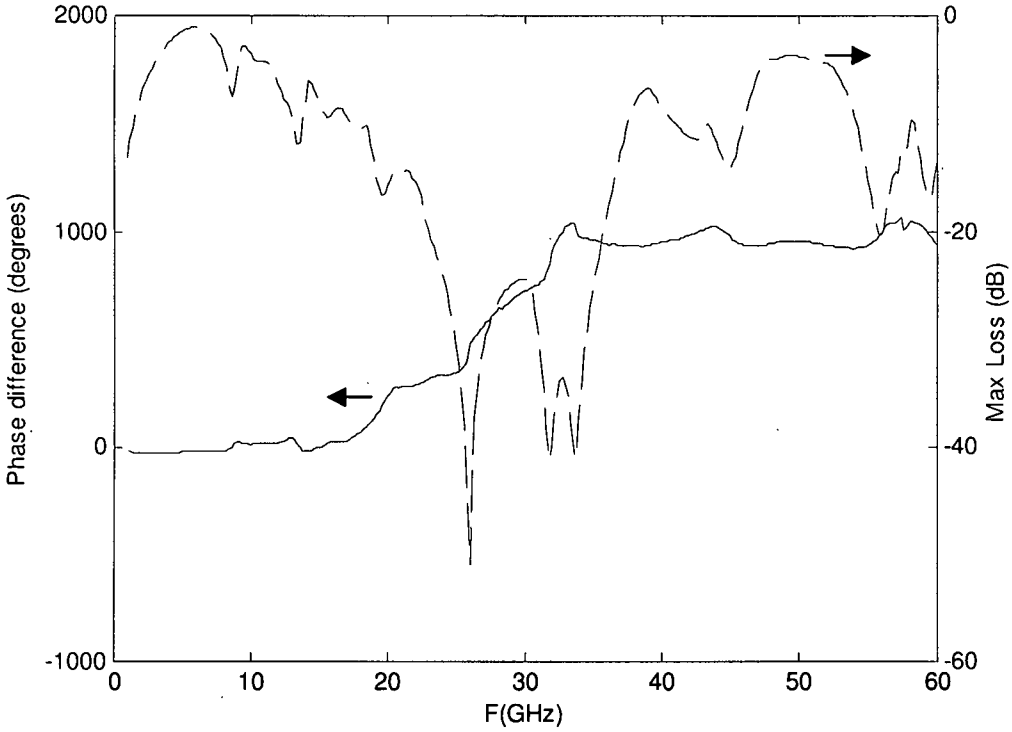


Figure 2-69: Ring on HIGP, Max transmission loss and phase difference

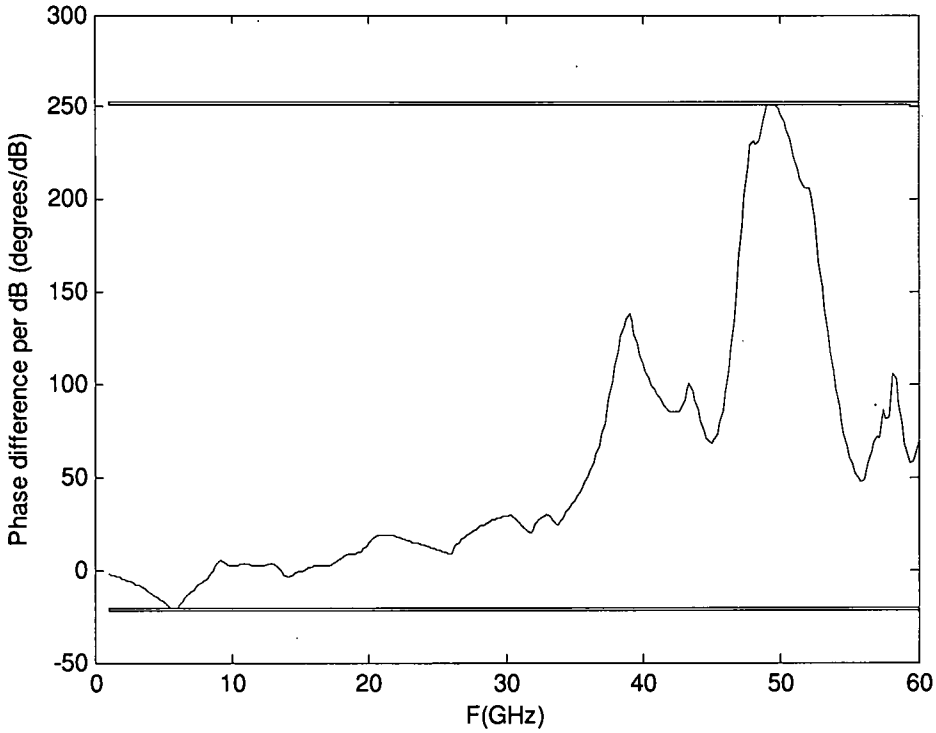


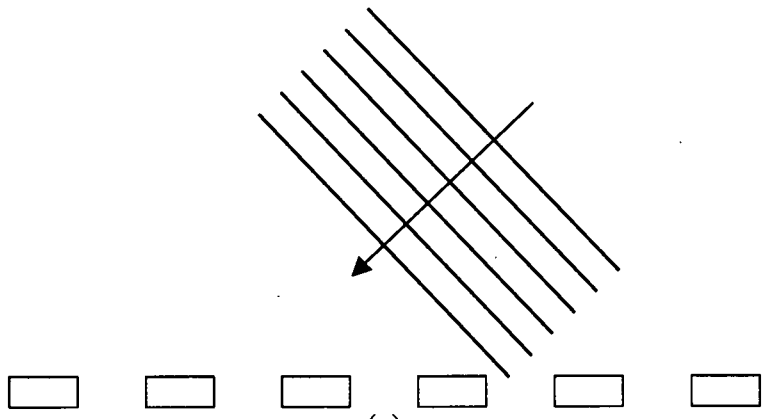
Figure 2-70: Ring on HIGP, S21 phase change per dB

2.9 Analysis and Discussions

With the presentation of the results question may arise about the justification of the entire design approach and how each design is analyzed. As stated earlier, this study is a preliminary venture into the area of large two dimensional tunable band gap structures. Work done on meta-materials, FSS and HIGP exists, but none follows the path taken in this study. The approach uses basic microwave circuit design techniques and attempts to expand the circuit through periodic repetition into a planar surface. The use of periodic elements on surface may relate the design closest to an FSS, but a very thorough analysis needs to be done before and FSS design approach can be effectively applied. At the commencement of this work the only knowledge available was the dielectric tunability of BST thin-films in smaller microwave circuits. There were no clear expectations about how a more complex structure would behave. Now that some insight has been gained in the workings of the device, it may be possible to revisit the problem and attempt to analyze it using an FSS approach.

HFSS by Ansoft is used as the industry standard for FSS design because of its ability to analyze the FSS element and to determine the performance of the repeated structure. Sonnet was chosen as the analysis software for this work for two reasons, one that past experiences have proved Sonnet to be a reliable tool for finite element analysis of multi-layered waveguide structures, and two that the capabilities of Sonnet worked well with the design, manufacturing, and testing capabilities of the research group. From a design perspective the group had much more experience in the development of microwave devices using MMIC

technology rather than a typical FSS. Manufacturing constraints are placed on the substrates that can be employed due to the high temperatures involved in the deposition and growth of BST thin-films. The testing apparatus needed for experimenting with an FSS tends to be more complex than the simple probing structure used in the study. As presented earlier, horn antennas are needed along with focusing lenses in order to avoid excessive diffraction that occurs due to the wide beam generated by the antennas. To circumvent these complexities, the FSS structure was approximated with a microstrip structure, which was then approximated with a CPW design. Although there are many assumptions involved, it is believed that the response of the FSS structure will resemble in some way or manner the response of the traveling-wave CPW design. The three excitation methods are shown in Figure 2-71. It is believed that the multiple resonances observed in the wave guide structures will disappear when plane waves are used for exciting the surface. The absence of the extraneous resonance may revert the system back to a form closer to its initial inception with a single pass band at resonance.



(a)

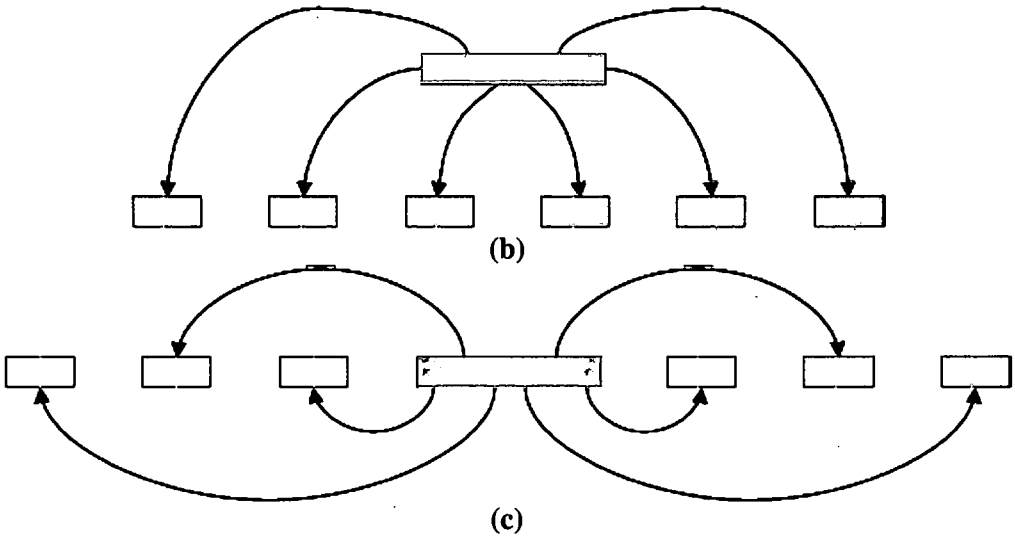


Figure 2-71: Three methods for exciting the surface, (*a*) plane waves, (*b*) microstrip line, (*c*) CPW line

The purpose of the work was to explore whether the use of BST material in a large planar surface has potential for two-dimensional surfaces such as the FSS or the HIGP. The results presented show that the proposed surface can greatly influence device performance. As this was a preliminary study into two dimensional structures using BST for tunability, it showed the difficulty of obtaining a representative unit cell, the existence of multiple resonance and multi-signal paths, and the complexities associated with the development of an effective biasing network. All these issues are neither resolved nor are they fully understood, but this work will serve as source for future designers to keep these problems under consideration.

Chapter 3 Results

The simulations presented use parameters based on expected values for the manufactured design such as the film thickness, dielectric constant, and loss tangent. The four designs chosen for manufacturing were created on two wafers with different methods of BST deposition on each wafer. The four designs of CPW structure are the narrow FSS, wide FSS, FSS with bi-polar bias, and FSS with uni-polar bias, as shown in Figure 3-1.

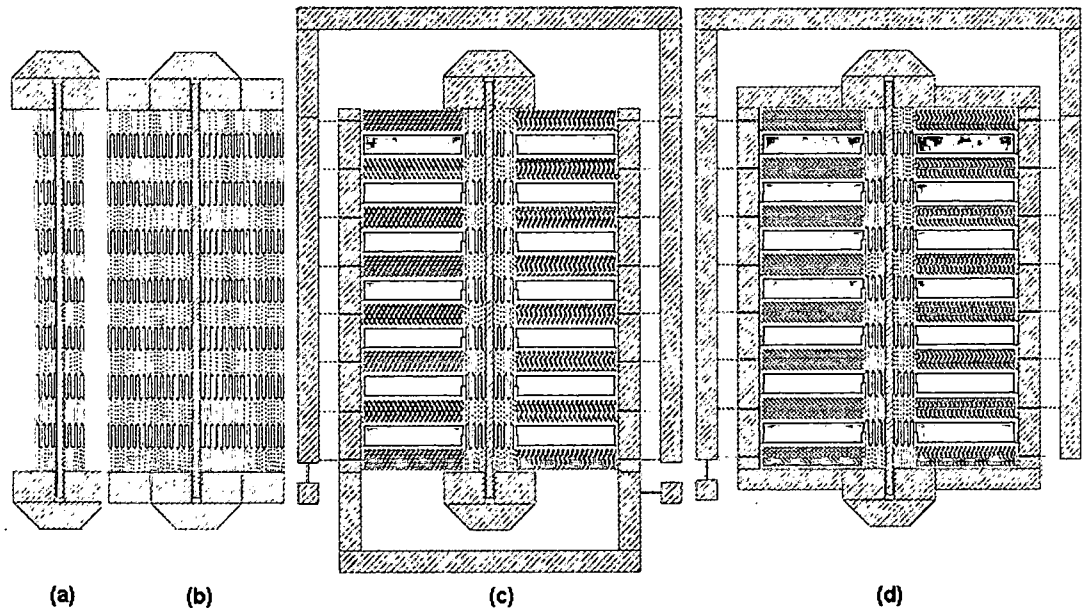


Figure 3-1: Manufactured design layouts, (*a*) Narrow FSS, (*b*) Wide FSS, (*c*) Bi-polar bias FSS, (*d*) Uni-polar bias FSS

One device sample had a 200nm sputtered BST film with an approximate dielectric constant of 250 and a loss tangent of 0.1. The parameters of the

sputtered film are different than those originally simulated. During the processing there was noticeable damage to the top metal layer and there was a slight misalignment between the metal layers. Another sample used 300nm BST film deposited using PLD method. An inexplicable error occurred during the liftoff process of the second metal layer which was not properly patterned. Some of the devices could be salvaged; however, the quality of the conductors could not be guaranteed. Test structures for measuring film parameters were also lost during processing therefore only estimates of the dielectric constant and loss tangent are available based on the processing conditions of the BST film. It is estimated that the dielectric constant is near 500 while a cruder estimate of the loss tangent lies between 0.1, to 0.25.

Two of the devices from the sputtered sample were measured at AFRL, which provided a much higher frequency range of measurement. The measurement setup available at the University of Dayton has a few limitations concerning the accuracy and the frequency range of measurements. The maximum analyzable frequency of the network analyzer is 20GHz. As the bandgap lies beyond this frequency range it is expected that only the pass band and the transition to the bandgap will be observed from the readings taken at UD. Another limitation is concerned with the calibration of the equipment. Calibration procedures could only include the cables connecting the network analyzer to the probe station. The probes themselves could not be included in the calibration because on-wafer calibration kit was not available. The measurements at UD are non-deembedded as calibration can be done only at the connectors to the probe station. Although

the probes are expected to be low loss and should have only a minor influence over the results, it is possible that the added inductance may cause some shifts in the observed features. The data measured at UD for the sputtered film have been smoothed out by a two sample moving average so that the trend is better viewable.

Due to the limitations in film quality and the available measurement equipment, a one-to-one comparison between simulation results and experimental results is not possible; however, as the main concern of the work is the existence of the features rather than their specific performance levels, the setup will serve for the current purpose.

3.1 Narrow FSS

The narrow FSS is the simplest of the four designs. Sonnet simulations were done to incorporate the parameters of the sputtered film. Simulation results predict a nicely formed pass-band and rejection band. Using the AFRL testing equipment it was possible to observe the expected feature; yet the design proved to be quite lossy and the features occurred much higher in frequency. This may be due to the misalignment present between the metal layers of the sputtered sample. The rejection band is unmistakably identifiable, although the excessive losses were not expected. Testing of the same sample done at UD could not reproduce the exact results as those obtained by AFRL, but as S21 data in Figure 3-2 shows, they are clearly comparable. The deviations may be a result of the differences in testing equipment, and may also be caused by the exposure of

the film to the elements. The results from UD for the sputtered sample tended to be quite noisy and only the trend line of the data points is shown. AFRL testing results for the PLD sample are also displayed and show the same trend as those observed from the sputtered sample. The losses are slightly less in the PLD case which may be attributed to the larger varactor size and possibly higher film quality. As the exact parameters for the PLD film are not known, a comparative Sonnet simulation could not be made. The lossy pass band can be seen as well as the transition into the rejection band. The rejection band of the PLD sample is comparable in depth and width to that generated by the sputtered sample. The level of transmission is expected to increase beyond 45GHz. The S11 results in Figure 3-3 show that all measurement data follow the same trend and corroborate well with the simulation results. There is a definite high mismatch in the device which is causing high levels of internal reflection resulting in the increased loss. The fact that the S11 curves do not fully reciprocate the S21 curves shows that the bandgap features are not directly a result of mismatch, but that there is a definite change in the observed impedance.

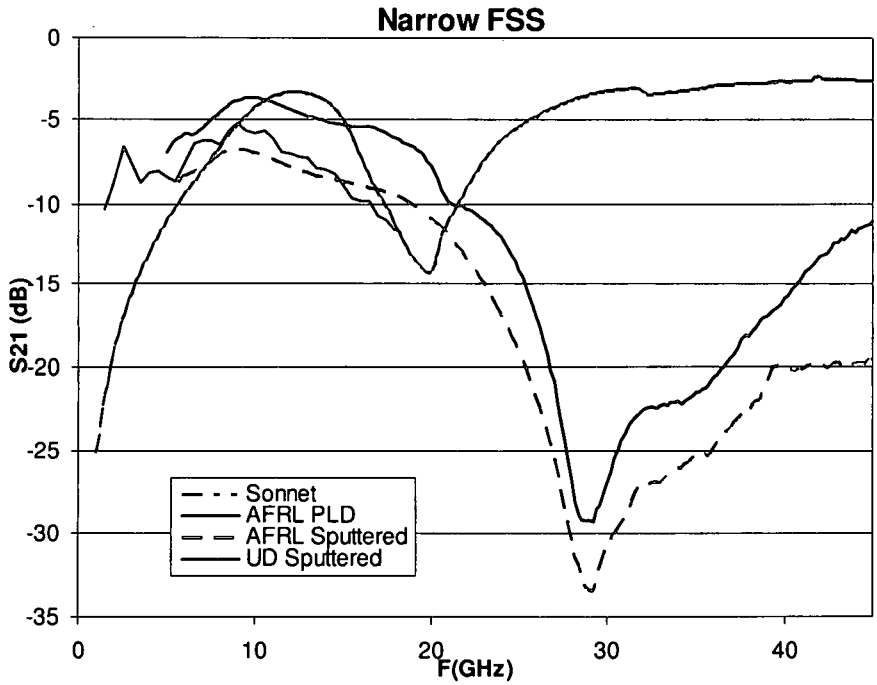


Figure 3-2: Narrow FSS S21 results

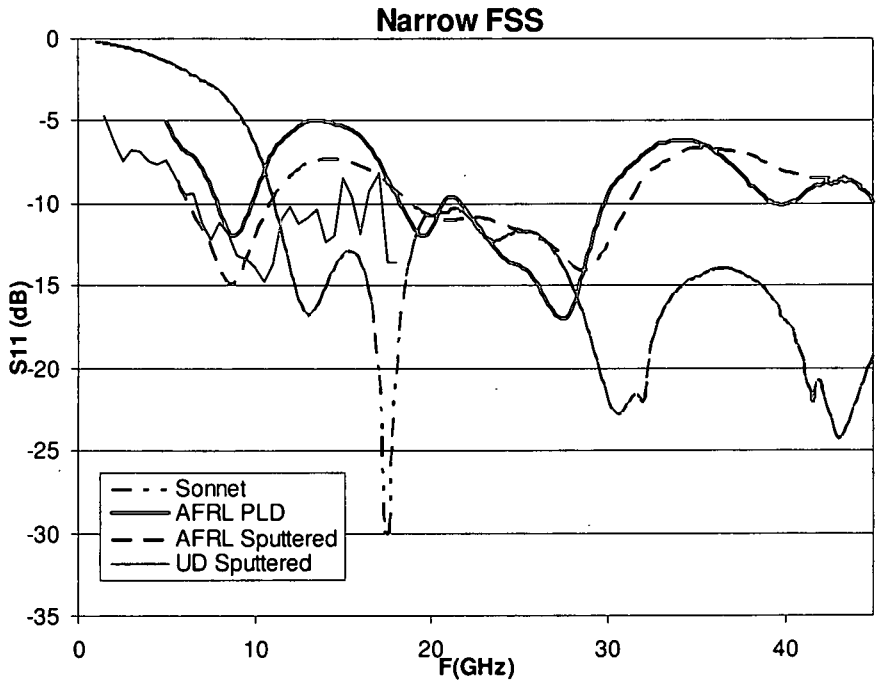


Figure 3-3: Narrow FSS S11 results

3.2 Wide FSS

The available data for the wide FSS design is very limited. Testing for this design was not done at AFRL, and due to the lift-off problems on the PLD sample the device could not be recovered. Only one set of measurements is available from the sputtered sample, which is compared to the Sonnet simulations in Figure 3-4 and Figure 3-5. The lossy pass-band can be seen and the expected bandgap appears to be much deeper than predicted by the simulation results. In general the results produced using the testing equipment available at UD are noisy and lossier than those generated by the AFRL facility. Keeping this in mind it is probable that had the wide FSS sample been measured at AFRL the result would be better.

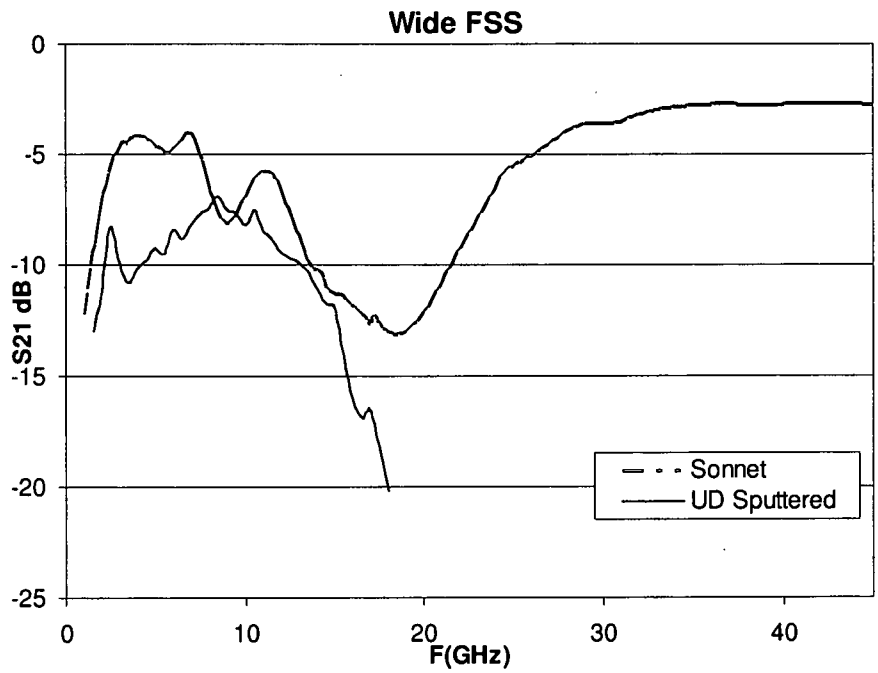


Figure 3-4: Wide FSS S21 results

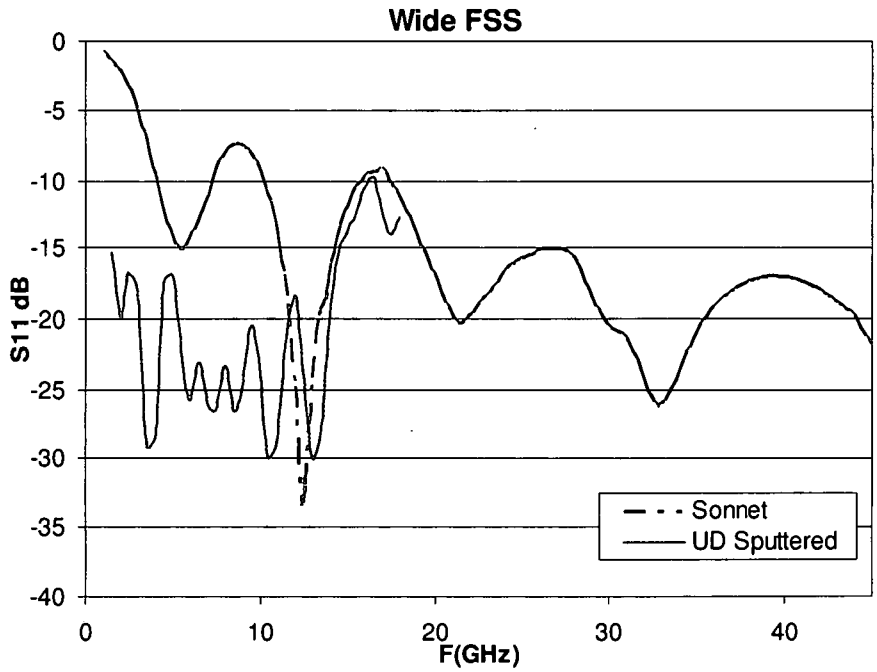


Figure 3-5: Wide FSS S11 results

3.3 Uni-polar Bias FSS

The uni-polar bias FSS suffered from the same circumstances as the wide FSS design. Only limited testing data could be gathered from the samples that survived and wide frequency results were not available as shown in Figure 3-6 and Figure 3-7. In this particular case the simulation results predicted a large deviation from the normal response of the FSS due to the biasing arrangement. This deviation is also observed in the experimental data. The deep rejection calculated by the Sonnet simulations may be a result of the resonance of the dc pads, which apparently does not occur in the realized circuit.

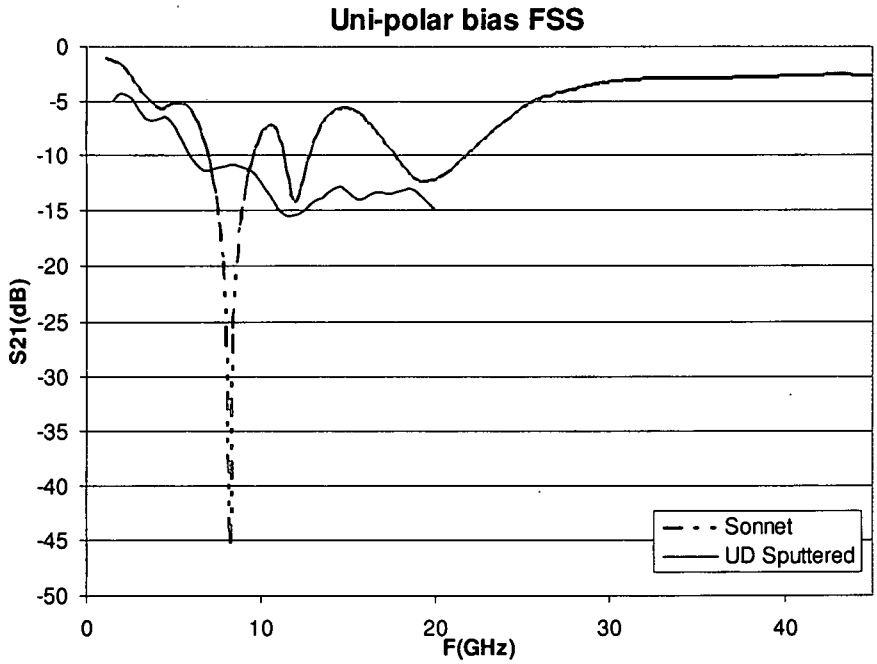


Figure 3-6: Uni-polar bias FSS S21 results

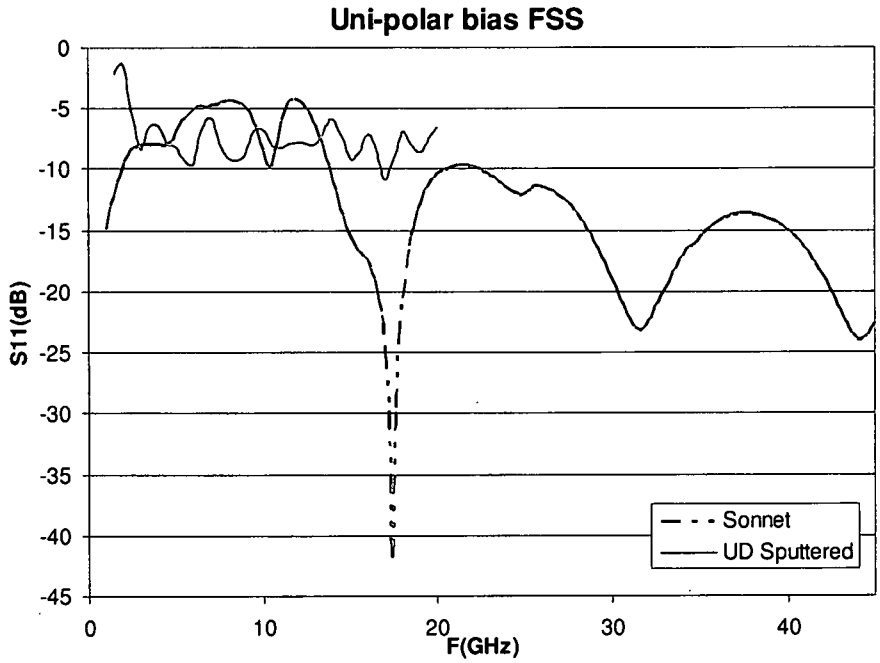


Figure 3-7: Uni-polar bias FSS S11 results

3.4 Bi-polar Bias FSS

Extensive data was available for the bi-polar bias FSS structure. Data from AFRL testing of the sputtered and PLD samples provide a clear picture of the bandgap as shown in Figure 3-8. There is a strong correlation between the simulated results and the AFRL results even though there is an observed frequency shift and greater loss in the experimental data. As in the case of the narrow FSS, the results obtained by AFRL could not be fully reproduced by the measurement setup at UD. The testing results for the PLD sample also shows a bandgap although it is not as deep or as wide as that shown by the sputtered sample. The higher dielectric constant of the PLD sample has pushed the bandgap lower in frequency and the results closely resemble the Sonnet simulation results. The level of loss in the pass-band is comparable to the loss observed in the narrow FSS design at frequencies below 5GHz. Between 5 to 20GHz the bi-polar bias design tends to be lossier than the narrow FSS design. Beyond 20 GHz the performance levels are comparable except that the bi-polar bias FSS shows a wider bandgap than the narrow FSS design. The results indicate that the bias network has influence over the FSS but it may by limited to a frequency range. The S11 results in Figure 3-9 show that the sputtered sample had much better matching than that predicted by Sonnet for the lower frequencies. The PLD sample however has very poor yet stable matching.

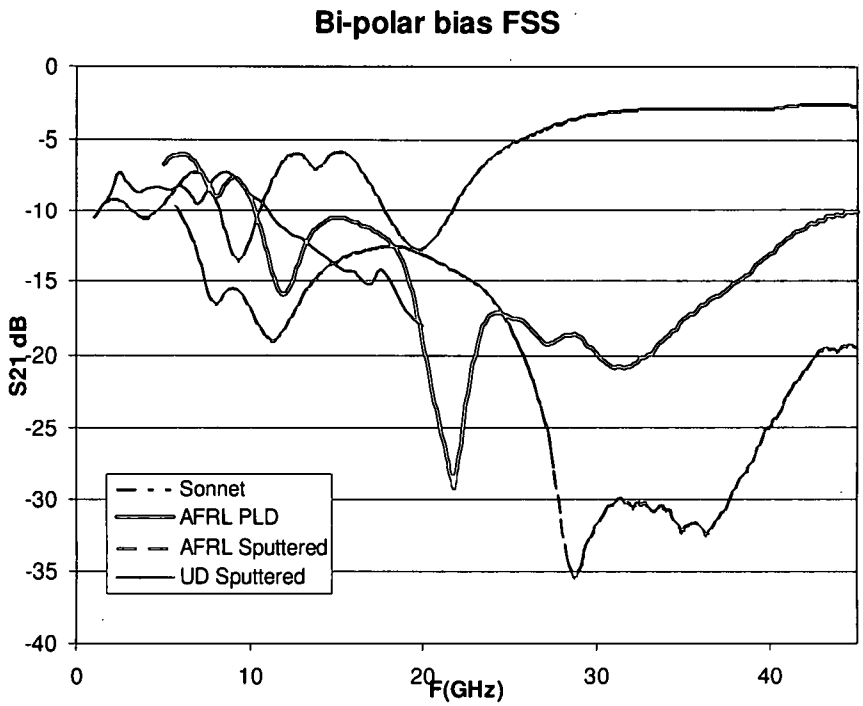


Figure 3-8: Bi-polar bias FSS S21 results

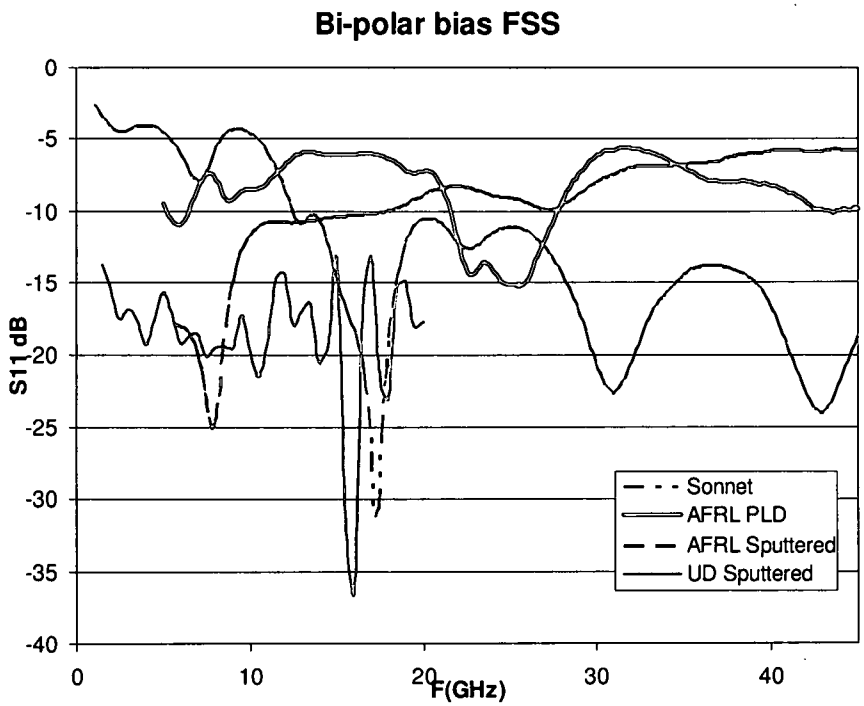


Figure 3-9: Bi-polar bias FSS S11 results

3.5 Result comparison

The Sonnet simulation results for the design that were manufactured are shown in Figure 3-10 for an ε_r of 500. The S21 results show a clear bandgap in the region between 15 and 20GHz. For the lower frequencies the responses vary but are still comparable for the most part.

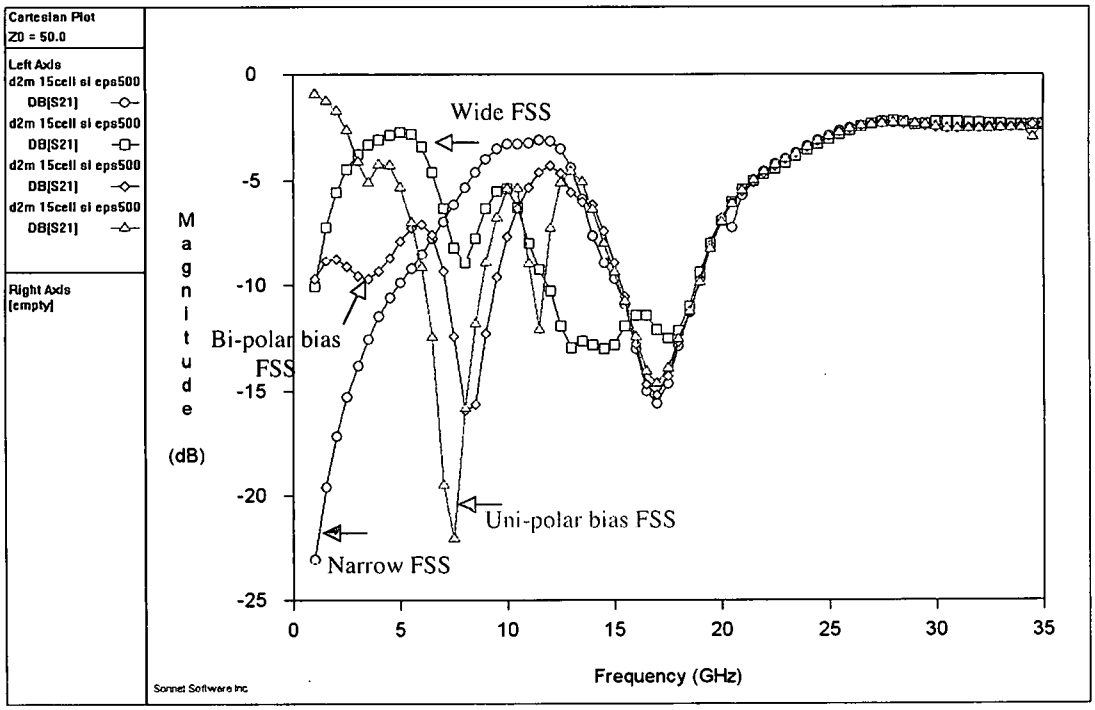


Figure 3-10: Sonnet S21 simulation results for manufactured designs with ε_r=500

From the testing results obtained from AFRL for the sputtered sample, the bandgap can be clearly observed in Figure 3-11. Although the losses are significantly greater than predicted by simulations, the results do verify the existence of the various features such as a lower band-pass, a rejection band, and a high-pass, as calculated by the simulations. The losses may be attributed to poorer than expected conductor and film quality.

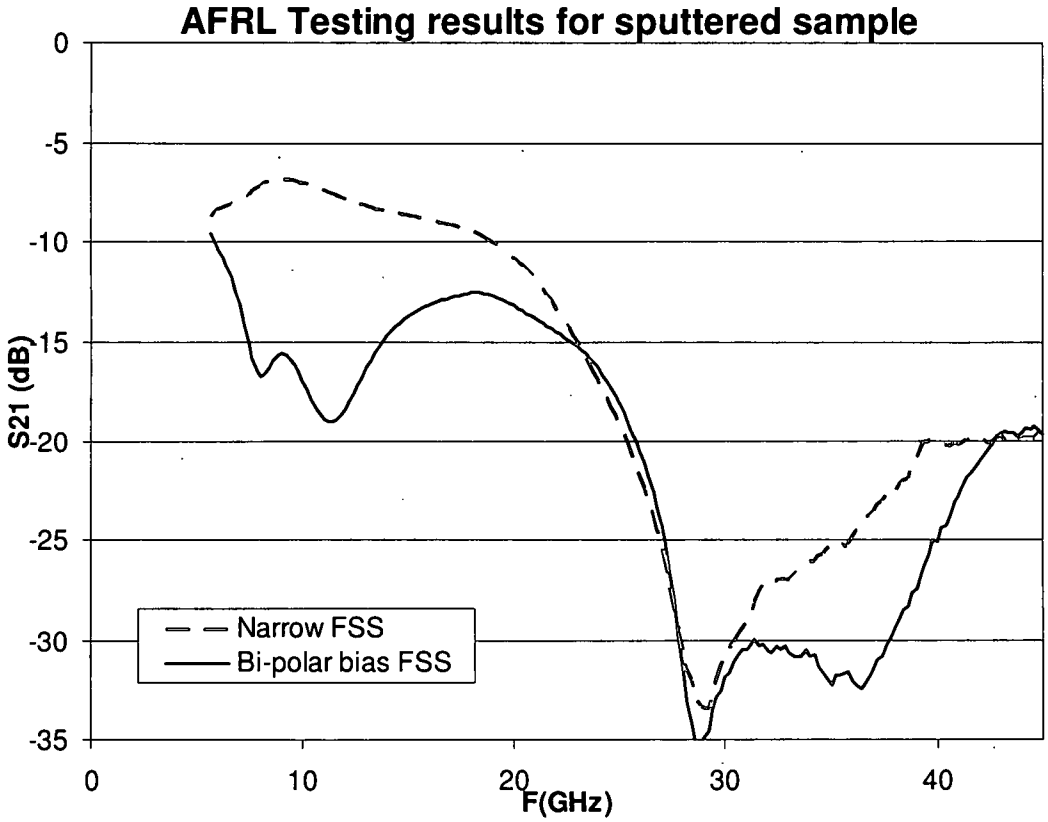


Figure 3-11: S21 testing results from AFRL for Narrow FSS and Bi-polar bias FSS on sputtered sample

The results obtained from the testing equipment at UD, shown in Figure 3-12, suggest a similar trend in the behavior of the manufactured designs. The behavior of the uni-polar bias FSS is an exception to the general performance of the FSS, as was predicted by Sonnet simulations. The wide FSS is lossier than the narrow FSS. This may be because the wide FSS designs were located at the edge of the wafer where the quality of the film could be poorer.

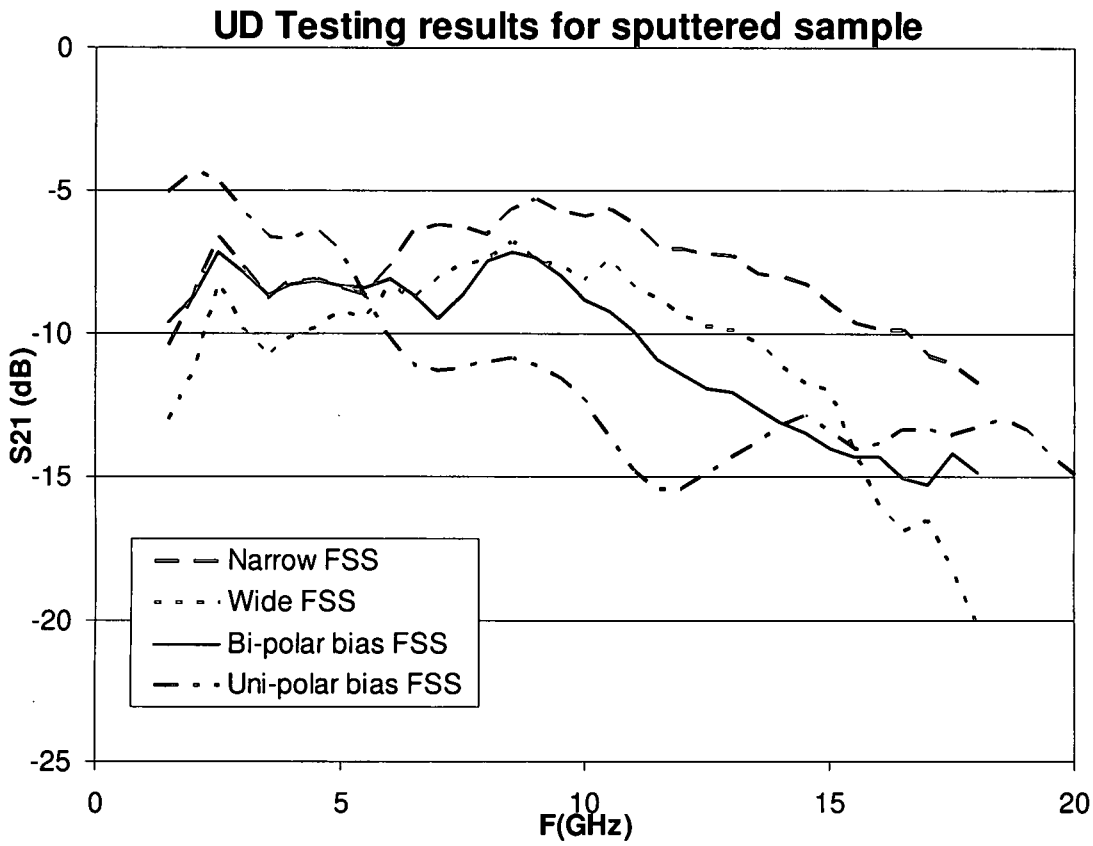
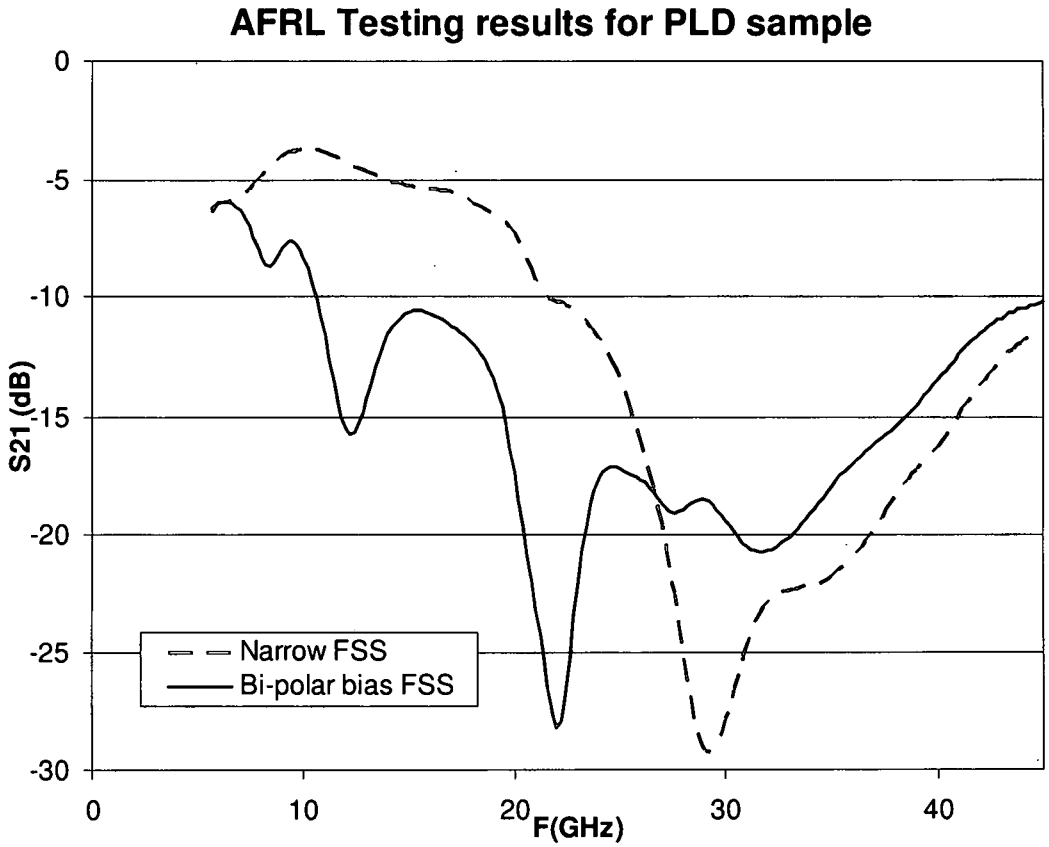


Figure 3-12: S21 testing results from UD for manufactured designs on sputtered sample

The testing results for the PLD sample as obtained through the AFRL facility show similar behavior as that for the sputtered sample. In general the narrow FSS performance is less disturbed below the bandgap while as the bi-polar FSS curves are interrupted by resonances below the bandgap. Although the device design for the two sample is identical, difference introduced by not only the film, but the metal quality could explain the deviations in the results.



The results in general allow for certain conclusions. The meander line design appears to be inherently lossy and is very sensitive to film quality. The bias network employed in the designs presented effects the device response by introducing added loss. The results identify a definite bandgap however the results are in general lossier than expected. The results can be improved by selective etching of unnecessary BST which is a source of additional dielectric loss. The experimental data presented is from devices suffering from some problems during processing, which may have been responsible for the deviations in the results but the main features are retained.

Chapter 4 Conclusions

4.1 Summary

The goal of the study was to realize a tunable bandgap structure using BST material in the form of a two-dimensional surface. The work shows that the problem is quite difficult and the interactions within the structure are complex. As this was the first venture into the area, the primary goal was to develop a band gap, while good performance levels were of secondary importance. Both simulation and experimental results show a clearly marked bandgap. The high impedance behavior of the surface is only available within a certain bandwidth. At higher frequencies the surfaces behaves like a traditional ground plane but with added losses.

In this study several designs are explored, all of which stem from the same concept, hence the behaviors of the designs are related to each other. The designs allow for biasing, and provide overlap regions for BST varactors. Using the meander and parallel strip designs, investigation of the effects of the number of strips, their spacing, and the number of series cells were done through Sonnet simulations. Although no definite conclusions are available, certain observation about the behavior of the surface can be made. The number of strips and their spacing directly contribute to the device performance. The cells in series tend to

behave like cascaded filters with increased rejection and ultimate deterioration of the pass band.

Biasing schemes are explored so that the device performance can be electronically tuned. Large dc pads are created so that dc voltage can reach the varactors. RF chokes are used to isolate the device from the biasing network which would otherwise provide a low impedance path for the microwave signal. The presence of the biasing network introduces additional losses. The research conducted sheds light on the various factors that must be considered when designing such a complicated structure. The work should serve as a stepping stone for future endeavors in the area.

4.2 Future Works

The next logical step in the research would be to have a bias setup for supplying dc voltages to the designs with the bias network. The parasitic resistance in the BST varactors is predicted to be higher than 1kΩ; however, with so many varactors in parallel, the effective resistance may become too small and high dc currents may flow through the FSS. Network analyzers usually have a 1mA limit for dc current flow before they are unable to make measurements. The amount of bias that can be applied and the level of response tunability are questions that can only be answered once the biasing apparatus is available.

With the knowledge gained from the current study concerning the various parameters that influence the performance of the FSS/HIGP, the problem can be

revisited to be understood from a more analytical point of view. Using the extensive work already done on FSS design, it may be possible to design and analyze the device using available techniques. Optimization of the meander design can be further attempted by reducing the bandwidth of the device. By reducing the bandwidth it may be possible to get much better performance levels, such as improved transmission in the pass-band and better rejection in the stop-band. The rectangular unit cell of the meander design can be made such that it is closer to a square. Having a symmetric repeated element may remove the anisotropic behavior which would be advantageous for certain applications where greater stability of the response with respect to the angle of incidence of the plane wave is required. The designs presented can be further analyzed by using reference planes to observe what happens within the device beyond the ports. Improving matching within the device may significantly improve performance. As the quality of the BST thin-film is a critical parameter in the design, higher quality films with less loss are required. Selective etching of BST so that it only exists in the varactor region has been proven to reduce losses due to the film [115].

While using the same technique as that used in this study, it may be possible to generate designs that are simpler or more complex in nature. Figure 4-1 shows a much simpler design that may be investigated, while Figure 4-2 shows a much more complex structure. The common trait between both designs is that they can be biased using a bias network along the edges of the surface, and varactors are formed where metal layers overlap. Investigation of such design may further improve understanding of the device behavior. Experiments in the development

of biasing networks are also needed. A resistive biasing grid would reduce the flow of dc current [116], while inductive elements would isolate the FSS from the dc network.

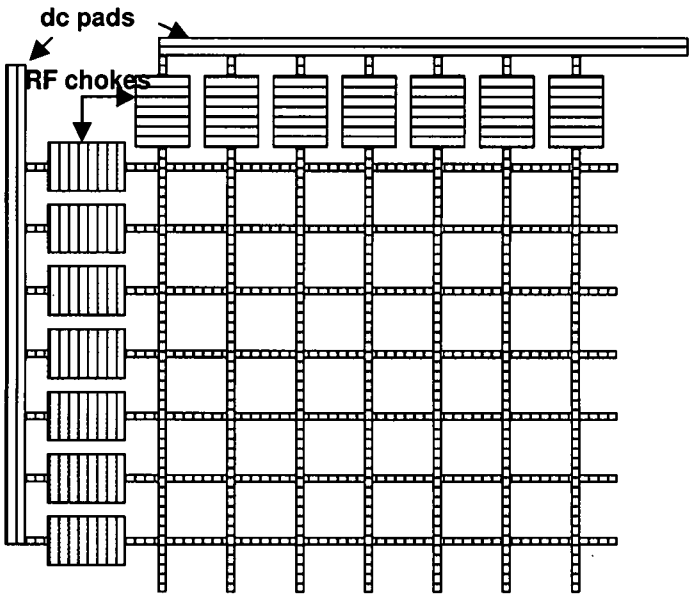


Figure 4-1: Simple inductor overlap design

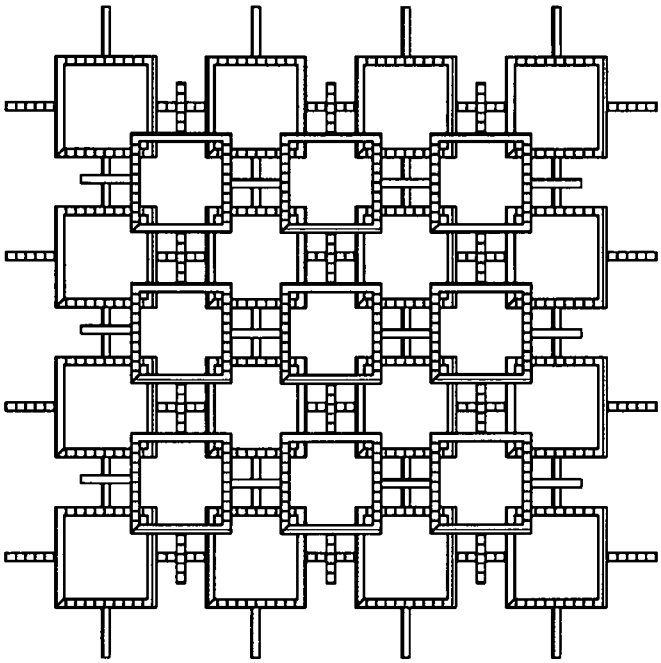


Figure 4-2: Complex resonator design

For further developments of a true FSS it may be necessary to use lower dielectric substrates instead of silicon in order to reduce the amount of loss. The choice of substrate is limited because of the high temperature demands placed due to BST film processing. It may be possible to manufacture the FSS and then ultimately etch away most of the lossy substrate. For simulation purposes, advanced software tailored for FSS design are needed along with algorithms for optimization. A complex testing scheme involving horn antennas and focusing lenses is required to obtain accurate experimental data.

This study has not yet verified if the proposed surface can be used as an artificial magnetic conductor. Although a bandgap exists, further testing is needed to understand if the surfaces it is truly a magnetic ground plane within the bandgap. Using an anechoic chamber it is possible to setup a transmitting and receiving antenna. The sample surface is placed at one end of the chamber while the transmitting horn antenna directs electromagnetic energy at the test sample. The receiving antenna is placed at the same end as the transmitting antenna and detects the reflected signal. If no phase change is observed in the reflected signal then the surface is behaving like a magnetic ground plane. A traditional metallic ground plane would have introduced a 180° phase shift in the reflected signal.

More work is definitely needed in the area for the development of viable surfaces with interesting properties. Using BST to introduce tunability will add another performance aspect to a traditional periodic surface.

Appendices

Appendix A: Split-ring modeling

The simple split-ring resonator is a commonly used structure for the construction of mixers, modulators, and the formation of meta-materials. Using existing knowledge of microstrip structures, and the theory of modeling using series and parallel RLC circuits, it is possible to create an accurate model near resonance. The split-ring's band gap response has drawn attention for use in meta-materials, for which having models to work with forms a firm foundation. By extending the split-ring into a two-dimensional arrangement it may be possible to develop a surface with interesting properties such as negative refractive index.

The purpose of this demonstration is to show how different techniques can be brought together for accurate and reliable modeling of a circuit. In the Sonnet simulations presented, a split ring is formed on a 508μm (20mil) thick silicon substrate with a 2.032μm (0.08mil) layer of silicon dioxide. The ring is made from 1μm thick gold with a conductivity of 4.521×10^7S/m. Figure A- 1 shows the layout of the ring used. The microstrip structure was design to have a characteristic impedance of 50Ω [117]. The top ends of the split ring can be approximated as $\lambda/4$ lines. In actuality the lines are slightly shorter than $\lambda/4$ at resonance due to the presence of the gap. The bottom half of the ring can be seen as a $\lambda/2$ line at resonance. Figure A- 2 shows the S21 simulation results obtained from Sonnet.

A deep rejection is seen at resonance of the ring structure. Multi-mode transmission begins at frequencies higher than 50GHz and the ring begins to radiate electromagnetic energy.

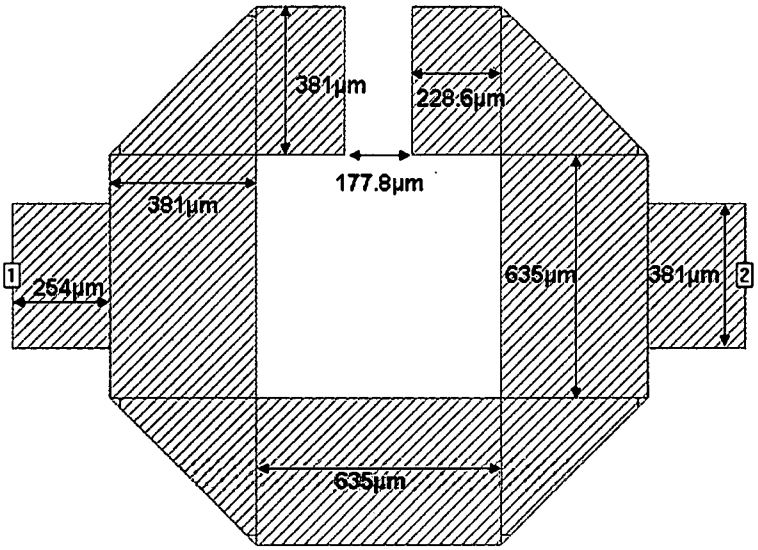


Figure A- 1: Split-ring layout

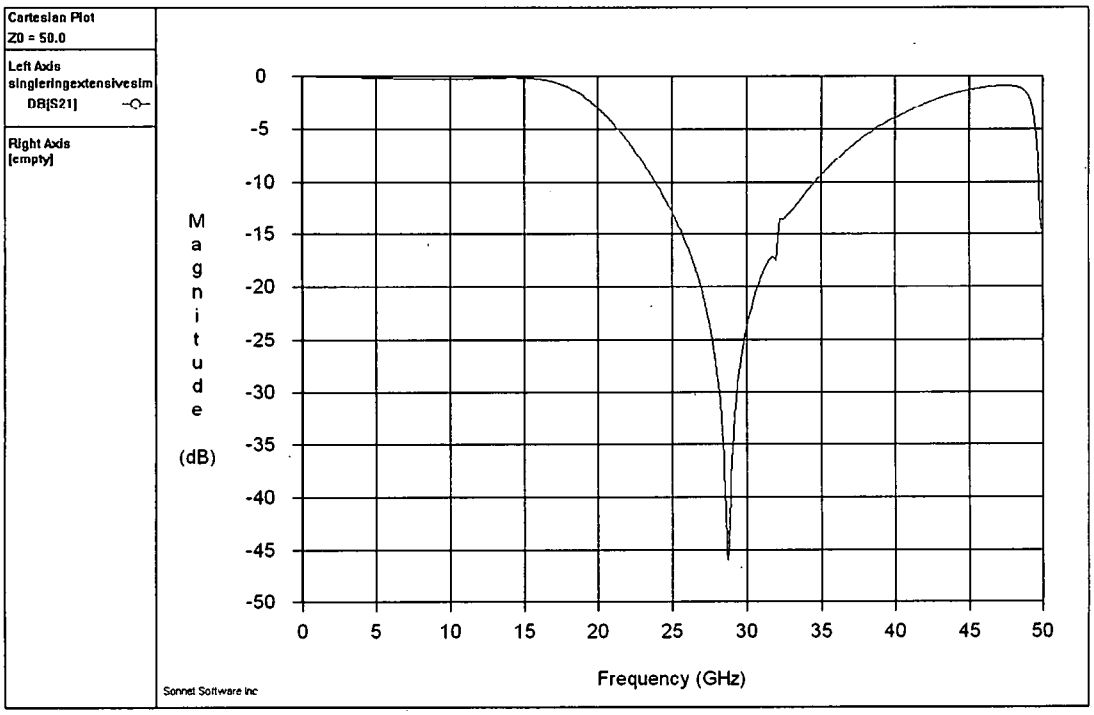


Figure A- 2: Split-ring layout, S21 Sonnet simulation

Parameters of the resonance such as frequency, rejection depth, port impedance, and effective dielectric constant can be used along side with known theories to obtain a better lumped element model of the split ring. Known physical constants and the parameter values found through Sonnet are shown in Table A-1. Using these parameters the λ/2 line will be modeled by a parallel RLC circuit and the two λ/4 line will be approximated by two series RLC circuits connected to the ends of the λ/2 line.

Parameter	Value and description
c	2.99792458×10^{8}m/s speed of light in free space
ε_0	8.8542×10^{-12} F/m permittivity of free space
μ_0	1.2566×10^{-6} Wb/Am permeability of free space
σ_{gold}	$4.521\text{x}10^{7}$S/m electrical conductivity of Au
ε_r	11.7 relative dielectric constant of Si
tanδ	0.001 loss tangent of Si
f_0	28.73×10^{9}Hz frequency of resonance (Sonnet)
S21	-45.9607dB rejection level at resonance (Sonnet)
Z_0	51.88Ω characteristic impedance at resonance (Sonnet)
ε_{eff}	8.25 effective relative dielectric constant of substrate (Sonnet)

Table A-1: List of parameters used for modeling

Before formulae for finding the RLC circuits can be applied, two other parameters must be found, the effective length of the circuit l_{eff}, and the attenuation α. The effective length of the λ/2 line is half the guide wavelength, while that of the λ/4

lines is approximately a quarter. The attenuation α is the sum of the attenuation from ohmic loss α_c, and dielectric losses α_d.

$$\lambda_g = \frac{c}{f_0\sqrt{\varepsilon_{eff}}}(\mathrm{m})$$ **Equation A-1**

$$l_{eff} = \lambda_g / 2$$ **Equation A-2**

$$\alpha_c = 8.686\frac{\sqrt{\pi f_0 / \sigma_{gold}}}{wZ_0}(\mathrm{dB/m})$$ **Equation A-3**

$$\alpha_d \cong 27.3\frac{\varepsilon_{eff}-1}{\varepsilon_r-1}\frac{\varepsilon_r}{\varepsilon_{eff}}\frac{\tan\delta}{\lambda_g}(\mathrm{dB/m})$$ **Equation A-4**

$$\alpha = \alpha_c + \alpha_d(\mathrm{dB/m})$$ **Equation A-5**

Using the results from the above equations, the parallel and series RLC circuits can be found [118]. The parallel RLC bank is used to represent the λ/2 line.

$$R = 8.686\frac{Z_0}{\alpha l_{eff}}(\Omega)$$ **Equation A-6**

$$C = \frac{1}{4f_0Z_0}(\mathrm{F})$$ **Equation A-7**

$$L = \frac{1}{(2\pi f_0)^2 C}(\mathrm{H})$$ **Equation A-8**

The series RLC circuit representing the λ/4 lines requires some approximation in length. The split ends of the ring do not exactly form λ/4 lines because of the gap in between the end causing them to be slightly shorter in length. It was found through previous simulations that the effective length l_{eff} for the λ/4 lines of the split ring is $(84/360)\lambda_g$. Using this approximation with the formulae given below, a very accurate model of the ring can be formed.

$$R = \frac{Z_0 \alpha}{8.686} \lambda_g \left(\frac{84}{360} \right) (\Omega)$$ **Equation A-9**

$$L = \frac{Z_0}{8 f_0} (\mathrm{H})$$ **Equation A-10**

$$C = \frac{1}{(2\pi f_0)^2 L} (\mathrm{F})$$ **Equation A-11**

The results for the RLC circuits are tabulated in Table A-2. Figure A- 3 shows the resulting model. Small 0.01Ω resistances are placed for port isolation and are needed for simulation purposes only. The comparison between the finite element analysis and lumped element model shows the validity of the model between 15 and 45GHz.

Component	Parallel	Series
R	8.4869kΩ	0.148Ω
L	0.183nH	0.2257nH
C	0.1677pF	0.136pF

Table A-2: Parallel and Series RLC calculation results

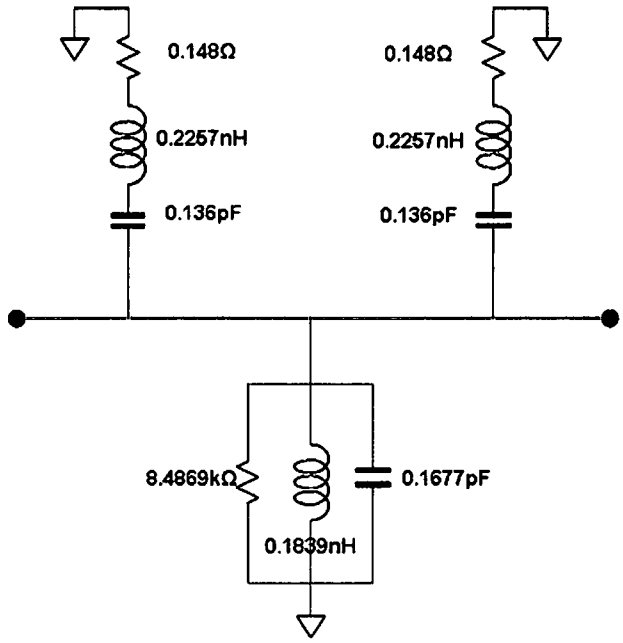


Figure A- 3: Split ring model

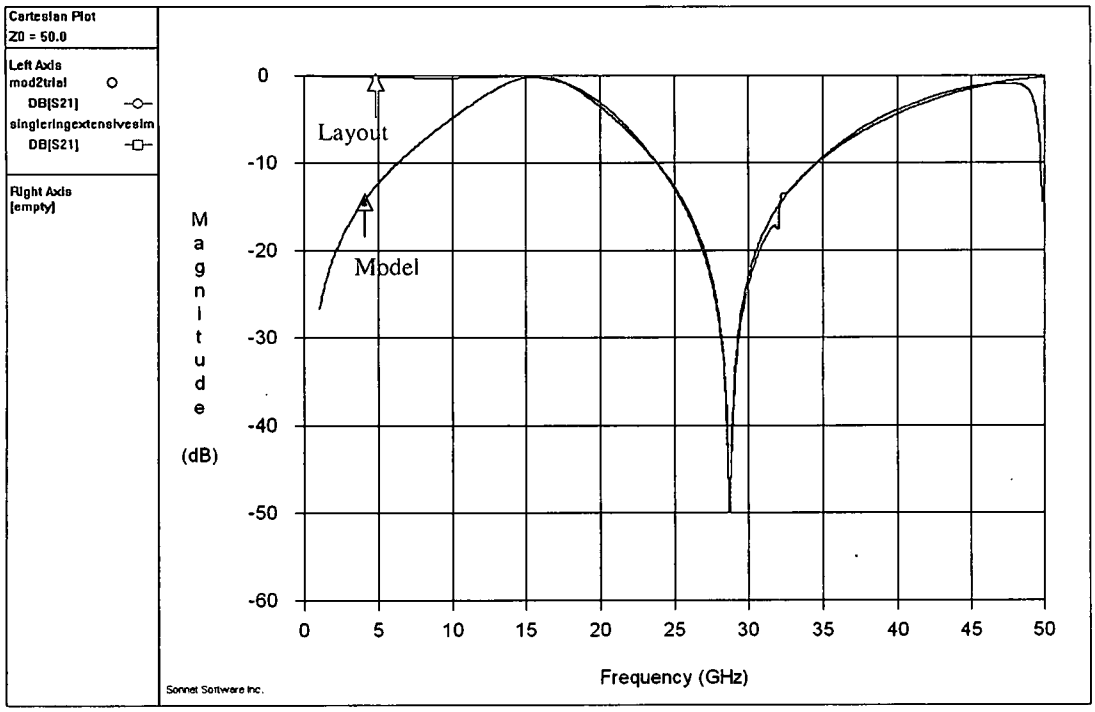


Figure A- 4: Split ring S21 modal and Sonnet simulation comparison

MATLAB code for finding model parameters

```
% Micro Electronic Research
% Finding equivalent electrical model
% Sunday Feb. 15th 2004

clc;close all;clear all;

c=2.99792458*10^8;        %m/s Speed of Light
Eo=8.8542*10^(-12);       %F/m Permittivity of Free Space
uo=1.2566*10^(-6);        %Wb/(Am) Permeability of Free
Space
Za=376.6;               %Ohms Impedance of Air

h=20 ;            %mil
hm=0.0000254*h;      %Meters h(m)
w=15             %mil
wm=0.0000254*w;      %Meters w(m)
wh=w/h;          %w/h ratio
Er=11.7;          %Relative permittivity
tand=0.001;       %loss tangent, tan delta
si=45210000;      %Electrical conductivity of gold S/m

fo=28.73*10^9;    %Resonant frequency, Obtained from Sonnet
Simulation
wo=2*pi*fo;      %Resonant Frequnecy in radians
f1=28.635*10^9;   %Lower Cutoff  Obtained from Sonnet
Simulation
f2=28.83*10^9;    %Upper Cutoff  Obtained from Sonnet
Simulation
S21dB=-45.9607;   %S21 in dB      Obtained from Sonnet
Simulation
Zo=51.88;         %Zo at fo in Ohms  Obtained from Sonnet
Simulation
Ee=8.25;            %Eeff from sonnet   Obtained from
Sonnet Simulation

%Finding Eet (Effective relative permittivity),
a=1+1/49*log(((wh)^4+(wh/52)^2)/((wh)^4+0.432))+1/18.7*log(
1+(wh/18.1)^3);
b=((Er-.9)/(Er+3))^0.053;
Eet=(Er+1)/2+(Er-1)/2*(1*10/wh)^(-a*b)   %Effective
relative permittivity theoreitcal

%Finding Guide wavelength and Phase veolcity
lambdao=c/fo;              %Meter wavelength in freespace
```

```
lambdag=lambdao/sqrt(Ee);            %Meter wavelength
withing wave guide
leff=lambdag/2;                 %Meter effective length of
line for half-wave length
vp=c/sqrt(Ee);                 %m/s wave guide phase velocity

%Finding Alpha
Rm=sqrt(wo*uo/2/si);             %Ohms  Metal wall resistance
ac=8.686*Rm/wm/Zo;   %Alpha c, Attenuation due to conductor
ad=27.3*(Ee-1)/(Er-1)*Er/Ee*tand/lambdag;    %Alpha d,
Attenuation due to dielectric
alpha=ac+ad             %Alpha  , Total attenuation in dB/m

%Lambda_by_4 line Series RLC
R=Zo*alpha/8.686*leff*84/180    %Resistance in Ohms
L=Zo*pi/4/wo;                    %Inductance in H
LnH=L/1e-9
C=1/wo^2/L;                     %Capacitance in F
CpF=C/1e-12
f=1/2/pi/sqrt(L*C)


%Lambda_by_2 line Parallel RLC
R=Zo/(alpha/8.686)/leff         %Resistance in Ohms
C=pi/2/wo/Zo;                    %Capacitancein F
CpF=C/1e-12
L=1/wo^2/C;                      %Inductance in H
LnH=L/1e-9
f=1/2/pi/sqrt(L*C)
```

MATLAB code for 50Ω Microstrip line design

```
c=2.99792458*10^8;        %Speed of light
Er=11.7                   %dielectric constant of Si
Zo=50                     %Desired line impedance
Za=376.6                  %Characteristic impedance of air
h=20                      %Height of Si substrate in mils

A=pi*sqrt(2*(Er+1))*(Zo/Za)+((Er-1)/(Er+1))*(0.23+.11/Er)

wh=4*(.5*exp(A)-exp(-A))^(-1)      %Width of line/height of
substarte
w=wh*h                    %Width of line
```

Appendix B: Sonnet Simulation

Sonnet offers a wide variety of option, and navigating through the various setting is crucial to understanding the results of the simulations. Sonnet starts out with a metal box within which the user is able to create layers of dielectrics. At the boundaries of these dielectrics infinitely thin metal can be placed to form the device. Thick metal models can also be used to further specify the properties of the metal. The thin metal model under the 'Normal' setting requires the current ratio between the top and the bottom of the layer. This ratio is usually found experimentally, but using the default setting of 0 allows Sonnet to use its own approximations which might be slightly lossier than in reality. Box definition is one of the first steps necessary when stetting up a simulation in Sonnet. The placements and definition of ports is critical to getting proper simulations results. Proper use of reference planes also can provide insightful information.

B.1 Box definition

It is important to note that an air layer of at least 5mm is needed to push the box top and bottom away from the device. For general microstrip structures the box bottom can be made of metal and used as a ground plane for the device directly underneath the silicon substrate; however, in the present study the box bottom must be pushed significantly far enough away so that it does not interfere with the testing of the ground plane being designed. Leaving the box tops and bottoms open also avoids the formation of standing waves between the two surfaces. The box sides are also formed by metal, therefore it is possible to short ports by touching metal to the box walls. Sonnet will provide a warning if the

ports are shorted through the box walls. In general having a larger box size is better because Sonnet will only consider fields within the box. Fields outside the box will be assumed to be truncated by the magnetic and electric walls formed by the box surface. Having a significant boundary between the device and the box sides assures that the influence of the box walls on device performance is minimized. As in most cases, advantages gained in one area must be weighed by disadvantages in another. One dimension of the box is fixed by the distance between the ports; the other dimension is under the user's control. Making this dimension larger pushes the walls away from the device but also causes box resonance to occur at lower frequencies. Box resonances tend to corrupt the results obtained from simulations. A healthy compromise is needed between pushing the box walls away and keeping box resonance out of the simulation range.

B.2 Port definition and reference planes

In Sonnet there are several methods by which to define ports. Ports must be placed at box walls. They can be placed inside box walls using reference planes. A reference plane must be first set up and then lossless metal is used to connect the box wall to the desired port location. Sonnet simulates the entire circuit, but then uses a de-embedding processing in which it removes the network connecting the reference planes to the box walls. Figure B- 1 shows the three metal layers for a device with and without the use of reference planes. It should be noted that the layout is using standard microstrip ports, but has a defined ground port. Using a defined ground port (designated by a negative port number)

makes it so that the current flow through the microstrip port and its respective ground port is the same. This makes perfect sense since the amount of current flowing through the microstrip (and its port), should be the same as that flowing through the ground plane. By using a negative port the metal layer is defined as a ground plane. Caution must be taken to remove the box bottom away from the device when simulating devices with defined ground planes. Such a precaution is also necessary for coplanar devices, which could give erroneous results due to the close presence of the box bottom as an additional ground plane.

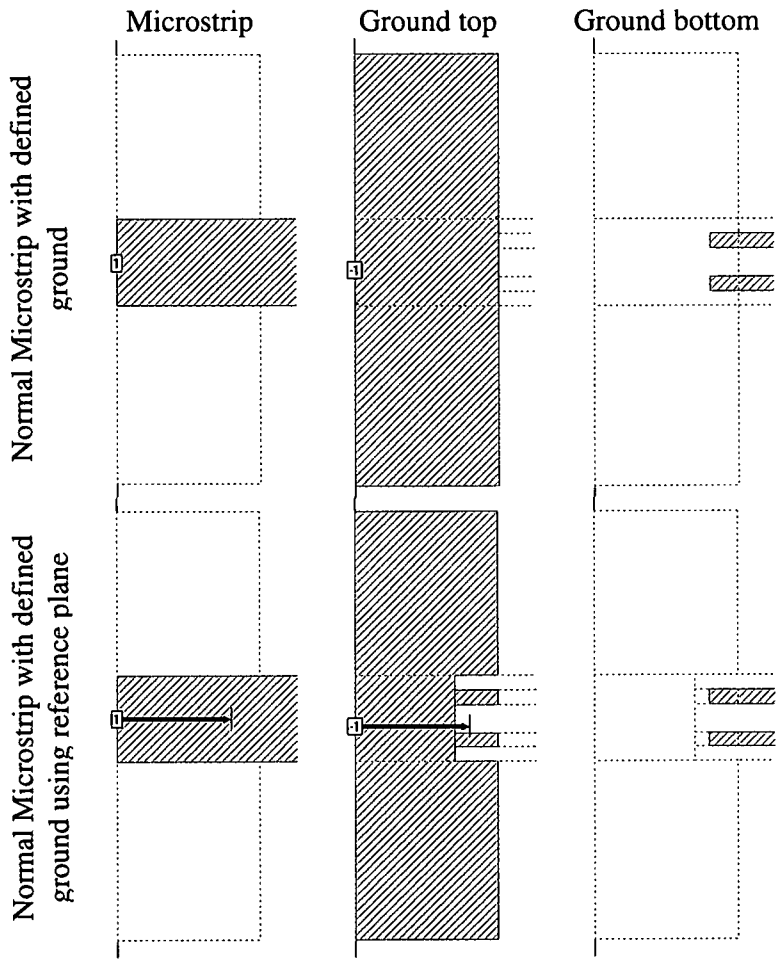


Figure B- 1: Standard microstrip port with defined ground using reference plane

Below is a discussion of the various port definitions relevant to this study. In the first case a standard microstrip port is used with the box bottom acting as the ground plane. In the second case a metal layer is added between the BCB and BST layers, and defined as the ground plane by using the respective negative ports. In the third case the ground plane ports are split to simulate the contact of coplanar probes used for testing actual devices. Using the same port definition at multiple locations is the same as having them externally shorted. The fourth and fifth cases use vias to bring the ground ports up to the same level as the microstrip port. In the two cases with the vias, the first case has the port defined directly at the via while the second has the port defined slightly away from the via. Caution should be taken when defining a port near a via so that the port lies on the metal surface and not on the via itself. The layouts of these five variations are shown in Figure B- 2. The S11 and S21 simulation results for the various port definitions are displayed in Figure B- 3. As can be observed from the results, there is little variation in the result associated with the change in the port definitions. For simulation purposes these various port definitions can in the most be used interchangeably.

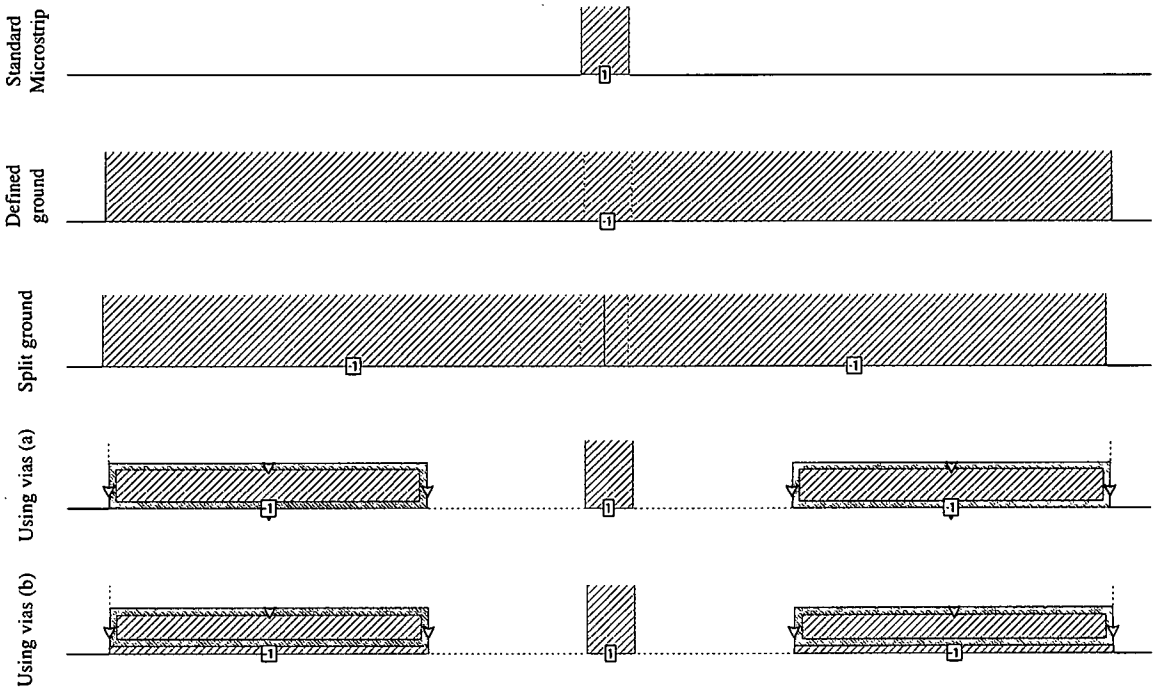


Figure B- 2: Port definition variations

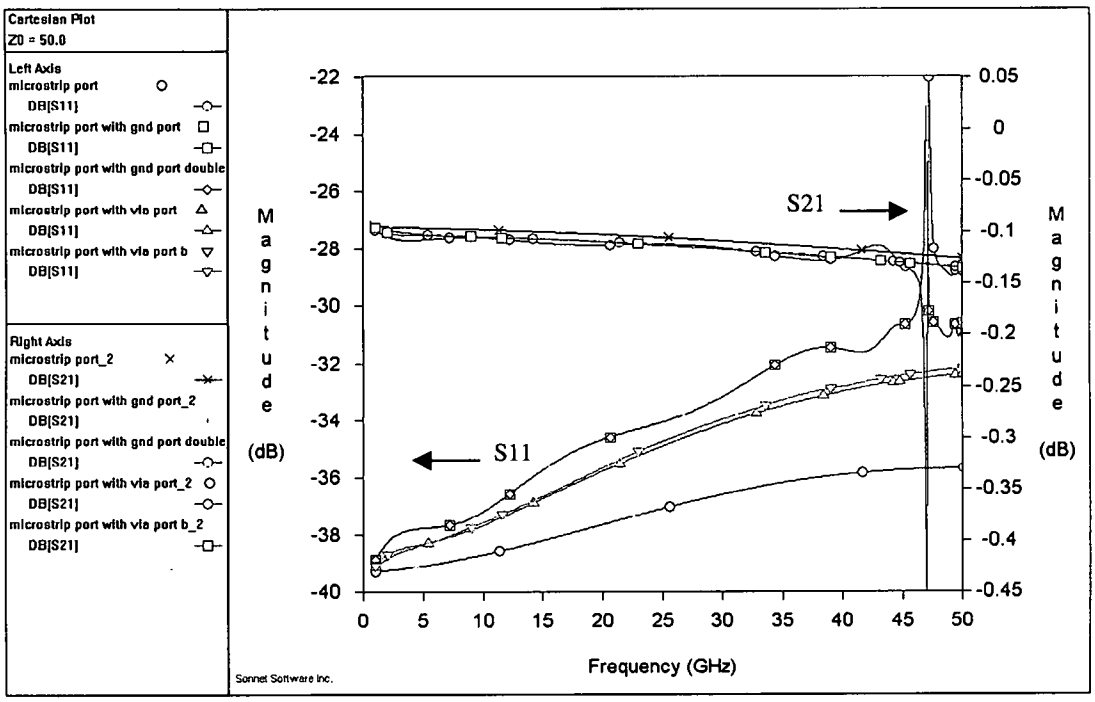


Figure B- 3: S11 and S21 simulation results for port variations

Combinations of port definitions and reference planes can also be used to obtain relevant information. Some techniques used for a 2 parallel strip device with 3 cells are shown in Figure B- 4. The layouts marked as (a) and (b) are the same as those shown in Figure B- 1. The purpose of these experiments is to discern the effect of the large metal pad used at the ports on the response of the device. The large pad allows a large capacitance to form right below the microstrip. Such capacitive loading near the ports could influence the results. Using the large pads at the ports also changes the conditions at the ports from those observed at the start of the inductive strips. Layouts marked as (c) and (d) attempt to minimize such capacitive loading by using smaller connection paths between ports and the inductive strips. Figure B- 5 displays the S11 simulation results for the four cases. There is very little change in the response, especially at lower frequencies. At higher frequencies the discrepancies are greater, but still small. The simulations were conducted with silicon substrate. Although the S11 simulation data closely resemble each other for the four cases, the port impedances observed vary greatly as shown in Figure B- 6. The port impedance is calculated directly at the port. The microstrip width was designed so as to provide 50Ω impedance with a large ground plane. As shown in (a) and (b), the large pads at the ports act as the large ground, thus achieving the desired impedance. In (c) and (d) no large ground exists and much higher impedance is observed at the ports. These experiments provide insight to the internal behavior of the strip structure. The use of the reference planes shows that considerable

impedance mismatch is possible between the device and the ports resulting in internal reflections.

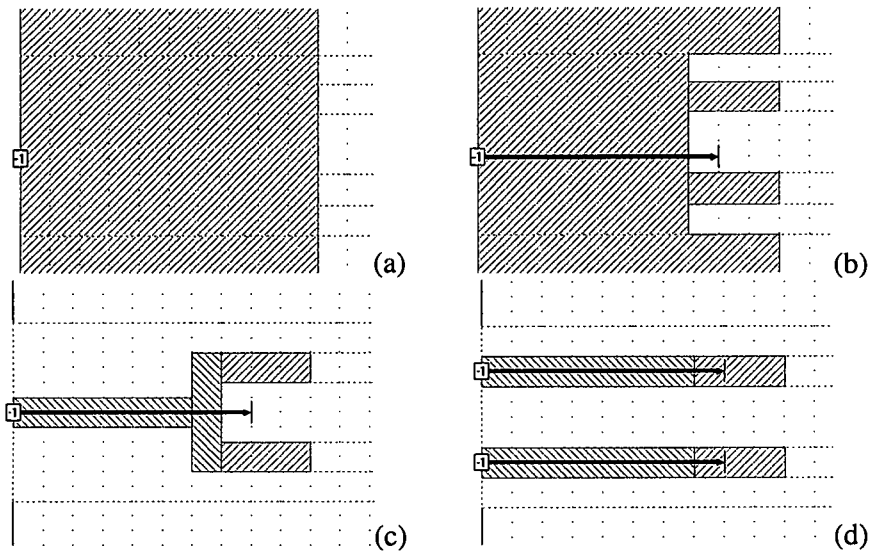


Figure B- 4: Port definitions and reference plane use

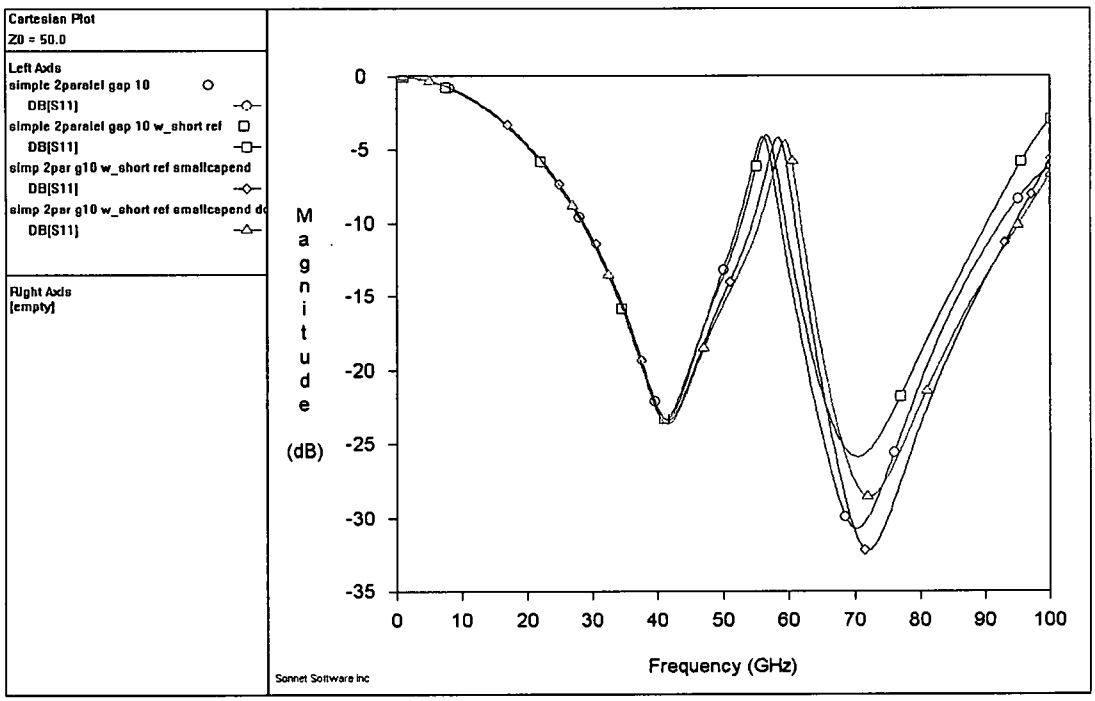


Figure B- 5: S11, Variations in port and reference plane

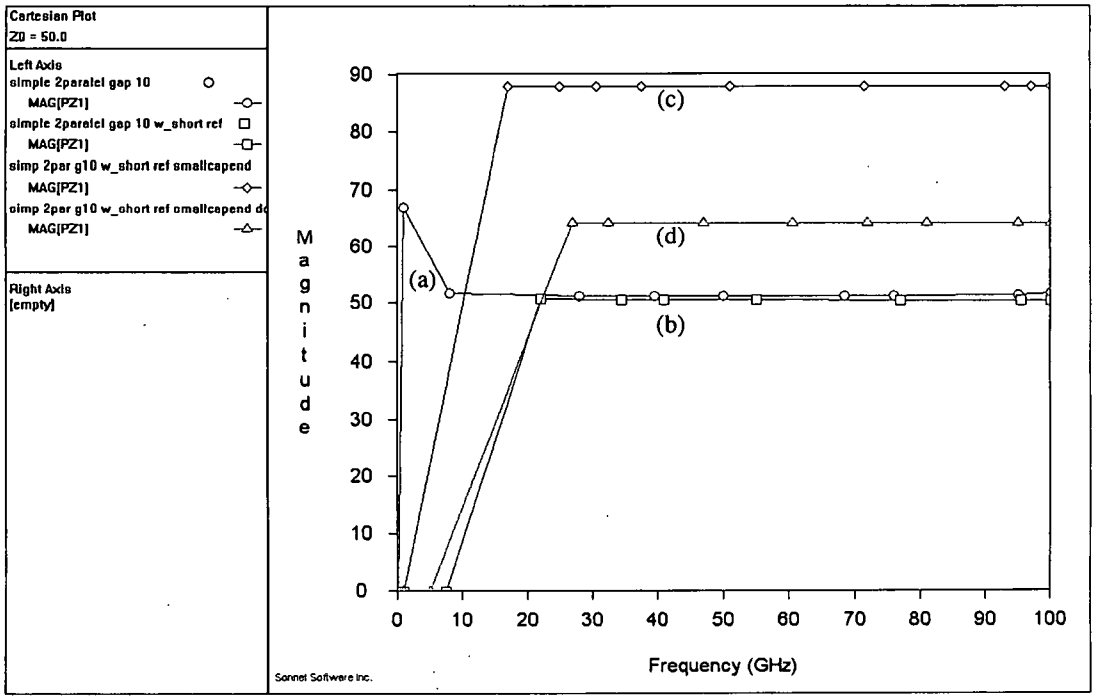
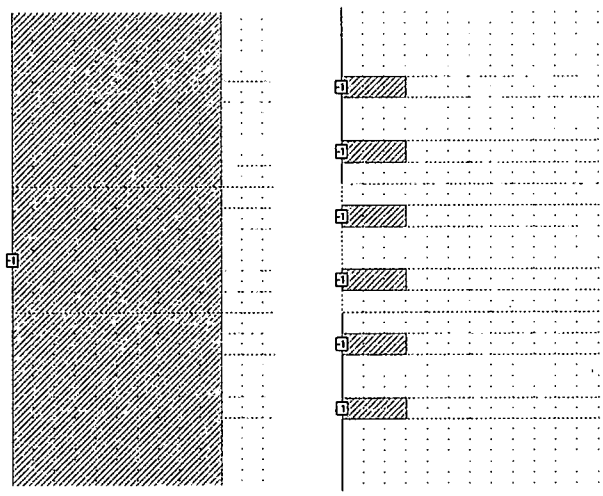


Figure B- 6: Port 1 impedance, Variations in port and reference plane

Figure B- 7 shows the layouts of designs using similar concepts as those discussed above but expanded to 6 parallel strip designs. The large dc pad serves as a shorting region for the port. Using a multiple port definition as shown in the figure, the shorting is done externally. Figure B- 8 shows that the S11 simulations response is not changed by the alteration in the port definition. According to Sonnet manual, using +1/-1 type of port definition means that the sum of the currents flowing through all ports with the same number and positive definition will be the same as the sum of the currents flowing through the ports with the same number with the negative definition. Such changes in port definitions may not produce alterations of the response, but the mechanics of the microwaves and their propagation through the device is subtly altered. In the case of the large pad, the signal phases and excitation levels (voltages) as they arrive at the strip after having flowed through the large pad will be different from

each other because of the different lengths of metal they must traverse through before arriving at the inductive strips; however, because there is only one -1 port and its distance from the +1 port is fixed, the impedance seen is also fixed. In the case of the multiple ports, the excitation and phases are the same but the impedance seen by each port is dependent on the proximity of the -1 ports to the single +1 port. As the -1 port moves away from the +1 port, the impedance observed is increased. This can be more clearly observed when viewed along side the earlier study conducted to demonstrate the change in observed inductance due to the proximity of the strip to the microstrip. Figure B- 9 shows a proportional increase in the port impedance as the distance between the ports is increased. Another point of note is the change in the effective relative permittivity at the ports as reported by Sonnet. As in most cases, impedance and effective permittivity are inversely proportional. The same phenomenon is observed in this study.



Single Port with large pad Multiple port

Figure B- 7: 6 parallel strip design with single port and multiple port definition

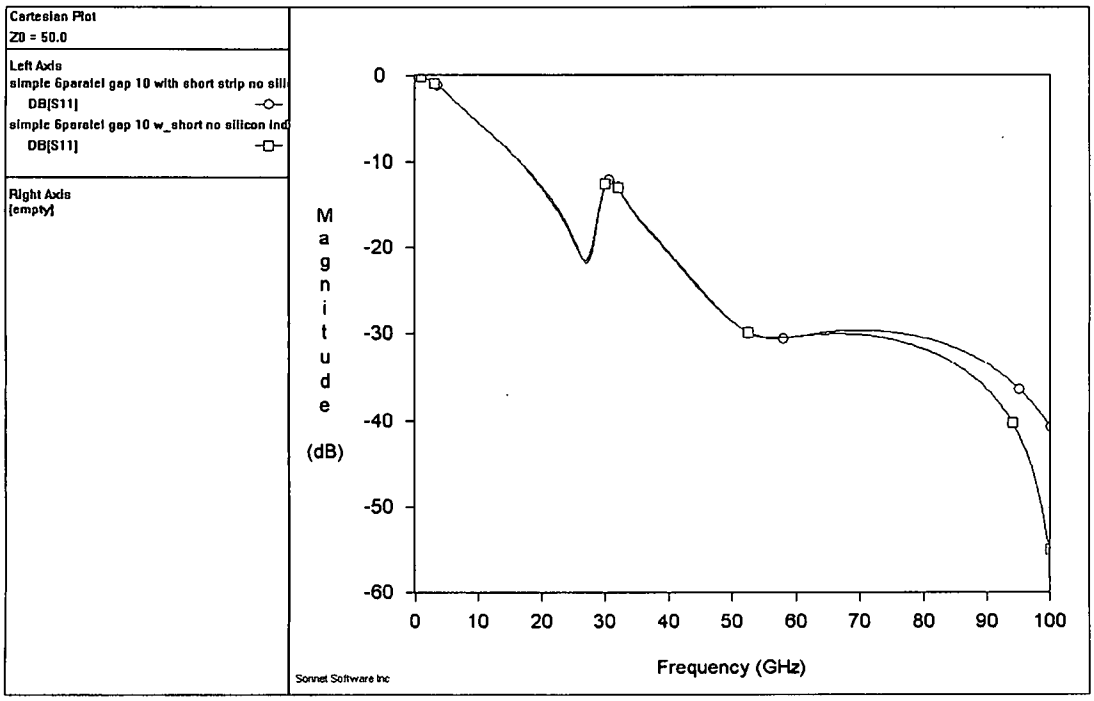


Figure B- 8: S11, 6 parallel strip with single and multi-port design

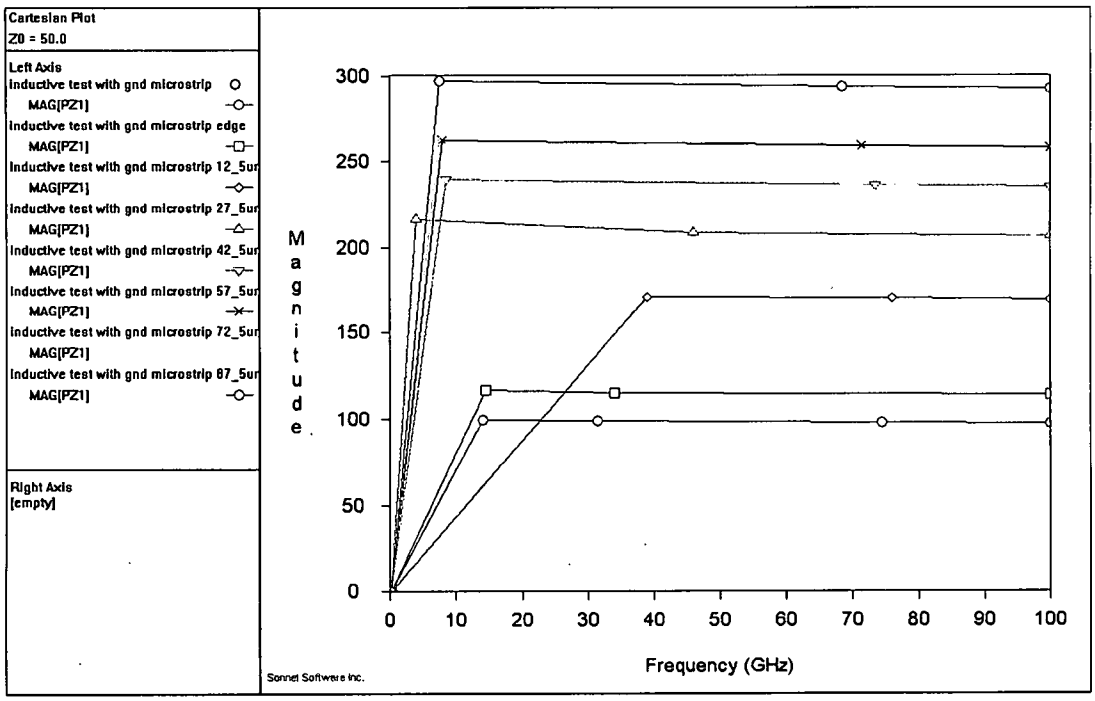


Figure B- 9: Z0 variation due to proximity to microstrip line

B.3 Memory and simulation speed

When dealing with large layouts, issues of memory and simulation time come to the forefront. The amount of RAM installed on a computer system limits how much memory is available to Sonnet. In finite element analysis each subsection is analyzed with respect to its neighbors by loading information into a matrix. The more subsections there are, the larger the matrix becomes that must be solved. As in the case of the FSS design, larger circuits require a significant amount of memory. If there is not sufficient memory, Sonnet will give an error and the simulation will not be conducted. Being able to conduct a cruder and less accurate simulation is better than not being able to conduct a simulation at all. Reducing the memory requirements is essential to getting around this problem. In Sonnet's Analysis → Setup area the memory can be reduced by conducting a cruder simulation. Furthermore, in the Advanced Subsectioning area the default Maximum Subsection Size can be reduced from 20 down to 6, which should significantly reduce memory usage. Another way of reducing memory usage is by simplifying the design layout. By merging polygons and then removing unnecessary vertices and shaping points, the memory is reduced. Higher frequency simulations require greater sub-sectioning of the circuit. By limiting the high frequencies to the absolute minimum the number of subsections will be reduced. Using a thick metal model increases memory usage, as does the use of angled lines. Simple staircase filled rectangular geometries require the least amount of memory.

The speed with which a simulation is done not only depends on the amount of memory needed, but also on the analysis settings used. Higher processor speeds allow for faster analysis of the circuit for a single frequency. If a larger number of frequency points are needed then the resulting simulation will take a longer time. Linear frequency sweeps are tried and tested and give an accurate measure of how long a simulation will take for user defined frequency range and step size. An adaptive sweep allows Sonnet to adjust the number of discrete frequencies and their interval so as to obtain the best result. When obtaining data adaptively algorithms are used to predict the response of the circuit at intermittent frequencies. In most cases the adaptive sweep is recommended for large frequency ranges, however, if box resonances and the advent of multi-mode transmission lie within the frequency range of simulation, then Sonnet tends to take many analysis points near the resonance because the adaptive program is unable to predict the rapid changes associated with resonance. The existence of the resonances and multi-mode transmission complicate matters on their own and the data gained from the excessive frequency simulations is of little value. In cases where the location of box resonance and the onset of multi-mode transmission are already known, frequency sweep combinations can be used to take advantage of linear and adaptive sweeps.

Appendix C: Mask Design

Mask designing is very important as they are needed in standard lithography techniques for pattering of metal layers and selective etching of dielectrics. Mask designing can be done in CAD (computer aided design) software, but it can also be done using Sonnet. Using the layout tools, a mask can be specified the way any other device is drawn, i.e. using polygons to represent metallic areas. Once the layout has been prepared Sonnet can export the design in proper CAD format. Mask designing can be a daunting task in the beginning, but once a rough idea of the organization of the mask is made there are only a few simple design rules that must be followed.

The masks made for this study were able to incorporate a total size of 1" by 1". One square inch is the maximum available area within which the designs must be incorporated. As each mask costs several hundred dollars, good organization is necessary to make efficient use of available real-estate. Once the setup for a mask is created and organization of the devices is understood, it is relatively easy to follow the design rules. Mils and microns are both used as the units of measure for mask designing, but for this study mils was used to make the mask. The rules are used as rough guidelines but the relevant spacings must not be reduced beyond those prescribed. The rules are as follows:

i) 25 mils gap must exist between the edge of the mask and any metallization

ii) 20 mils gap must be present between alignment marks and a device

iii) 40 mils gap must exist between two adjacent devices

The edges of the mask are not used for metallization because it is difficult to pattern the metal towards the edges. Usually the devices formed away from the edges are of higher quality with better conductor edges, and uniform film deposition. To avoid using the edges, a 25mil boundary is created around the perimeter of the mask. The spacing between devices and alignment marks is needed so that the performance of a device is not influenced by the presence of conductors which are not part of the device under observation. Alignment marks are relatively small and do not require as much spacing as a device.

Alignment marks are used as reference points so that during processing layers can be properly aligned with the layers already manufactured. The number of alignment marks and their distribution is determined by how the devices are to be manufactured. If each device (or a group of devices) on a mask must undergo manufacturing procedures unique to that device, then it is preferred to have alignments marks for each device. This way only a portion of the mask needs to be concentrated on during manufacturing. If all the devices on a mask are to undergo the same procedure, then only one set of alignment marks along the perimeter are needed. The use of fewer alignment marks improves the efficiency with which space can be used, but then all the devices on a given mask must be manufactured at the same time, reducing flexibility with which individual devices can be manufactured.

Alignment marks are designed to be larger in the bottom layers, and progressively grow smaller in the upper layers. The bottom layers are manufactured first, and the large bottom alignment mark provides a perimeter

within which the upper alignment marks must snugly fit. The number of unique alignment marks needed is determined by the number of mask involved in the manufacturing of a device. For simple designs involving only a few layers very simple alignment marks suffice, but with increased number of layers the complexity of the alignment marks can grow. For flexibility of manufacturing, the alignment marks must not lose functionality if certain non-essential layers are not patterned. For a simple metal/dielectric/metal layer structure, in which each layer is patterned by a mask, the use of progressively smaller alignment marks such as a square-cross-square is enough. As shown in Figure C- 1, the smaller alignment marks fit into the boundaries created by the larger alignment marks from the layers below. However, if for some reason the pattering of the dielectric was to be eliminated so as to save on manufacturing time, such an alignment scheme would fail because without the middle layer alignment mark there will be no clear boundaries for the top alignment mark. Such things must be considered when choosing an alignment mark scheme. For the designs manufactured for this study, only the metal layers were patterned and therefore a simple square-cross combination of alignment marks is sufficient. Eight alignment marks were evenly distributed along the 25mil boundary because all the devices on the mask were to be manufactured at the same time on a single silicon wafer.

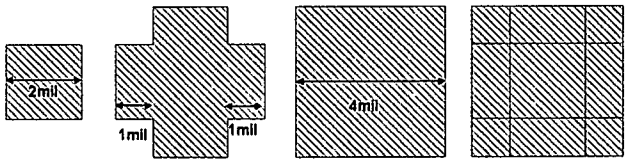


Figure C- 1: Alignment marks

The distribution and organization of the devices within the mask is complicated by the number of devices, sizes, and the number of instances of each device. It is generally preferred to have more than one instance of a device so that if once instance does not survive manufacturing then another instance might be available. The number of instances of a device is limited by the available space. Having a rough idea of how to accommodate the devices and the spacing between them is critical for efficient mask design. Two techniques are presented here for mask designing; in either case the initial steps for mask layout are the same. A 1" square box is created within Sonnet with a very small cell size. Two types of metal are used to create the designs. One type of metal will be used as for the actual mask layout (in this case gold), while the other is used only for alignment and organization purposes (lossless). The second type of metal will be removed before the final mask layout is ready. A 25 mil boundary is created along the edge of the inside edge of the box using lossless metal. All designs will be created within this boundary.

Depending on the distribution of the device sizes and the number of instances of each device there are two possible approaches, each with advantages and disadvantages. If the sizes of the devices are varied considerably and the number of instances is small, then each device will have to be placed within the mask individually. The best way to achieve this is having as many layers within the mask layout as there are within the device. All the layers of the device must be copied directly into the mask. Doing so assures that the device layers are well aligned. Then the device must be moved with all its layers to its location within

the mask. This can be a difficult procedure because throughout this process all the layers of the device must remain selected. If selection is lost then the layers may become misaligned or get entangled with other designs. The positioning of the device is best determined by the cursor information given in the right-hand corner of the Sonnet display. The various patterned layers must be separated into individual files before generating the final masking file as specified by the manufacturer. This is a difficult method by which to create a mask. The process can be made slightly easier by having a cell size which is as large as the smallest dimension during the actual mask design. Once the mask has been completed the cell size can be reduced to a finer setting. Copied devices are pasted automatically in the top-left corner of the mask, therefore starting the layout from the bottom-right may reduce the entanglement of various designs during copying and pasting. Having a well organized plan for the location of each device prior to the actual mask design is essential for this method. It must be known beforehand where to place each device so that the cursor information can be relied upon for proper positioning. The task is difficult especially if the there many devices that must be accommodated within the mask. Sonnet also tends to use a lot of memory when working with large layouts. Moving around within a complicated layout with many devices is a slow process. If the auto save function is selected in the preferences, Sonnet makes backups of the layout but even saving the layout takes a considerably longer time than normal layouts. This method of mask design is slow but if properly planned and executed it is quite reliable.

Another method for mask designing relies on having many devices in the design with the same size. A lot less planning is needed in this design and only a rough idea of the organization is necessary. In this method 20 mil boundaries are created around a device. The 20 mil boundary of a device will act like a buffer zone and combine with the 20 mil boundary of an adjacent device to form the 40 mil gap required by the masking design rules. The boundary is created using 20mil squares placed around the edge of the device. The squares are connected and then merged together for bettering handling of the stencil created. Properly aligned notches are created at the edges so that adjacent stencils fit together like pieces of a jigsaw puzzle. Figure C- 2 gives an example of the use of the stencil technique.

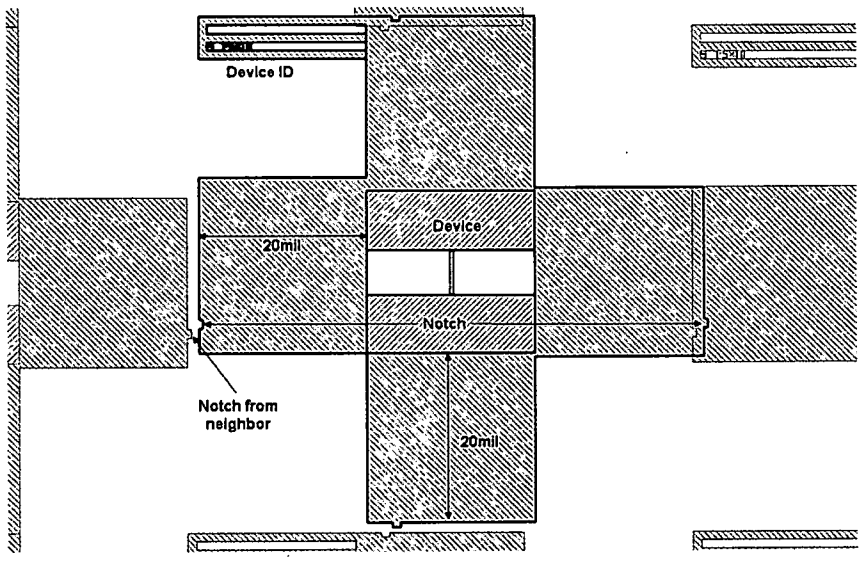


Figure C- 2: Stencil technique demonstration

The stencil technique greatly increases the speed with which a mask can be created. The alignment of the layers is done by a single growth point from which

the design grows by increments. The notches make it easier to align devices with their neighbors. The masks can also be created in two different layouts. The simplicity with which the design is created also has its faults. Because the layout grows based on the neighbors and their relative positions, a single mistake can propagate throughout the design. In the previous method, the absolute positions provided by the cursor were used as the reference points for the device positioning. Another problem with the stencil technique is that each device must have its own stencil. Although the stencil is relatively easy to construct the speed of this techniques is derived from stencils fitting together. Figure C- 3 shows the mask created using the stencil technique. Each design is connected to at least one neighbor through the stencil. The final step is to remove the stencils and create a DFX file using Sonnet.

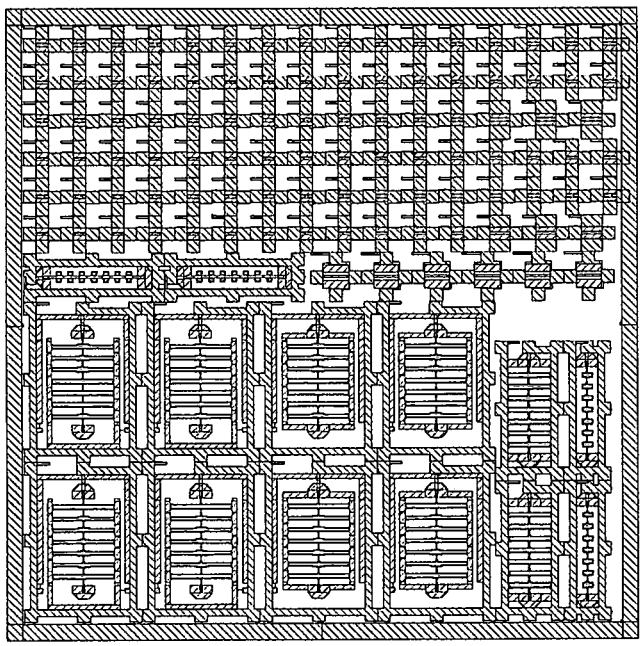


Figure C- 3: Mask using stencil technique

Appendix D: Lift-off Processing of Au or Au+Pt

Starting from High Resistivity Si/SiO2 substrates

No.	Process Step	Time	Status
1	1:10 BOE:DI H_2O solution	30 secs	
2	DI rinse wafers (3 or 4 rinses)		
3	Prebake wafers @ 110 C on the hotplate	1 min	
4	Degreasing in Acetone and IPA (spin+spray)	30 Secs	
5	PMGI SF-11 spin coat @4000 rpm, ramp at 200 (~1 µm thick) Remove edge-bead with nanoEBR	30 secs	
6	Bake at 270 C on the hot-plate	2 mins	
7	Spin-coat S1813 photoresist @4000 rpm, ramp at 200 (~2 µm) Remove edge-bead with acetone	30 secs	
8	Bake at 110 C on the hot-plate	1 min	
9	Align and expose in MJB3	12 secs	
10	Develop in AZ351 developer solution followed by DI spray And blow dry in N2 (examine pattern)	30 secs	
11	Deep UV exposure	200 secs	
12	Develop in SAL101 solution followed by DI rinse and N2 blow Dry (examine pattern)	2 mins	
13	Plasama ash in O2 plasma	4-8 mins	
14	Pre-metal etch (BOE solution, 1:10 with DI H2O)	30 secs	N/A
15	Metallization (e-beam), Ti: 20 nm, Au: 1 µm		
16	Lift-off step 1: Soak in acetone for ~ 5 mins. Spin+spray acetone, followed by IPA to remove residue (examine pattern)		
17	Lift-off step 2: Soak in 1165 solution @90C	2 mins	
18	DI rinse in the rinse station, blow dry in N2 (examine pattern)	4 cycles	
19	Plasma Ash in oxygen plasma	2-4 mins	
20	Examine pattern under the microscope		

Abbreviations

ac, AC	Alternating current
Ag	Silver
Al	Aluminum
Au	Gold
Ba	Barium
BCB	Benzocyclobutene
BST, BSTO	Barium Strontium Titanate $Ba_xSr_{1-x}TiO_3$
CPW	Coplanar Waveguide
dc, DC	Direct Current
EBG	Electromagnetic Bandgap
FSS	Frequency Selective Surface
GaAs	Gallium Arsenide
HIGP	High Impedance Ground Plane
$LaAlO_3$	Lanthanum Aluminate
MEMS	Microlectromechanical Systems
MgO	Magnesium Oxide
MMIC	Monolithic Microwave Integrated Circuit
Mn	Manganese
MOCVD	Metal Organic Chemical Vapor Deposition
Nb	Niobium
PBG	Photonic Bandgap
PLD	Pulse Laser Deposition
Pt	Platinum
RCS	Radar Cross-Sectionn
RF	Radio Frequency
Ru	Ruthenium
Si	Silicon
Sr	Stronium
STO	Strontium Titanate $SrTiO_3$
Ti	Titanium
TiO_3	Titanium Oxide

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