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Shailesh Balwant Nerurkar
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**MODELING, DESIGN AND LAYOUT OF A CASCADED
THIRD-ORDER FEED-FORWARD DELTA-SIGMA
ANALOG-TO-DIGITAL CONVERTER FOR
RF WIRELESS APPLICATIONS**

Dissertation

Submitted to

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UNIVERSITY OF DAYTON

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by

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Dayton, Ohio

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MODELING, DESIGN AND LAYOUT OF A CASCADED THIRD-ORDER FEED-FORWARD DELTA-SIGMA ANALOG-TO-DIGITAL CONVERTER FOR RF WIRELESS APPLICATIONS

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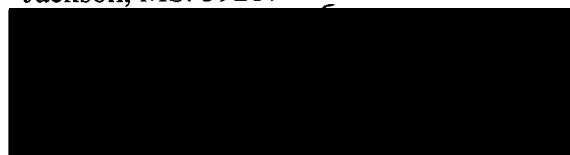
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ABSTRACT

MODELING, DESIGN AND LAYOUT OF A CASCADED THIRD-ORDER FEED-FORWARD DELTA-SIGMA ANALOG-TO-DIGITAL CONVERTER FOR RF WIRELESS APPLICATIONS

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In this dissertation, modeling, design and chip layout of a novel cascaded third-order feed-forward delta-sigma analog-to-digital converter (ADC) is presented. This ADC is realized using a fully differential architecture and produces a high resolution at a data output rate (DOR) of 2.5 MS/s for RF wireless applications. The delta-sigma modulator consists of a second-order single-bit feed-forward modulator cascaded with a multi-bit first-order modulator. The cascaded feed-forward third-order (2-1) ADC is simulated in Matlab. We modeled an ideal feed-forward (2-1) ADC in Simulink; and then, gradually introduced non-idealities like finite dc gain, finite slew-rate, finite unity gain band-width, thermal and amplifier noise, clock jitter to observe their effects on the signal-to-noise ratio (SNR). A new derivation on finding coefficients of the cascaded feed-forward (2-1) ADC is presented. A novel *NMOS-PMOS* thermometer-to-binary encoder was incorporated in the design of the multi-bit ADC. The delta-sigma modulator is designed using Cadence Virtuoso (Spectre simulator) in TSMC 0.18 μ m CMOS technology. The power consumption of the designed modulator ($V_{DD} = 2.5$ V) is 12.74 mW, the resolution is 12.16 bits (over-sampling ratio $M = 32$), and the figure of merit (FOM) is 1.11 pJ. The delta-sigma modulator is implemented in Cadence Virtuoso-XL

Layout editor in 0.5 μm (0.6 μm drawn length) AMI CMOS technology. The power consumption of the implemented modulator ($V_{DD} = 5\text{ V}$) is 63.44 mW, the resolution is 10.33 bits (over-sampling rate= 20), and the FOM is 19.7 pJ. The area occupied by this implemented modulator is 1.44 mm².

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TABLE OF CONTENTS

1	INTRODUCTION	1
1.1	CURRENT RESEARCH IN RF WIRELESS RECEIVERS AND ADC.....	2
1.2	DISSERTATION ORGANIZATION.....	3
1.3	APPLICATIONS	5
1.4	ORIGINALITY	6
2	FUNDAMENTALS OF RF DESIGN.....	7
2.1	TRANSMISSION LINES	8
2.1.1	<i>Power transfer efficiency in transmission lines</i>	<i>8</i>
2.2	INPUT AND OUTPUT MATCHING NETWORKS	10
2.2.1	<i>S-Parameters</i>	<i>10</i>
2.2.2	<i>Smith Chart</i>	<i>11</i>
2.3	PROBLEMS ASSOCIATED WITH RF DESIGN	12
2.3.1	<i>Selectivity</i>	<i>13</i>
2.3.1.1	Harmonic Distortion	13
2.3.1.2	Gain Compression.....	14
2.3.1.3	Desensitization and Blocking	15
2.3.1.4	Inter-modulation (IM).....	15
2.3.1.5	Third Order Intercept point, IIP3	17
2.3.2	<i>Sensitivity</i>	<i>17</i>
2.3.2.1	Thermal Noise.....	18
2.3.2.2	Shot Noise (Schottky Noise).....	18
2.3.2.3	Flicker Noise (1/f Noise).....	19
2.3.2.4	Noise Figure.....	19
2.4	RECEIVER ARCHITECTURES	20
2.4.1	<i>Heterodyne Receiver.....</i>	<i>21</i>
2.4.2	<i>Homodyne Receiver</i>	<i>22</i>
2.4.3	<i>Low IF Receiver.....</i>	<i>23</i>
2.5	MAIN COMPONENTS IN RECEIVER ARCHITECTURE.....	24
2.5.1	<i>RF Band-pass Filters</i>	<i>24</i>
2.5.2	<i>Low Noise Amplifiers.....</i>	<i>24</i>
2.5.3	<i>Mixer.....</i>	<i>25</i>
2.5.4	<i>Image-reject Filter (IR).....</i>	<i>26</i>
2.5.5	<i>Channel Select Filter.....</i>	<i>26</i>
2.5.6	<i>Base-band Signal Processing</i>	<i>27</i>
2.5.7	<i>Analog-to-digital Converter (ADC).....</i>	<i>27</i>
2.6	SOME CURRENT WIRELESS STANDARDS AND SPECIFICATIONS	27
2.6.1	<i>Global System for Mobile Communication (GSM)</i>	<i>28</i>
2.6.2	<i>Bluetooth Standard</i>	<i>28</i>
2.6.3	<i>Universal Mobile Telecommunication System (UMTS).....</i>	<i>29</i>
2.6.4	<i>Code Division Multiplexing Access (CDMA 2000).....</i>	<i>29</i>
3	INTRODUCTION TO NYQUIST AND OVER-SAMPLING DATA CONVERTERS.....	30
3.1	TYPES OF DATA CONVERTERS	30
3.1.1	<i>Nyquist Data Converters.....</i>	<i>30</i>
3.1.2	<i>Over-sampling Data Converters.....</i>	<i>31</i>
3.1.3	<i>Quantization Error.....</i>	<i>33</i>
3.2	SIGNAL-TO-NOISE (SNR) RATIO OF NYQUIST AND OVER-SAMPLING ADCS	34
3.2.1	<i>Signal-to-Noise noise (SNR) Ratio of Nyquist rate Data Converters.....</i>	<i>34</i>
3.2.2	<i>Signal-to-Quantization noise (SNR) Ratio of Over-sampling Data Converters.....</i>	<i>36</i>
3.3	OVER-SAMPLING NOISE SHAPING DATA CONVERTERS.....	38
3.3.1	<i>SNR of First-Order Over-sampling Noise Shaping Data Converters.....</i>	<i>40</i>
3.3.2	<i>SNR of Second-Order Over-sampling Noise Shaping Data Converters.....</i>	<i>42</i>

3.4	HIGHER ORDER MODULATORS	44
3.5	CASCADED NOISE SHAPING MODULATORS.....	45
3.6	DERIVATION OF AN EMPIRICAL FORMULA FOR COEFFICIENTS OF A CASCADED THIRD ORDER (2-1) FEEDBACK TOPOLOGY FOR OPTIMUM NOISE SHAPING.....	48
3.7	DERIVATION OF AN EMPIRICAL FORMULA FOR COEFFICIENTS OF THE PROPOSED CASCADED THIRD ORDER (2-1) FEED-FORWARD FOR OPTIMUM NOISE SHAPING.....	53
4	ARCHITECTURES OF DELTA SIGMA MODULATORS.....	59
4.1	FIRST ORDER SINGLE-BIT DELTA SIGMA MODULATOR	60
4.2	SECOND ORDER SINGLE-BIT DELTA SIGMA MODULATOR	60
4.3	SECOND ORDER MODULATOR WITH MULTI-BIT QUANTIZER	61
4.4	HIGHER ORDER SINGLE-BIT OR MULTI-BIT MODULATORS.....	62
4.5	CASCADED SINGLE-BIT DELTA SIGMA MODULATOR.....	63
4.6	CASCADED MULTI-BIT HIGHER ORDER MODULATORS.....	65
4.7	FEED-FORWARD ARCHITECTURE WITH FEEDBACK COEFFICIENTS.....	67
4.8	HYBRID FEED-FORWARD TOPOLOGY.....	67
4.9	SIMPLE FEED-FORWARD ARCHITECTURE.....	68
4.10	PROPOSED CASCADED THIRD ORDER FEED-FORWARD DELTA SIGMA ADC.....	69
4.11	SUB-COMPONENTS WITHIN THE PROPOSED ADC	71
4.12	LINEAR MODEL OF THE CASCADED FEED-FORWARD DELTA SIGMA MODULATOR.....	72
5	INTEGRATED CIRCUIT DESIGN.....	79
5.1	OPERATIONAL AMPLIFIER DESIGN	79
5.1.1	<i>Properties of Operational Amplifier</i>	79
5.2	TOPOLOGIES FOR OPERATIONAL AMPLIFIERS	83
5.2.1	<i>Two Stage Miller Compensated OTA</i>	84
5.2.2	<i>Telescopic Cascode OTA</i>	85
5.2.3	<i>Folded Cascode OTA</i>	86
5.3	COMMON MODE FEEDBACK CIRCUIT	87
5.3.1	<i>Continuous CMFB Using Resistor Divider</i>	88
5.3.2	<i>Switched Capacitor CMFB</i>	89
5.4	NON-IDEALITIES IN OTA	90
5.4.1	<i>Finite DC Gain</i>	90
5.4.2	<i>Linear Settling Time and Finite Unity Gain Bandwidth</i>	92
5.4.3	<i>Slew Rate</i>	93
5.4.4	<i>Thermal Noise</i>	94
5.4.5	<i>Switch On-resistance and Dominant Closed Loop Pole of OTA</i>	94
5.4.6	<i>OTA Capacitive Loading</i>	96
5.5	DESIGN OF THE FOLDED CASCODE OTA	97
5.6	FULLY DIFFERENTIAL COMPARATORS.....	100
5.6.1	<i>Regenerative Latch Comparators</i>	102
5.6.2	<i>Non-idealities in Comparators</i>	103
5.7	INTEGRATORS	104
5.7.1	<i>Switched Capacitor Integrators</i>	106
5.8	NON IDEALITIES IN SWITCHED CAPACITOR INTEGRATOR.....	108
5.8.1	<i>Settling Time</i>	108
5.8.2	<i>Gain Errors</i>	108
5.8.3	<i>Pole Errors</i>	109
5.8.4	<i>Thermal Noise</i>	109
5.9	ANALOG-TO-DIGITAL AND DIGITAL-TO-ANALOG CONVERTER (ADC/DAC)	110
5.9.1	<i>Multi-bit ADC and DAC Non-idealities</i>	112
5.10	NOVEL NMOS-PMOS THERMOMETER-TO-BINARY ENCODER	113
6	VLSI CIRCUIT IMPLEMENTATION.....	114

6.1	DIFFERENTIAL 1-BIT DAC	114
6.2	FULLY DIFFERENTIAL IMPLEMENTATION	118
6.3	CAPACITOR MISMATCH	120
6.4	THERMAL OR kT/C NOISE.....	121
6.5	NON-OVERLAPPING CLOCKS.....	122
6.6	DETERMINATION OF THE NOISE TRANSFER FUNCTION (NTF).....	124
6.7	IMPLEMENTATION OF THE FEED-FORWARD SUMMING JUNCTION.....	128
7	MODELING OF CASCADED FEED-FORWARD THIRD ORDER DELTA SIGMA MODULATOR.....	131
7.1	SAMPLING JITTER.....	131
7.2	THERMAL kT/C NOISE.....	133
7.3	OP-AMP NOISE	135
7.4	MODELING SLEW-RATE, FINITE GAIN-BANDWIDTH AND FINITE DC GAIN	136
8	RESULTS.....	139
8.1	CADENCE SIMULATION RESULTS	139
8.2	QUANTIZATION NOISE.....	148
8.3	CADENCE LAYOUT RESULTS.....	150
8.4	FIGURE OF MERIT (FOM)	157
9	CONCLUSION AND FUTURE WORK.....	162
	APPENDIX A BASIC ADC AND DAC DESIGNS.....	165
A. 1	ANALOG-TO-DIGITAL CONVERTER (ADC)	165
A. 1.1	Flash ADC	165
A. 1.2	Two-step Flash ADC.....	166
A. 1.3	Pipeline ADC.....	166
A. 1.4	Successive Approximation (SAR) ADC	167
A.2.	DIGITAL-TO-ANALOG CONVERTER (DAC)	168
A. 2.1.	R-2R DAC	169
A. 2.2	Charge Scaling DAC	169
	APPENDIX B STATIC AND DYNAMIC PARAMETERS.....	170
B.1.	OFFSET ERROR.....	171
B.2.	GAIN ERROR	172
B.3.	DIFFERENTIAL NON LINEARITY (DNL).....	172
B.4.	INTEGRAL NON LINEARITY (INL).....	173
B.5.	SIGNAL-TO-NOISE RATIO (SNR).....	174
B.6.	SIGNAL-TO-NOISE AND DISTORTION (SINAD)/ (SNDR).....	174
B.7.	EFFECTIVE NUMBER OF BITS (ENOB)	174
	APPENDIX C MATLAB ALGORITHMS AND OUTPUT SPECTRA.....	175
C.1	DATA OR INPUT SIGNAL.....	175
C.2	SECOND ORDER FEED-FORWARD MODULATOR.....	175
C.3	FIRST ORDER MULTI-BIT MODULATOR.....	176
C.4	DIGITAL_ERROR_CORRECTION.....	177
C.5	SIGNAL PROCESSING	178
C.6.	OUTPUT SPECTRA.....	179
	APPENDIX D LAYOUTS.....	183
	APPENDIX E MATLAB FUNCTIONS.....	194
E.1	MATLAB CODE FOR FINITE DC GAIN, FINITE SLEW-RATE AND FINITE GAIN BANDWIDTH.....	194

E.2 MATLAB ALGORITHM FOR FINDING NTF OF THE SECOND ORDER FEED-FORWARD MODULATOR..	196
E.3 MATLAB FUNCTION FOR CALCULATING OP-AMP NOISE	197
APPENDIX F SIMULATION RESULTS.....	198
F.1 OP-AMP PARAMETERS	198
F.2. WIDE SWING CURRENT MIRROR.....	205
F.3. DNL AND INL FOR 3-BIT DAC.....	206
F.4. SWITCHED CAPACITOR INTEGRATOR RESPONSE	207
APPENDIX G TESTING OF PHYSICAL LAYOUT OF THE ADC	208
REFERENCES.....	211

LIST OF FIGURES

FIGURE 2.1 POWER TRANSFER EFFICIENCY WITH $Z_L = Z_S^*$	9
FIGURE 2.2 POWER TRANSFER IN TRANSMISSION LINES WITH CHARACTERISTIC IMPEDANCE Z_0	9
FIGURE 2.3 POWER TRANSFER IN TRANSMISSION LINES WITH SHORT AND OPEN CIRCUIT.....	10
FIGURE 2.4 S-PARAMETERS.....	11
FIGURE 2.5 SMITH CHART [29].....	12
FIGURE 2.6 1-DB COMPRESSION POINT.....	14
FIGURE 2.7 THIRD ORDER INTERCEPT POINT, IIP3.....	17
FIGURE 2.8 A FEW STAGES OF A RECEIVER FRONT END.....	20
FIGURE 2.9 HETERODYNE RECEIVER.....	21
FIGURE 2.10 HOMODYNE RECEIVER.....	22
FIGURE 2.11 LOW IF RECEIVER.....	23
FIGURE 2.12 OPERATION OF A MIXER.....	25
FIGURE 3.1 NYQUIST ADC.....	30
FIGURE 3.2 OVER-SAMPLING ADC.....	31
FIGURE 3.3 PROBABILITY DENSITY FUNCTION OF QUANTIZATION ERROR.....	33
FIGURE 3.4 POWER SPECTRAL DENSITY OF NOISE IN NYQUIST ADC.....	34
FIGURE 3.5(A). 3-BIT MID-RISE QUANTIZER. (B). QUANTIZATION ERROR SPECTRUM.....	35
FIGURE 3.6 POWER SPECTRAL DENSITY OF NOISE IN OVER-SAMPLING ADC.....	36
FIGURE 3.7 FIRST ORDER DELTA SIGMA MODULATOR.....	38
FIGURE 3.8 LINEAR MODEL OF FIRST ORDER DELTA SIGMA MODULATOR.....	39
FIGURE 3.9 LINEAR MODEL OF SECOND ORDER MODULATOR.....	42
FIGURE 3.10 N^{th} ORDER DELTA SIGMA MODULATOR.....	44
FIGURE 3.11 TWO-STAGE 1-1 MASH MODULATOR.....	46
FIGURE 3.12 CASCADED 2-1 THIRD ORDER FEEDBACK MODULATOR.....	48
FIGURE 3.13 CASCADED 2-1 THIRD ORDER FEED-FORWARD MODULATOR.....	53
FIGURE 4.1 FIRST ORDER SINGLE-BIT DELTA SIGMA MODULATOR.....	60
FIGURE 4.2 SECOND ORDER SINGLE-BIT DELTA SIGMA MODULATOR.....	61
FIGURE 4.3 SECOND ORDER MODULATOR WITH MULTI-BIT QUANTIZER.....	61
FIGURE 4.4 HIGHER ORDER SINGLE-BIT OR MULTI-BIT MODULATORS.....	62
FIGURE 4.5 CASCADED SINGLE-BIT DELTA SIGMA MODULATOR.....	63
FIGURE 4.6 CASCADED SINGLE-BIT HIGHER ORDER DELTA SIGMA MODULATOR.....	64
FIGURE 4.7 CASCADED MULTI-BIT HIGHER ORDER DELTA SIGMA MODULATOR.....	65
FIGURE 4.8 FEED-FORWARD ARCHITECTURE WITH FEEDBACK COEFFICIENTS.....	67
FIGURE 4.9 HYBRID FEED-FORWARD TOPOLOGY.....	68
FIGURE 4.10 SIMPLE FEED-FORWARD ARCHITECTURE.....	68
FIGURE 4.11 CASCADED THIRD-ORDER FEED-FORWARD DELTA SIGMA MODULATOR.....	69
FIGURE 4.12 DIGITAL ERROR CORRECTION.....	75
FIGURE 4.13(A) TESTING OF DELTA SIGMA MODULATOR. (B) SYSTEM DESIGN OF.....	77
FIGURE 5.1 MILLER COMPENSATED FULLY DIFFERENTIAL OTA.....	84
FIGURE 5.2 TELESCOPIC CASCODE OTA.....	85
FIGURE 5.3 FOLDED CASCODE OTA.....	86
FIGURE 5.4 (A) CONTINUOUS CMFB. (B) SENSE AMPLIFIER.....	88
FIGURE 5.5 SWITCHED CAPACITOR CMFB.....	89
FIGURE 5.6 (A) SAMPLING PHASE AND (B) INTEGRATION PHASE.....	91
FIGURE 5.7 OTA CAPACITIVE LOADING.....	96
FIGURE 5.8 FULLY DIFFERENTIAL COMPARATOR IN SWITCHED CAPACITOR INTEGRATOR.....	101
FIGURE 5.9 REGENERATIVE LATCH COMPARATOR.....	102
FIGURE 5.10 SWITCHED CAPACITOR INTEGRATOR.....	106
FIGURE 5.11 FLASH ANALOG-TO-DIGITAL CONVERTER.....	110
FIGURE 5.12 DIFFERENTIAL DIGITAL-ANALOG-DIGITAL (DAC/ADC) CONVERTER.....	111
FIGURE 5.13 A NOVEL NMOS-PMOS THERMOMETER-TO-BINARY CONVERTER.....	113
FIGURE 6.1 COMMERCIALLY IMPLEMENTED FULLY DIFFERENTIAL 1-BIT DAC.....	115
FIGURE 6.2 FULLY DIFFERENTIAL 1-BIT DAC WITH DUAL POLARITY REFERENCE VOLTAGES.....	117

FIGURE 6.3 NON-OVERLAPPING CLOCKS.....	123
FIGURE 6.4 NTF OF THE SECOND ORDER FEED-FORWARD MODULATOR.....	126
FIGURE 6.5 STABILITY OF SECOND ORDER FEED-FORWARD MODULATOR.....	127
FIGURE 6.6 SECOND ORDER FEED-FORWARD MODULATOR.....	128
FIGURE 7.1 MODELING OF SAMPLING JITTER.....	131
FIGURE 7.2 EFFECT OF SAMPLING JITTER ON SNR.....	133
FIGURE 7.3 MODELING OF THERMAL NOISE kT/C	134
FIGURE 7.4 EFFECT OF kT/C ON NOISE POWER.....	134
FIGURE 7.5 MODELING NOISE SOURCES IN IDEAL MODULATOR.....	135
FIGURE 7.6 NON-IDEAL CASCADED THIRD ORDER FEED-FORWARD MODULATOR INCLUDING FINITE DC-GAIN, FINITE SLEW-RATE AND FINITE GAIN-BANDWIDTH.....	137
FIGURE 7.7 EFFECT OF FINITE SLEW-RATE ON SNDR.....	137
FIGURE 7.8 EFFECT OF FINITE DC GAIN ON THE NOISE POWER.....	138
FIGURE 8.1 CASCADED FEED-FORWARD THIRD ORDER (2-1) MODULATOR.....	140
FIGURE 8.2(A) TIME DOMAIN OUTPUT OF FIRST INTEGRATOR OUTPUT.....	141
FIGURE 8.2(B) OUTPUT DISTRIBUTION OF THE FIRST INTEGRATOR.....	141
FIGURE 8.3(A) TIME DOMAIN OUTPUT OF SECOND INTEGRATOR.....	142
FIGURE 8.3(B) OUTPUT DISTRIBUTION OF THE SECOND INTEGRATOR.....	142
FIGURE 8.4(A) TIME DOMAIN OUTPUT OF THIRD INTEGRATOR.....	143
FIGURE 8.4(B) OUTPUT DISTRIBUTION OF THE THIRD INTEGRATOR.....	144
FIGURE 8.5 TIME DOMAIN OUTPUT OF THE DESIGNED SECOND ORDER MODULATOR.....	144
FIGURE 8.6 TIME DOMAIN OUTPUT OF THE DESIGNED FIRST ORDER MULTI-BIT MODULATOR.....	145
FIGURE 8.7 DIGITAL NOISE CANCELLATION LOGIC.....	145
FIGURE 8.8 PSD OF THE DESIGNED CASCADED THIRD ORDER FEED-FORWARD DELTA SIGMA MODULATOR.....	147
FIGURE 8.9 SNR, SNDR WITH RESPECT TO VARIOUS AMPLITUDES AT FIXED FREQUENCY.....	148
FIGURE 8.10 FREQUENCY DOMAIN OF THE QUANTIZATION NOISE WHEN MODULATOR.....	149
FIGURE 8.11 FREQUENCY DOMAIN OF THE QUANTIZATION NOISE WHEN MODULATOR.....	150
FIGURE 8.12 TIME DOMAIN OUTPUT OF THE IMPLEMENTED SECOND ORDER MODULATOR.....	151
FIGURE 8.13 TIME DOMAIN OUTPUT OF THE IMPLEMENTED FIRST ORDER MODULATOR.....	151
FIGURE 8.14 INTERDIGITATION.....	153
FIGURE 8.15 MATCHING AND INTERDIGITATION OF TRANSISTORS.....	153
FIGURE 8.16 CENTROID ARRANGEMENT OF SEVEN PASS-GATES AND COMPARATORS.....	154
FIGURE 8.17 PHYSICAL LAYOUT OF CASCADED FEED-FORWARD THIRD ORDER MODULATOR.....	156
FIGURE 8.18 PSD OF THE IMPLEMENTED CASCADED FEED-FORWARD DELTA SIGMA MODULATOR.....	156
FIGURE A.1 FLASH ADC. [26].....	165
FIGURE A.2 TWO-STEP FLASH ADC.....	166
FIGURE A.3 PIPELINE ADC [26].....	167
FIGURE A.4 SUCCESSIVE APPROXIMATION (SAR) ADC.....	167
FIGURE A.5 R-2R DAC.....	169
FIGURE A.6 CHARGE SCALING DAC.....	170
FIGURE B.1 OFFSET ERROR OF A 3-BIT DAC.....	172
FIGURE B.2 DNL FOR A 3-BIT DAC.....	173
FIGURE B.3 INL FOR A 3-BIT DAC.....	174
FIGURE C.1 DATA SPECTRUM.....	181
FIGURE C.2 FFT SPECTRUM OF SECOND ORDER MODULATOR.....	181
FIGURE C.3 FFT SPECTRUM OF FIRST ORDER MODULATOR.....	182
FIGURE C.4 POWER SPECTRUM OF SIGNAL TO NOISE PLUS DISTORTION.....	182
FIGURE D.1 MULTI-BIT FIRST ORDER DELTA SIGMA MODULATOR.....	183
FIGURE D.2 FEED-FORWARD SECOND ORDER MODULATOR.....	184
FIGURE D.3 A 3-BIT ADC AND THERMOMETER-TO-BINARY ENCODER.....	185
FIGURE D.4 A 3-BIT ADC, THERMOMETER-TO-BINARY ENCODER AND DAC.....	186
FIGURE D.5 A 3BIT DAC.....	187
FIGURE D.6 FIRST STAGE OP-AMP.....	188
FIGURE D.7 SECOND AND THIRD STAGE OP-AMP.....	189
FIGURE D.8 COMPARATOR.....	190
FIGURE D.9 COMPARATOR WITH PASS-GATES.....	191

FIGURE D.10 NON-OVERLAPPING CLOCKS.	192
FIGURE D.11 COMMERCIALY IMPLEMENTED 1-BIT DAC.	193
FIGURE F.1 FOLDED CASCODE OTA DC GAIN.	198
FIGURE F.2 SLEW-RATE OF FOLDED CASCADE OTA.	199
FIGURE F.3 DC RESPONSE OF THE FOLDED CASCADE OTA.	200
FIGURE F.4 DC CURRENTS IN OTA.	201
FIGURE F.5 UNITY GAIN BANDWIDTH AND PHASE MARGIN OF THE OTA.	202
FIGURE F.7 LINEAR OUTPUT SWING OF THE FOLDED CASCODE OTA.	204
FIGURE F.8 WIDE SWING CURRENT MIRROR.	205
FIGURE F.9 DNL OF THE 3-BIT DAC.	206
FIGURE F.10 INL OF THE 3-BIT DAC.	206
FIGURE F.11 RESPONSE OF A SWITCHED CAPACITOR INTEGRATOR.	207
FIGURE G.1 DIE LAYOUT OF SECOND-ORDER MODULATOR, INTEGRATOR, OP-AMP.	211

LIST OF TABLES

Table 5.1 Transistor sizes of designed folded cascode OTA.....	99
Table 5.2 Results of the designed folded cascode OTA.....	100
Table 5.3 Results of the designed folded cascode OTA.....	101
Table 8.1 Summary of the cascaded feed-forward 2-1 delta sigma modulator.....	158
Table 8.2 Comparison of low-pass delta sigma modulators in terms of FOM.....	159
Table 8.3 Comparison of low-pass delta sigma modulators in terms of area.....	161
Table G.1 Pin arrangements for physical IC layout.....	210
Table G.2 Bias voltages of the operational amplifier.....	211

1 INTRODUCTION

There has been a resurgence of integrated radio frequency (RF) transceivers due to renewed interest in wireless applications. The cost-effective and portable nature of RF systems has increased consumer demands. RF systems find themselves in both security related and commercial applications. Mobile phones, RF ID, Wireless LAN, and GPS are some of the RF applications. There is a continuing need to develop efficient integrated RF architectures that provide low cost, low power, and high performance. Analog-based architectures have several disadvantages such as lack of integrability, mismatch of gain, amplitude and phase between analog components, noise sensitivity, and limitations of analog circuits [33]. The existing solutions for RF applications are inefficient in terms of power and noise; and in addition, have integrability issues. Digital receiver technology is rapidly replacing many of traditional analog techniques for reception of RF signals. For digital receivers to provide high performance compared to their analog counterparts there is a need to design high performance analog-to-digital converters (ADC). High speed, low power, high resolution, and small area are some of the desired qualities of a high performance ADC. There is always a trade off between power and speed and it is difficult to obtain all the desired qualities in a single ADC. Therefore, ADCs are major bottlenecks in obtaining high performance receivers. Advances in ADC implementation are important because a high performance ADC can relax the stringent requirements not only on the RF front end but also on the digital signal

processing section of the receiver. The goal of this project is to design a highly efficient ADC that meets the specifications of high performance receivers.

1.1 Current research in RF Wireless Receivers and ADC

Current research performed in the field of wireless design attempts to realize highly adaptive RF architectures that incorporate low cost, low power, low noise, and high speed [46]. Some of the research areas under investigation are studies of lower cost silicon technology, low power consumption, development of high speed systems by pushing the capacity and data rates, and adaptive architectures for multiple RF standards such as GSM, DECT, CDMA, and WCDMA [29, 33].

The strict requirements on RF front end components have captured a great deal of attention [52]. The design of such components as the low noise amplifier (LNA), mixer and voltage controlled oscillator (VCO) is continuously improved to obtain high gain and low noise performance. Differential LNA and double balanced mixers have provided solutions to many of the problems faced by RF designers [30]. Narrow-band and wideband VCO have also populated the RF market. A high performance analog-to-digital converter, mismatch of gain, amplitude, and phase between analog components, noise sensitivity, selectivity, accuracy and stability of analog circuits are still some of the major bottlenecks in RF design which are yet to be overcome. In my opinion, the way to improve the design of receivers is to use high speed, low power, low noise ADCs; and thereby, reduce the number of stages of RF front end. The ADC should be moved towards the antenna in receiver architectures so that these bottlenecks can be overcome by high precision digital circuits. The idea is to convert the analog signal to digital signal

as quickly as possible so that advantages of low power, high precision digital circuits can be utilized. Although substantial research is performed on the RF front-end section, a lot is required of the mixed signal section of the wireless receiver. Serious efforts have been made over the past decade to improve the performance of ADCs [1-7]. These data converters have a single stage and are not efficient in providing enough resolution at high speeds. The single stage data converters were replaced by multi-stage or cascaded modulators [9, 11-15]. These modulators provided high resolution but were not suitable for wide-bandwidth applications. The MASH modulators [16-22] have very high resolution and wide-bandwidth but suffer from high power consumption. With the advent of very low sub-micron technology ($0.18\mu\text{m}$ or less), recent research in ADC has gained strength and high performance ADCs have been designed [46, 48, 60-63]. There is still an area for improvement in designing low power and hardware efficient ADCs with sampling rates above 80 MHz.

1.2 Dissertation Organization

This dissertation introduces a novel delta sigma analog-to-digital converter for high speed, low power, and low noise RF wireless applications. The dissertation is divided into the following chapters. Chapter 2 gives an overview of the fundamentals of RF circuits and systems required for designing wireless applications. Some of the RF wireless architectures and standards are also presented. Chapter 3 describes the Nyquist and over-sampling data converters. Brief information on finding the signal-to-noise (SNR) ratio or resolution of these modulators is given. New equations to obtain appropriate coefficients for scaling the gain and shaping the quantization noise of

feedback and feed-forward delta sigma modulators are derived. These coefficients are incorporated in design and implementation of the proposed delta sigma data converter. Chapter 4 reviews possible architectures of delta sigma modulators, which are further classified into feed-back and feed-forward modulators. A linear system of the proposed ADC is presented along with its advantages over other architectures. Chapter 5 deals with integrated circuits that are required to design data converters. A complete description of designed circuits such as operational amplifiers, comparators, switched capacitor integrators, Nyquist analog-to-digital and digital-to-analog converter is presented. This chapter also presents some of the non-idealities that occur in these electronic circuits. Some key aspects for implementation of the proposed delta sigma modulator are mentioned in Chapter 6. These aspects cover important information that should be taken into account before physical chip implementation. Modeling of the proposed cascaded third order feed-forward delta sigma data converter is obtained using Simulink and Matlab in Chapter 7. In this chapter, non-idealities like finite slew-rate, finite gain, finite unity gain-bandwidth, thermal and op-amp noise, and sampling jitter are gradually introduced into an ideal cascaded third order delta sigma data converter and their effects on the SNR or resolution is documented. The non-idealities modeled in Matlab are based on the actual non-idealities encountered during the design of the modulator in Cadence. Chapter 8 presents the results obtained from design simulations and extraction of the physical chip layout of the proposed data converter in terms of resolution, speed, area, and power consumption. A brief discussion on quantization noise is given. This chapter also provides a classical approach to laying out analog and mixed signal circuits with a few illustrations. The proposed delta sigma ADC is

compared with recent data converters in terms of their area and figure of merit (FOM), which is a parameter typically used to obtain the performance of the data converters with respect to power, resolution, and data output rate (DOR). A conclusion and novel contribution advancing the state-of-art technology are provided in the final chapter with emphasis on future work.

Appendix A contains an overview of Nyquist analog-to-digital and digital-to-analog converters. Appendix B includes the static and dynamic parameters that define the performance of the data converters. The results and Matlab algorithm of the linear system described in Chapter 4 can be found in Appendix C. Appendix D has the layout of the final modulator and its circuit components. The Matlab functions for modeling non-idealities in Simulink blocks and for designing noise transfer function (NTF) are available in Appendix E. Appendix F has a snapshot of some of the simulation results of key design components like operational amplifiers, digital-to-analog converter (DAC), and switched capacitor integrator. Appendix G provides a procedure for testing the physical layout of the ADC.

1.3 Applications

RF wireless systems have several applications serving different needs. Some of these applications of wireless receivers along with their purposes are given below [29]:

1. Wireless Local Area Networks (WLANs)

Operating frequency: 900MHz, 2.4GHz bands

Purpose: To provide wireless connectivity in offices, hospitals, factories, etc.

2. Global Positioning System (GPS)

Operating frequency: 1.5GHz band

Purpose: To determine geographic location with usage in automobile industry.

3. RF Identification Systems (RF IDs)

Operating frequency: 900MHz, 2.4GHz bands

Purpose: small, low cost tags attached to objects for tracking their position.

4. Mobile Phones for GSM, CDMA, UMTS

Operating frequency: GSM (800 MHz), CDMA (900, 1900 MHz), UMTS (2100 MHz)

Purpose: commercial wireless telephones

1.4 Originality

The main focus of this research is to develop a highly efficient high speed (ADC) for CMOS receiver. The mixed signal ADC should have attributes such as small size, low power, and high resolution. The power and area of the proposed ADC is reduced by using a second order feed-forward modulator instead of the conventional feedback modulator. A feed-forward modulator has only one DAC in the feed-back path that not only reduces hardware complexity but also minimizes the total area and power. The 12-bit resolution is obtained by cascading the feed-forward modulator with a multi-bit first order modulator. The multi-bit first order modulator consists of a flash ADC incorporating a novel low power, small-sized and high speed thermometer-to-binary encoder [65]. This original architecture provides an effective way of improving the resolution of high speed ADCs without consuming more area and power.

2 FUNDAMENTALS OF RF DESIGN

This chapter deals with the fundamentals of radio frequency (RF) integrated circuits. The importance of a RF front end, transmission lines, and matching networks are discussed. The parameters used to measure the RF signal and the problems associated with the design of RF systems are presented. An overview of different types of RF architectures along with the current wireless standards is also given.

Due to path loss, envelope fading, and additive white gaussian noise (AWGN) the amplitude of the RF signal from the antenna is considerably degraded. We need a certain amount of signal power at the input of the demodulator to receive the transmitted input signal [29]. If there is no front-end, we cannot achieve this signal power and the signal gets embedded in noise. Thus a front end is needed to boost the signal power and remove noise. The wavelength of a traveling signal is defined by equation (2.1).

$$\text{Wavelength} = \text{Speed of light} / \text{input signal frequency} \quad (2.1)$$

For RF at low frequencies, the relationship between wavelength and length of the wire carrying the signal is given by equation (2.2).

$$\text{Wavelength} \gg \text{length of the wire} \quad (2.2)$$

The measured voltage and current are not dependent on the position along the wire. The current travels down wires easily for efficient power transmission. For RF at high frequencies, the relationship between wavelength and transmission wire length is given by equation (2.3).

Wavelength \ll length of the wire (2.3)

There is a need of transmission lines for efficient power transmission of the high frequency signals. The envelope voltage, dependent on the position along the transmission line, is a reliable signal attribute because it is constant along a lossless transmission wire. RMS voltage and current can be extracted directly from RF signal power.

2.1 Transmission lines

The fundamental parameter of a transmission line is its characteristic impedance Z_0 . Impedance describes the relationship between the voltage and current of the propagated signal. It is a function of physical dimensions and the dielectric constant. Z_0 is usually defined as real impedance (e.g. 50 or 75 ohms) [32].

For a loss-less transmission line:

$$Z_0 = \sqrt{\frac{L}{C}} \quad (2.4)$$

where L is the distributed inductance of the line

and C is the distributed capacitance of the line.

2.1.1 Power transfer efficiency in transmission lines

For complex frequencies, power is efficiently transferred over transmission lines when $Z_L = Z_0$ as can be seen from Figure 2.1.

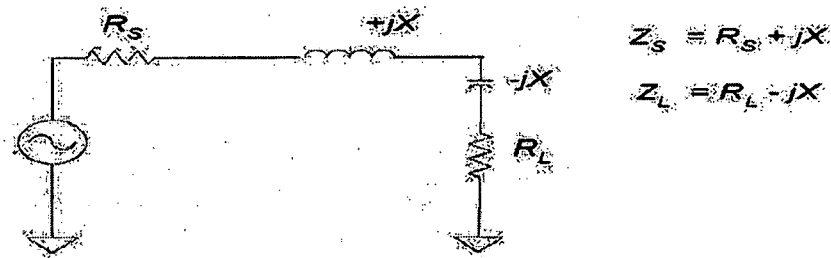


Figure 2.1 Power transfer efficiency with $Z_L = Z_s^*$.

At high frequencies [30], maximum power is transferred when $R_s = R_L = Z_0$. As can be seen from the Figure 2.2 a transmission line with termination impedance Z_0 has no reflected power. All the signal power is absorbed by the load leading to maximum power transfer efficiency.

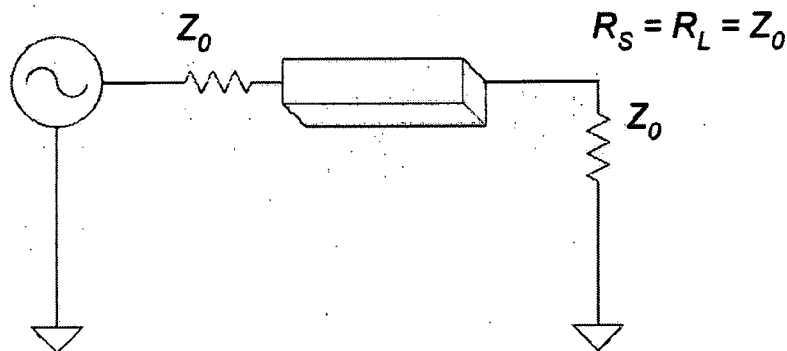


Figure 2.2 Power transfer in transmission lines with characteristic impedance Z_0 .

When a transmission line is terminated with a short circuit, the incident signal is reflected with a 180° phase shift. If a transmission line is terminated with an open circuit, the incident signal is reflected with no phase shift. This phenomenon is depicted in Figure 2.3. For the transmission line terminated by short, full power is reflected to the source.

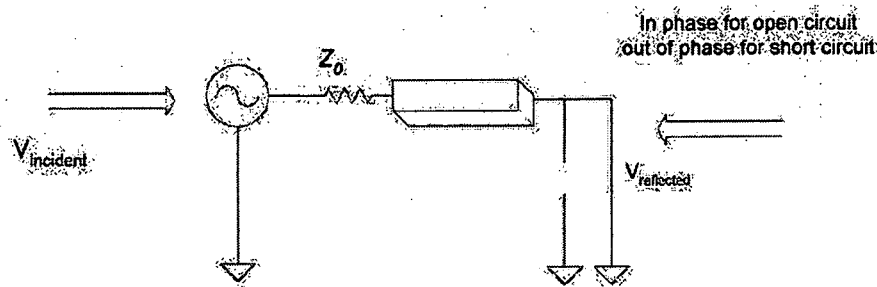


Figure 2.3 Power transfer in transmission lines with short and open circuit.

2.2 Input and Output Matching Networks

Matching networks, consisting of strip-lines, resistors, capacitors, and inductors are primarily used to achieve the following objectives [30]:

1. They preserve the frequency response of the circuits by providing proper termination.
2. The input matching network not only provides optimum noise performance and stability at the input but also provides matching of input impedance.
3. The output matching network ensures stability at the output.
4. In order to match power or efficiently transfer power from the input to the output, matching of input impedance and output impedance is carried out by input and output matching networks.

2.2.1 S-Parameters

S-parameter-based analysis is used when the signals at high frequencies are used and power becomes a primary variable of measurement for these signals. *S*-parameters are relatively easy to obtain at high frequencies. They relate easily to familiar measurements such as gain, loss, reflection coefficient. *S*-parameters of multiple devices can be cascaded to predict system performance. On the other hand, lumped parameter models,

represented by short and open circuit conditions, are difficult to obtain at high frequencies. In addition, high frequency transistors are susceptible to oscillations under open loop and closed loop conditions [30]. The four different S -parameters are given below and shown in Figure 2.4

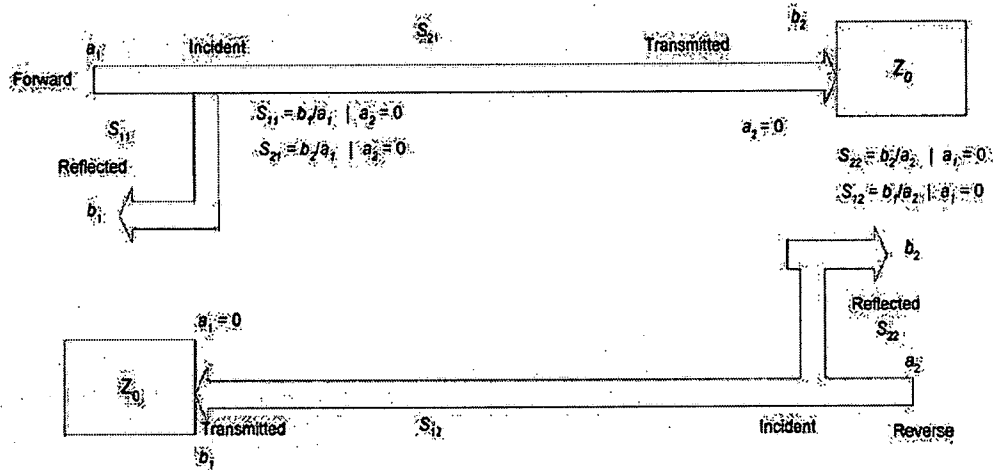


Figure 2.4 S -parameters.

Where,

S_{11} = forward reflection coefficient (*input match*)

S_{22} = reverse reflection coefficient (*output match*)

S_{21} = forward transmission coefficient (*gain or loss*)

S_{12} = reverse transmission coefficient (*isolation*)

2.2.2 Smith Chart

The Smith chart is a polar representation of the complex reflection coefficient known as the 1-port scattering parameter S or S_{11} , for reflections from a normalized complex load impedance $Z = r + jx$. The Smith chart relates polar reflection coefficient Γ to the normalized load impedance Z_L/Z_0 that causes the reflection, and also to the distance we

are from the load in terms of the wavelength of the transmitted signal waves [29]. The normalized impedance is a ratio of the actual load impedance Z_L and the characteristic impedance Z_0 of the transmission line. As can be seen from Figure 2.5, the contours of $z = r + jx$ are mapped on top of this polar reflection coefficient Γ . The center of the Smith chart is at $\Gamma = 0$, which is where the normalized load impedance $z = 1 + j0$. The resistive part of the load impedance Z_L equals the characteristic impedance of the transmission line, and the reactive part of the load impedance is zero. This suggests that the transmission line is matched.

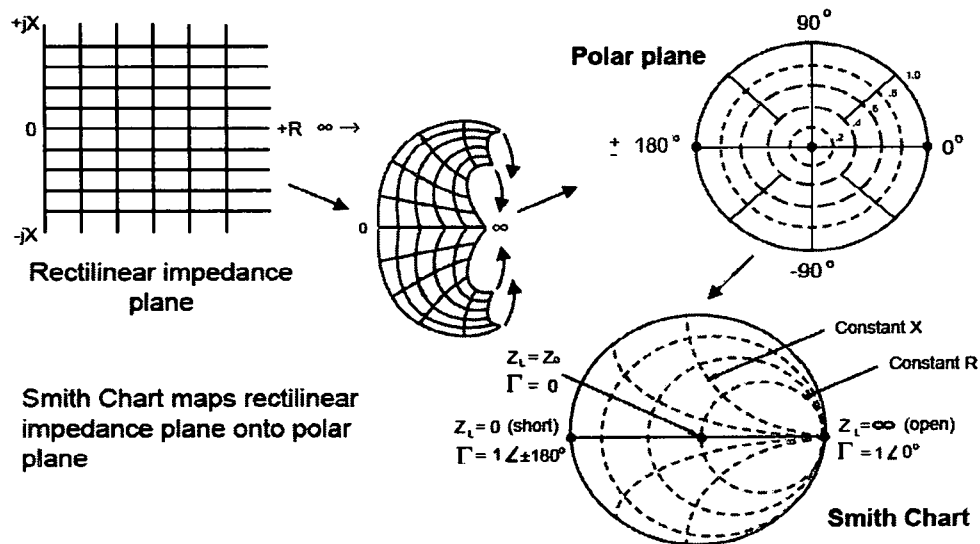


Figure 2.5 Smith chart [29].

2.3 Problems associated with RF design

Consider a nonlinear, memory-less, time-variant system $y(t) = f(x(t))$ which can be modeled by Taylor's series (consider only the first three terms). This Taylor series is represented by equation (2.5). All the parameters that affect the linearity in the system are derived from this model equation.

$$y(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) \quad (2.5)$$

2.3.1 Selectivity

Selectivity is defined as the quality of reception of signal amplitude amidst nonlinear signals like interferers, blockers, and unwanted harmonics. The following terms are related to the selectivity in RF signals.

2.3.1.1 Harmonic Distortion

If a sinusoidal input signal is applied at the input, frequency components are present at multiples of the fundamental frequency of the sinusoidal input signal. These frequency components, termed as harmonics, are created by the non-linearity in the input signals. The harmonic distortion is defined as a ratio of the amplitude of a particular harmonic to the amplitude of the fundamental signal [30]. The harmonic distortion is given by equation (2.6).

if $x(t) = A \cos(\omega t)$

$$\begin{aligned} y(t) &= \alpha_1 A \cos \omega t + \alpha_2 A^2 \cos^2 \omega t + \alpha_3 A^3 \cos^3 \omega t \\ &= \alpha_1 A \cos \omega t + \alpha_2 \frac{A^2}{2} (1 + \cos 2\omega t) + \alpha_3 \frac{A^3}{4} (3 \cos \omega t + \cos 3\omega t) \\ &= \alpha_2 \frac{A^2}{2} + \left(\alpha_1 A + 3\alpha_3 \frac{A^3}{4} \right) \cos \omega t + \alpha_2 \frac{A^2}{2} (\cos 2\omega t) + \alpha_3 \frac{A^3}{4} (\cos 3\omega t) \\ &= \alpha_2 \frac{A^2}{2} + A_1 \cos \omega t + A_2 (\cos 2\omega t) + A_3 (\cos 3\omega t) \end{aligned} \quad (2.6)$$

Where, A is the amplitude of the fundamental input signal,

A_1 is the gain of the system,

A_2 is amplitude of the first harmonic,

A_3 is the amplitude of the second harmonic.

2.3.1.2 Gain Compression

When the input signal to an amplifier stage is large, the amplifier saturates, hence clipping the signal. When the strength of the input signal is further increased, output signal is no longer amplified but starts attenuating. The output is said to be compressed [31].

Neglecting the higher order harmonics equation (2.6) becomes:

$$y(t) = \alpha_2 \frac{A^2}{2} + \left(\alpha_1 A + 3\alpha_3 \frac{A^3}{4} \right) \cos \omega t \quad (2.7)$$

The gain of the system is given by equation (2.8):

$$A_s = \alpha_1 A + 3\alpha_3 \frac{A^3}{4} \quad (2.8)$$

For small amplitude A , the small signal gain is α_1 . When input signal amplitude A increases, the gain begins to decrease, and the second term starts to dominate. The output gain decreases rapidly for high input levels.

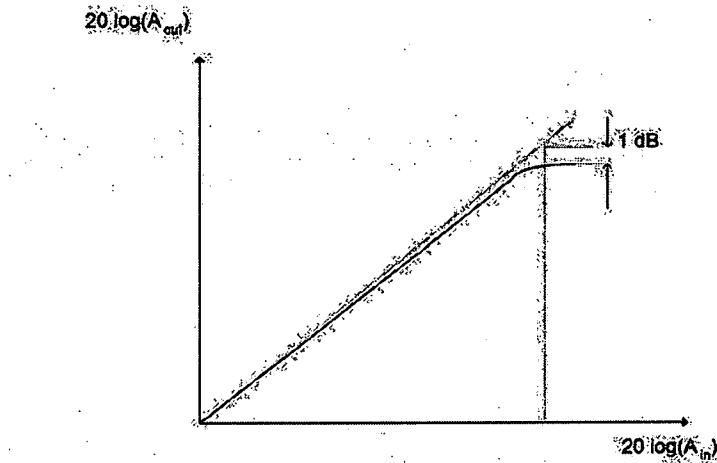


Figure 2.6 1-dB compression point.

This effect is quantified by the “1-dB compression point” (1-dBCP), the input signal level for which the small signal gain drops by 1 dB. This is illustrated by equation (2.9) and Figure 2.6.

$$20 \log |\alpha_1| - 1 \text{ dB} = 20 \left| \alpha_1 + \frac{3}{4} \alpha_3 A_{1-\text{dB}}^2 \right| \quad (2.9)$$

2.3.1.3 Desensitization and Blocking

When a weak desired signal undergoes amplification in the presence of a strong interferer the small signal gain α_1 is reduced by the interferer A_0 and the receiver is said to be desensitized [32]. The desensitization of the input signal is given in equation (2.10), where B_1 completely dominates the gain α_1 . Consider a input signal $x(t)$ as a combination of a desired signal A and a strong interferer A_0 present at the input:

$$\begin{aligned} \text{if } x(t) &= A \cos(\omega_1 t) + A_0 \cos(\omega_2 t) \\ y(t) &= \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) \\ &= \left(\alpha_1 A + \frac{3}{4} \alpha_3 A^3 + \frac{3}{2} \alpha_3 A A_0^2 \right) \cos \omega_1 t + \dots \\ &= \left(\alpha_1 A + \frac{3}{2} \alpha_3 A A_0^2 \right) \cos \omega_1 t + \dots \\ &= (B_0 + B_1) \cos \omega_1 t + \dots \end{aligned} \quad (2.10)$$

The gain decreases as B_1 increases. For large B_1 , the gain B_0 drops to zero and the signal is blocked. In RF design, blocking signals are referred to as interferers that desensitize a circuit. RF receivers should have the capability of withstanding blocking signals 60 to 70 dB greater than the desired signal.

2.3.1.4 Inter-modulation (IM)

Inter-modulation arises when more than one tone is present at the input signal. The inter-modulation effect is modeled using the “two tone” test as described in equation (2.11)

[30]. Consider a input signal $x(t)$ as a combination of two strong interferers A_1 and A_2 present at the input. We will use the same non-linear model equation given in equation (2.6) for the output.

$$\begin{aligned}
 \text{if } x(t) &= A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t) \\
 y(t) &= \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) \\
 &= \alpha_1 (A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t)) + \alpha_2 (A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t))^2 \\
 &\quad + \alpha_3 (A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t))^3
 \end{aligned} \tag{2.11}$$

After expanding and solving we obtain the following frequencies given in equations (2.12), (2.13), and (2.14).

$$\begin{aligned}
 \text{At } \omega_1: & \left(\alpha_1 + \frac{3}{4} \alpha_3 A_1^2 + \frac{3}{2} \alpha_3 A_2^2 \right) A_1 \cos \omega_1 t \\
 \text{At } \omega_2: & \left(\alpha_1 + \frac{3}{4} \alpha_3 A_2^2 + \frac{3}{2} \alpha_3 A_1^2 \right) A_2 \cos \omega_2 t
 \end{aligned} \tag{2.12}$$

Second order terms:

$$\begin{aligned}
 \text{At } 2\omega_1, 2\omega_2: & \left(\frac{1}{2} \alpha_2 A_1^2 \right) \cos 2\omega_1 t, \left(\frac{1}{2} \alpha_2 A_2^2 \right) \cos 2\omega_2 t \\
 \text{At } \omega_1 \pm \omega_2: & \left(\alpha_2 A_1 A_2 (\cos(\omega_1 + \omega_2)t) \right) + \left(\cos(\omega_1 - \omega_2)t \right)
 \end{aligned} \tag{2.13}$$

The third-order inter-modulation (IM3) terms are at

$$2\omega_1 - \omega_2, 2\omega_2 - \omega_1 \tag{2.14}$$

If the difference between ω_1 and ω_2 is small, the IM3 components consisting of the following two frequencies $2\omega_1 - \omega_2, 2\omega_2 - \omega_1$ are in the vicinity of ω_0 , which is the fundamental frequency, and the signal is corrupted due to the two strong interferers. To filter them out, very narrow-band filters are required. To measure the distortion due to nonlinearity, the ratio of the amplitude of the IM3 terms to the amplitude of the

fundamental signal, called the third order IM distortion, is calculated. Reducing $2\omega_1 - \omega_2$, $2\omega_2 - \omega_1$ by keeping the nonlinearity down is the only solution to the problem.

2.3.1.5 Third Order Intercept point, IIP3

The amplitude of the fundamental frequency signal increases in proportion to A ($\sim \alpha_1 A$) whereas that of the IM3 terms increase in proportion to A^3 ($\sim 3 \alpha_3 A^3/4$). The power level of the IM3 products increase three times the rate at which the desired signal increases [32]. IIP3 is the signal level at which the amplitude of the IM3 would become equal to that of the fundamental signal. A plot for IIP3 is shown in Figure 2.7.

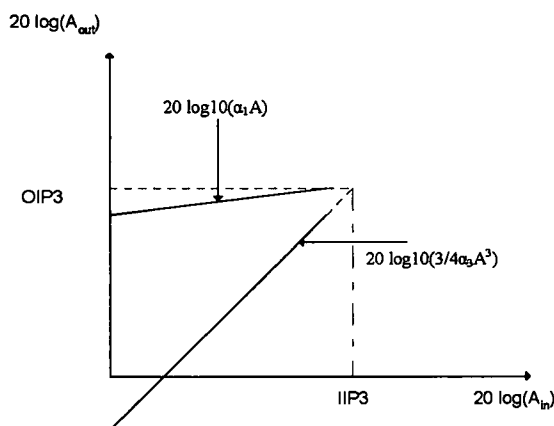


Figure 2.7 Third order intercept point, IIP3.

2.3.2 Sensitivity

Sensitivity is the minimum signal power applied to the receiver input terminals that yields the required signal-to-noise ratio [31]. The following terms concern the sensitivity of the signal.

2.3.2.1 Thermal Noise

Thermal noise arises due to random motion of thermally agitated electrons in resistor devices. Thermal noise exists even though the resistor is not connected and no current is flowing through it. It is generally modeled by a voltage source in series or a current source in parallel and its power spectral density (PSD) given by equation (2.15).

$$V_n^2 = 4kTR\Delta f \quad (2.15)$$

Where, k is the Boltzmann constant,

V_n^2 is the mean square noise voltage,

R is the resistance,

T is the temperature in Kelvin,

Δf is desired frequency bandwidth.

2.3.2.2 Shot Noise (Schottky Noise)

In MOS devices the shot noise of the very small gate leakage current can be neglected.

The shot noise is given by equation (2.16).

$$I_n^2 = 2qI_{DC}\Delta f \quad (2.16)$$

Where, I_n^2 is the mean square noise voltage,

q is the electron charge,

I_{dc} is the current in amperes,

Δf is desired frequency bandwidth.

2.3.2.3 Flicker Noise (1/f Noise)

Flicker noise is defined as random trapping of charge at oxide interface of MOS transistors. Flicker noise is modeled by a noise current source with a spectral density given by equation (2.17).

$$I_n^2 = \frac{K g_m^2}{f W L C_{ox}^2} \Delta f \quad (2.17)$$

Where, I_n^2 is the mean square noise voltage;

K is mobility constant;

g_m , W , L are the transconductance, width and length of the MOS transistor;

Δf is the desired frequency bandwidth with f being the frequency of operation.

At high frequency, flicker noise may be neglected. However in mixers and oscillators the $1/f$ -shaped spectrum can be translated to the desired signal range for direct conversion receivers.

2.3.2.4 Noise Figure

Noise figure (NF) is a parameter that measures the additive noise inherent in a system. It is often specified for a 1-dB bandwidth [29] as given in equation (2.18).

$$\begin{aligned} \text{Noise Figure} &= \frac{\text{Total noise power at the output}}{\text{Total noise power due to input sources}} \\ \text{Noise Factor} &= \frac{\text{SNR}_{\text{in}}}{\text{SNR}_{\text{out}}} \\ \text{Noise Figure} &= 10 \log_{10}(\text{Noise Factor}) \end{aligned} \quad (2.18)$$

Noise figure or noise factor measures the SNR degradation as a signal passes through a system. If there is no noise present, then $NF = 1$. In reality, the finite noise of a system degrades the SNR , yielding $NF > 1$.

The NF of cascaded stages is stated in equation (2.19).

$$NF_{total} = 1 + (NF_1 - 1) + \frac{NF_2 - 1}{P_1} + \dots + \frac{NF_m - 1}{P_1 P_2 P_{(m-1)}}$$

$$\text{Power gain} = P = \frac{\text{Output Power}}{\text{Power at input source}} \quad (2.19)$$

Figure 2.8 shows the figure of first few stages of a receiver front end. NF of next stage is calculated with respect to the power gain of the previous stage as given in equation (2.19). The noise contributed by each stage decreases as the gain of the preceding the stage increases. The first few stages in a cascade are the most critical [30] as given by equation (2.20).

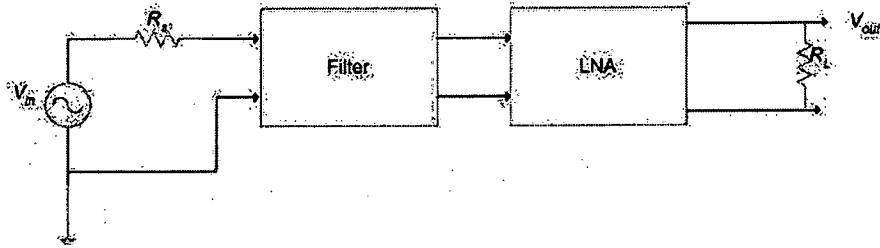


Figure 2.8 A few stages of a receiver front end.

$$NF_{Filter} = L$$

$$NF_{total} = 1 + (NF_{Filter} - 1) + \frac{NF_{LNA} - 1}{A_{p,Filter}} = N_{Filter} + \frac{NF_{LNA} - 1}{L^{-1}} = L + (NF_{LNA} - 1)L$$

$$= NF_{LNA}L \quad (2.20)$$

2.4 Receiver Architectures

In this section, receiver architecture such as heterodyne, homodyne, and low-IF will be reviewed. A working principle for each of the receivers is mentioned and their advantages and disadvantages are stated. The heterodyne receiver has relaxed

specifications and high performance but is not suitable for system-on-chip (SOC) applications whereas other receivers like homodyne and low-IF suit these applications.

2.4.1 Heterodyne Receiver

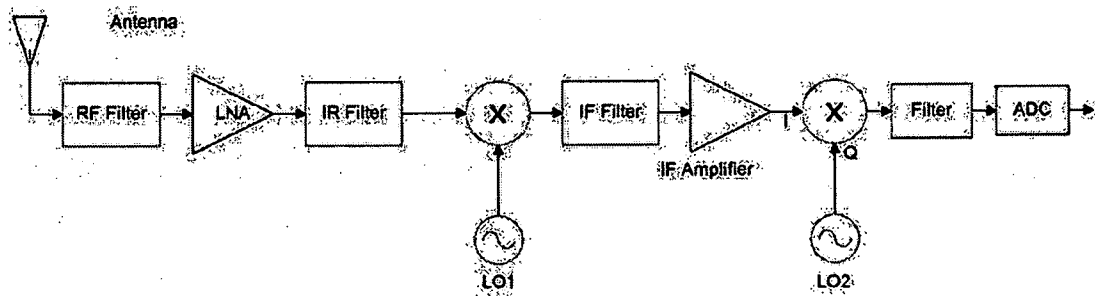


Figure 2.9 Heterodyne receiver.

A heterodyne receiver is shown in figure 2.9. The RF filter selects the band of interest while providing some image rejection. The signal is then amplified by a low noise amplifier (LNA). The image signal formed during mixing is rejected by image rejection (IR) filter before it is formed. The first mixer and local oscillator (LO1) translate the RF frequency signal and the adjacent interferers to intermediate frequency (IF) signal. The desired channel selection is performed by the IF filter. After IF filtering, signal is further amplified by the variable gain IF amplifier (VGA) to increase the strength of the signal. The second mixer and local oscillator (LO2) performs the base-band down-conversion by employing in-phase and quadrature phase (I/Q) demodulation techniques. After suitable low-pass filtering to remove the undesired spurious at the mixers output, the signal is digitally converted by an analog-to-digital converter (ADC) and fed to the digital signal processor (DSP). The Heterodyne architecture has the following attributes and disadvantages [33].

1. Strengths: good sensitivity, selectivity, relaxed specs for analog circuits after the IF, simple ADC.
2. Drawbacks: image problem, expensive filters, not integrable, increased power consumption, complex, I/Q mismatch due to mismatch in gain, phase and amplitude of analog components.

2.4.2 Homodyne Receiver

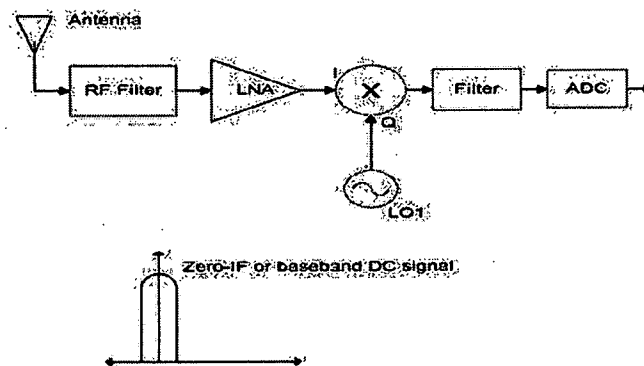


Figure 2.10 Homodyne receiver.

In direct conversion or homodyne receivers [34] shown in Figure 2.10, the RF spectrum or the input signal is simply translated to base-band (DC) in the first down-conversion. In order to achieve zero IF or base-band signal, we set the RF and LO at the same frequencies as shown in equation (2.21).

$$\omega_{RF} = \omega_{LO} (\omega_{IF} = 0) \quad (2.21)$$

The channel selection requires only a low-pass filter with relatively sharp cutoff characteristic. Because there is a direct down-conversion to base-band spectrum, the image problem is circumvented. The RF filter, IF amplifier, IF filter, and the second mixer in the heterodyne architecture are replaced by low-pass filters and base-band

amplifiers in the homodyne architecture. This makes the architecture integrable on a single chip. The strengths and drawbacks of this architecture are given below [35].

1. Strengths: very compact & simple, integrable, no image rejection needed, multi-standard, simple ADC
2. Drawbacks: DC offset & $1/f$ noise, more RF gain needed, LO leakage, linear RF blocks needed, I/Q mismatch due to amplitude and quadrature phase imbalances of analog components, LO feed-through.

2.4.3 Low IF Receiver

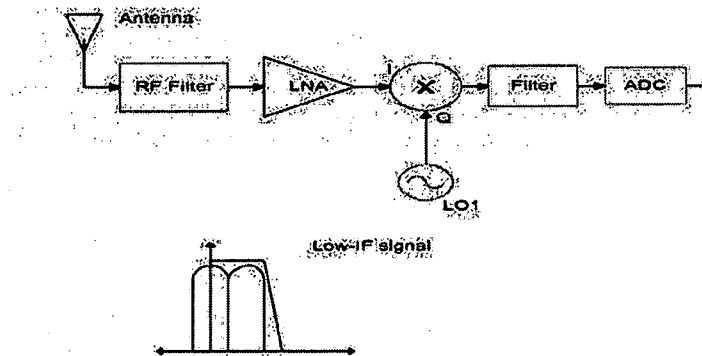


Figure 2.11 Low IF receiver.

In low-IF receivers shown in Figure 2.11, the IF frequency is in the range of a few hundreds of KHz to a few MHz [36]. They have similar advantages to direct conversion in terms of integration level but they considerably reduce the DC offset and $1/f$ noise problems present in direct conversion receivers. The new low-IF designs use complex poly-phase filters for image rejection. The following are the strengths and drawbacks of this architecture [29].

1. Strengths: compact, integrable, multi-standard, avoids Zero-IF problems, no flicker noise.

2. Drawbacks: I/Q paths, need better I/Q mismatching for optimum image suppression, LO feed-through, need complex poly-phase filter for good image rejection.

2.5 Main Components in Receiver Architecture

An overview of the components used to design receiver architectures is presented. A classification of these components is made on the basis of their features so that a few implications could be concluded.

2.5.1 RF Band-pass Filters

The main purpose of band-pass filters is to select the band of interest and eliminate all other frequency bands above and below the desired frequency band. At RF, band selection of only the receive band, which is fixed for a particular standard is performed. Band-pass filters can be designed using passive or active circuits. Passive circuits have a serious drawback of poor gain. Active circuits, on the other hand, help in increasing gain but they have issues like linearity, noise, and power consumption.

2.5.2 Low Noise Amplifiers

Low noise amplifiers (LNA) provide first order signal amplification to reduce the impact of noise on latter receiver blocks. The signal is degraded when it is received at the RF front-end due to path-loss, AWGN and multi-path fading. The main qualities of a LNA are high gain to amplify weak signals and low noise figure to suppress the noise produced by interferers and blockers [38]. The LNA boosts the gain of the signal without significantly increasing noise in the system. Because of the above mentioned characteristics, the LNA is placed before mixers. LNAs are of two types: 1. Single ended LNA. 2. Differential LNA [34]. Differential LNAs have high gain and better

noise figure compared to a single ended LNA, but have high power consumption, since they use two single ended stages.

2.5.3 Mixer

The purpose of a mixer is to perform the translation from RF frequency to IF frequency. The RF signal is mixed (multiplied) with a signal generated by a voltage controlled oscillator (VCO) to generate an IF signal. The mixer should have high IP3 or should have highly linear output to preserve the original signal content [29]. Typically because of its high noise, the mixer must be preceded by a low noise amplifier (LNA). A low pass filter is needed to remove the high frequency term. The operation of a mixer is given by equation (2.22) and depicted in Figure 2.12.

$$\begin{aligned} A_{rf} \cos(w_{rf}t) A_{lo} \cos(w_{lo}t) &= A_{rf} A_{lo} [\cos(w_{rf} - w_{lo})t + \cos(w_{rf} + w_{lo})t] \\ &= \frac{A_{rf} A_{lo}}{2} \cos(w_{if})t \end{aligned} \quad (2.22)$$

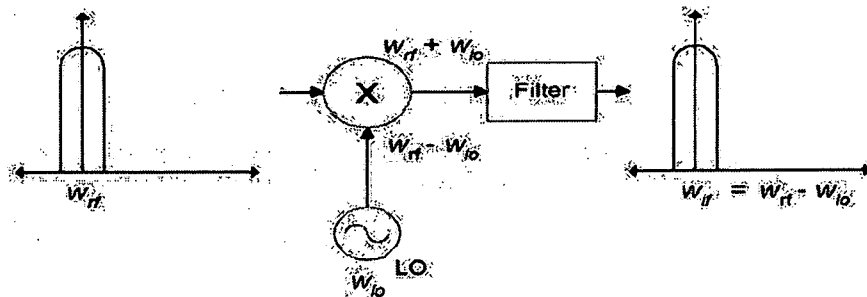


Figure 2.12 Operation of a mixer.

Several unwanted harmonics and inter-modulated components are produced during the mixing of two signals. Mixers can be followed by band-pass filter to recover the band of

interest. Although passive mixers have low distortion, they have very low gain. Active mixers have high gain but suffer from distortion. Active mixers are generally divided into two major types [31]: 1. Single balanced. 2. Double balanced. Double balanced mixers eliminate the feed-through problems caused by the RF and LO signal, but require more area and power. Also an additional band-pass filter is needed to recover the band of interest. Single balanced mixers like square law mixers, have a LO feed-through problem, but this can be eliminated by proper biasing. The unique feature of the single balanced mixers is that they have integrated band-pass filter to obtain the required band of interest.

2.5.4 Image-reject Filter (IR)

When RF signal and LO signal are mixed, an image signal is formed at the IF frequency. This image signal should be removed before mixing, since it is impossible to remove it after filtering as it coincides with the IF frequency. The image signal can be suppressed by an image-reject filter, placed before the mixer. The IR filter is designed to have small loss in the desired band and large attenuation in the image band [38].

2.5.5 Channel Select Filter

The channel select filter also referred to as IF filter is used to select the channel bandwidth of the desired signal. The requirements on the channel select filter depend upon the IF frequency [30]. The quality factor (Q) of the channel select filter is given in equation (2.23).

$$Q = \frac{\omega_{IF}}{\text{Channel Bandwidth}} \quad (2.23)$$

As IF frequency increases, the quality factor (Q) increases. Therefore, the constraints on the channel select filter are high, as it is desirable to have low Q.

2.5.6 Base-band Signal Processing

In base-band signal processing, the signal is translated or demodulated down to DC band or 0 Hz to recover the original signal content. An anti-aliasing filter is needed to preserve or band-limit the original signal. It should also remove unwanted signals or interferers. An analog-to-digital converter (ADC) is employed after the anti-aliasing filter to convert the signal to digital domain for further digital filtering.

2.5.7 Analog-to-digital Converter (ADC)

A typical constraint on high performance RF wireless architectures is the design of a high dynamic range, high resolution ADC. The ADC should have high dynamic range to capture the amplified analog signal. The resolution should be high enough to attenuate out-band noise and suppress interferers. The different types of ADC [41] are surveyed in Appendix A. A digital-to-analog converter (DAC) is used for converting signals from digital to analog domain in over-sampling data converters. Detailed information about DACs can be found in [39].

2.6 Some current wireless standards and specifications

Federal Communications Commission (FCC) imposes wireless standards for specific applications. Receiver architectures should conform to these wireless standards. The requirements and specifications of standards such as GSM, Bluetooth, UMTS, and CDMA 2000 are stated below. UMTS and CDMA 2000 are considered to be popular standards for high performance wireless applications because of their high bandwidth and low power consumption requirements.

2.6.1 Global System for Mobile Communication (GSM)

TDMA/FDD system

- GMSK modulation
- TX band: 890 – 915 MHz
- RX band: 935 – 960 MHz
- Signal bandwidth: 200 KHz

Sensitivity: -102dBm

- BER = 10^{-3} or SNR @demodulator > 9dB
- Signal Range: -102dBm to -15dBm
- For signal of -99dBm (Sensitivity + 3dB)

Selectivity

- Intermodulation test: two signals = -49dBm @800kHz and @1600kHz

Noise spectrum

- Noise @3MHz < -115dBc/Hz
- Noise @6MHz < -130dBc/Hz

Output power

- Up to 2-3 W: 33-35dBm

2.6.2 Bluetooth Standard

Frequency Hopping CDMA/TDD system

- GFSK modulation
- 1600 hops/s in normal operation
- TX/RX band: 2400 – 2483.5MHz (license free band)
- Signal bandwidth: 1MHz

Sensitivity: -70dBm

- BER = 10^{-3} or SNR @demodulator > 22dB
- Signal Range: -70dBm to -20dBm
- For signal of -67dBm (Sensitivity + 3dB)

Selectivity

- Intermodulation test: two signals = -39dBm @3MHz and @6MHz

Noise Spectrum

- Noise @550kHz < -20dBc/Hz
- Noise @2MHz < -20dBc/Hz

Output power

- Up to 100mW - 20dBm

2.6.3 Universal Mobile Telecommunication System (UMTS)

Wide-band CDMA system

- QPSK modulation
- TX band: 1920 – 1980MHz
- RX band: 2110 – 2170MHz
- Signal bandwidth: 1.92MHz

Sensitivity: -117dBm

- BER = 10^{-3} or SNR @demodulator > 7dB
- Signal Range: -117dBm to -25dBm
- For signal of -114dBm (Sensitivity + 3dB)

Selectivity

- Intermodulation test: -46dBm @5MHz and @10MHz

Noise spectrum

- Noise @10MHz < -132dBc/Hz
- Noise @15MHz < -144dBc/Hz

Output power

- Max 100mW (20dBm)

2.6.4 Code Division Multiplexing Access (CDMA 2000)

CDMA system

- QPSK modulation
- TX band: 1750 – 1790MHz
- RX band: 1840 – 1870MHz
- Signal bandwidth: 1.25MHz

Sensitivity: -117dBm

- BER = 10^{-3} or SNR @demodulator > 7dB
- Signal Range: -117dBm to -25dBm
- For signal of -102dBm (Sensitivity + 3dB)

Selectivity

- Intermodulation test: -46dBm @5MHz and @10MHz

Noise spectrum

- Noise @2.5MHz < -132dBc/Hz
- Noise @5MHz < -144dBc/Hz

Output power

- Max 100mW (20dBm)

3 INTRODUCTION TO NYQUIST AND OVER-SAMPLING DATA CONVERTERS

3.1 Types of Data Converters

In order to interface analog signals with digital signals, there is a need for analog-to-digital converters (ADC). A typical ADC consists of an analog modulator and a digital signal processor. ADCs are mainly classified into two types Nyquist and over-sampling data converters [26].

3.1.1 Nyquist Data Converters

A Nyquist ADC has input signal bandwidth exactly half of the sampling rate. To avoid aliasing, the input signal has to be sampled at twice the Nyquist frequency. In Nyquist ADCs, as shown in Figure 3.1, the input signal frequency is equal to the Nyquist frequency and anti-alias filters are employed to remove any signal above the Nyquist frequency.

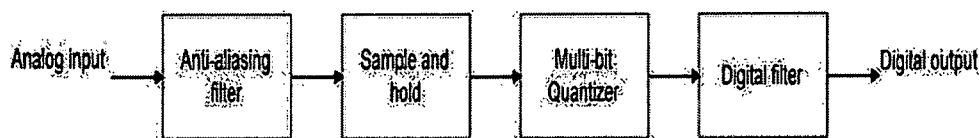


Figure 3.1 Nyquist ADC.

A Nyquist ADC consists of a track-hold or a sample-hold circuit to hold the input amplitude before quantization. The track-hold circuit is followed by a multi-bit

quantizer, which is typically a flash ADC or a pipeline ADC. The different types of multi-bit quantizers, mentioned in Appendix A, convert sample by sample in a single clock cycle without being dependent on the previous sample. Nyquist rate converters are simple to implement but have very low resolution. Since they have input frequencies close to Nyquist frequency aggressive noise shaping of unwanted out-of-band signals is obtained using a very high order anti-alias filter (AAF). The resolution obtained at the cost of expensive AAF filters still does not meet the demands of receiver application.

3.1.2 Over-sampling Data Converters

The advantages of over-sampling data converters over Nyquist data converters are high resolution and relaxed requirements for anti-alias analog filter. The over-sampling data converters that have sampling frequency much higher than twice the input signal frequency considerably reduce the complexity in analog filters.

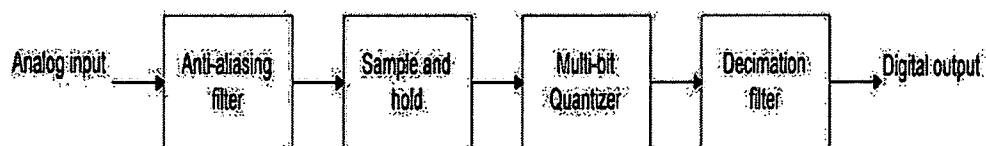


Figure 3.2 Over-sampling ADC.

Over-sampling attenuates the non-linearity, out-of-band noise components and increases the resolution. In over-sampling converters shown in Figure 3.2., the analog signal is sampled and quantized at a high frequency and converted to a high resolution low frequency digital signal by signal processing. In this case, decimation filters are used instead of typical digital filters. Decimation filters have the ability of efficiently down-

sampling the quantizer output frequency to the required signal bandwidth. The anti-alias filters play a similar role of removing signal components above the signal bandwidth; but in this case the input bandwidth is much smaller than the Nyquist frequency. Over-sampling converters rely on previous samples to produce their output. For a fixed signal bandwidth, the over-sampling ratio M , which is the ratio between the sampling frequency and desired signal bandwidth, can be increased to improve the resolution of the converter. Also the number of bits of the quantizer can be increased to effectively increase the resolution of the data converter. The over-sampling data converters are considered over Nyquist rate for their high resolution and relaxed system complexity. The basics of over-sampling modulators are discussed next.

To understand over-sampling ADCs, the two basic operations of sampling and quantization should be analyzed. Sampling is a conversion of continuous time signal into discrete signal and quantization is the process of converting infinite possible values of a continuous signal into N values of a discrete signal. In order to avoid aliasing, the continuous time signal must be sampled by at least twice its maximum signal frequency. According to Nyquist theorem, if this condition is satisfied, the analog signal can be reconstructed from the digital signal output without loss. In over-sampling data converters, sampling is performed at a much higher frequency than the signal bandwidth; as a result, aliasing and non-idealities due to out-of-band noise are highly attenuated. The same statement cannot be applied to the quantization process. Quantization is a mapping of infinite values of discrete-time analog signal into finite number of discrete time digital signal. This transformation inherently introduces non-idealities and distortion of the original analog signal. The quantization process plays a critical role in determining the

resolution of the converter. Therefore, the primary goal in designing data converters is to reduce quantization error by producing a close representation of analog signal in digital domain.

3.1.3 Quantization Error

In a typical over-sampling converter, the digital output signal is converted back to discrete analog signal and subtracted from the sampled input signal. This results in a quantization error. If analog input signal has full scale range equal to the range of the quantizer, then the quantization error is limited to $\{+\Gamma/2, -\Gamma/2\}$, Γ being the quantizer output step-size [39]. For a 3-bit quantizer with full scale range of 2.5 V, the quantizer step-size is given by equation (3.1)

$$\Gamma = \frac{2.5}{2^3 - 1} = 0.3571 \quad (3.1)$$

The quantization error completely depends upon the amplitude of the input signal. If the input amplitude varies in comparison with the quantizer step size without causing saturation then the quantization error is highly uncorrelated with the input signal and has a probability of lying in between $\{+\Gamma/2, -\Gamma/2\}$. The statistics of quantization noise is simplified by stating it simply as “input-independent additive white noise”. Figure 3.3 shows a probability density function (PDF) of the quantization error.

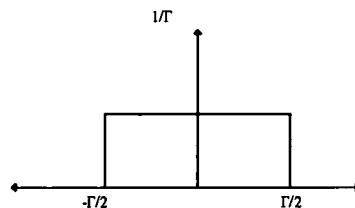


Figure 3.3 Probability density function of quantization error.

3.2 Signal-to-Noise (SNR) Ratio of Nyquist and Over-sampling ADCs

This section includes a discussion of the signal-to-noise ratio of the Nyquist and over-sampling data converters. Background information on how to theoretically calculate the signal and the noise power of a modulator is presented. The calculation results can be directly applied to find the resolution of the data converters.

3.2.1 Signal-to-Noise (SNR) Ratio of Nyquist rate Data Converters

For the Nyquist rate converters, noise power spectrum or power spectral density (PSD) is displayed in Figure 3.4.

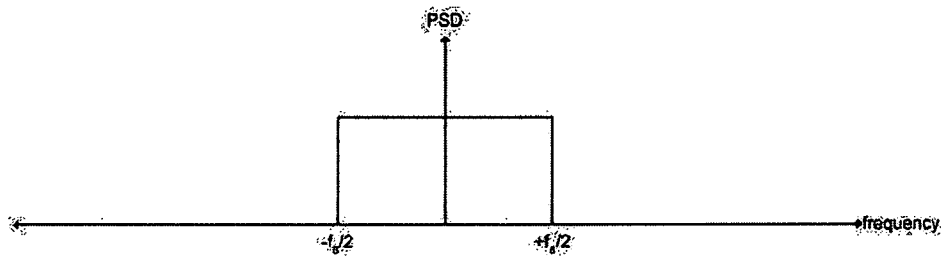


Figure 3.4 Power spectral density of noise in nyquist ADC.

The transfer characteristic of a 3-bit mid-rise quantizer is shown in Figure 3.5 (a). Figure 3.5 (b) displays the quantization error spectrum. The full range input is denoted by S and the input step-size or the least significant bit (LSB) of the quantizer is given by equation (3.2).

$$\Delta = \frac{S}{2^B} \quad (3.2)$$

Where, B is the number of bits of the quantizer.

Similarly the output of the quantizer has maximum range of P and its step-size or minimum distance between two output levels is given by equation (3.3)

$$\Gamma = \frac{P}{2^B - 1} \quad (3.3)$$

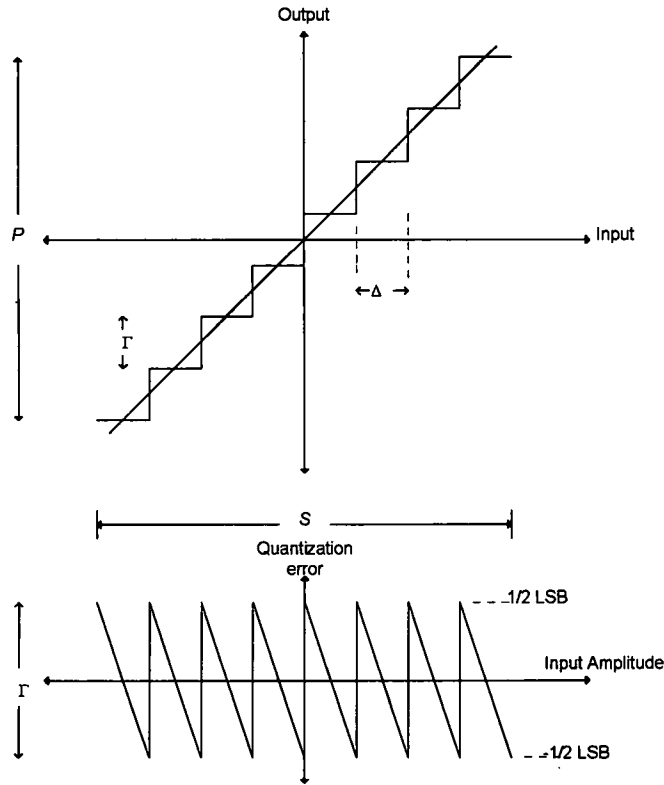


Figure 3.5(a). 3-bit mid-rise quantizer. (b). Quantization error spectrum.

The signal-to-quantization noise ratio can be obtained by applying a sinusoidal input signal with peak-to-peak amplitude of S volts. The power of this signal is given by equation (3.4)

$$S_{in} = \left(\frac{S}{2\sqrt{2}} \right)^2 = \left(\frac{\Delta \cdot 2^B}{2\sqrt{2}} \right)^2 \quad (3.4)$$

The quantization noise power can be determined from the PDF of Figure 3.3. The variance of quantization noise N_Q can be calculated by multiplying the magnitude of the

quantization error with square of the quantization error variable q and integrating the product over full scale range of quantization error. Equation (3.5) gives the variance or noise power of the quantization noise.

$$N_Q = \int_{-\infty}^{+\infty} q^2 \cdot P(q) d(q) \quad (3.5)$$

$$= \frac{1}{\Gamma} \int_{-\frac{\Gamma}{2}}^{+\frac{\Gamma}{2}} q^2 dq = \frac{1}{3\Gamma} \left[q^3 \right]_{-\frac{\Gamma}{2}}^{+\frac{\Gamma}{2}} = \frac{\Gamma^2}{12}$$

After combining equations (3.2), (3.3), (3.4), and (3.5), we can define the signal-to-noise ratio (SNR) of the quantizer as

$$SNR = 10 \log_{10} \left(\frac{S_{in}}{N_Q} \right) \quad (3.6)$$

$$= 10 \log_{10} \left(\frac{12 \cdot 2^{2B}}{8} \right)$$

$$= 1.76 + 6.02B \text{ dB}$$

3.2.2 Signal-to-Quantization noise (SNR) Ratio of Over-sampling Data Converters

For over-sampling data converters, the noise power spectrum or power spectral density (PSD) is displayed in Figure 3.6.

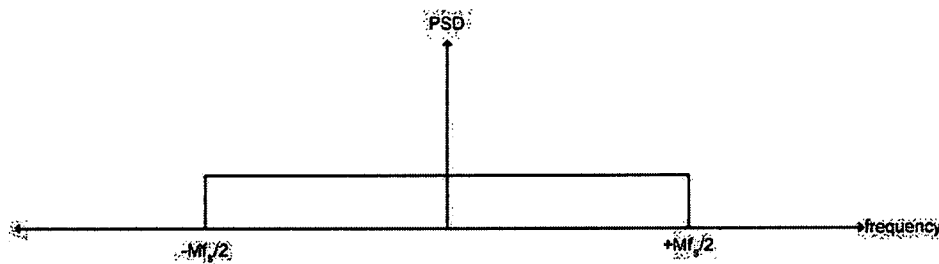


Figure 3.6 Power spectral density of noise in over-sampling ADC.

In over-sampling converters, over-sampling ratio M is given by equation

$$M = \frac{f_s}{2f_b} \quad (3.7)$$

The noise power spectrum reveals that noise power is spread over M times the sampling frequency for the over-sampling converter because of the over-sampling ratio, while in Nyquist rate converters it is spread over a range of twice the Nyquist frequency. The over-sampling of input frequency helps in attenuating noise over signal bandwidth. The signal power for over-sampling data converters is obtained using a similar approach to the one for Nyquist data converters, as given in equation (3.4). The noise power can alternatively be determined by integrating the magnitude of the transfer function and the PSD over the sampling range shown in Figure 3.6, but the transfer function $|H(f)|$ only extends over the signal bandwidth and we integrate over a fixed signal bandwidth $\{-f_b, f_b\}$. The noise power is given in equation (3.8).

$$\begin{aligned} N_{QM} &= \int_{-\frac{f_s}{2}}^{+\frac{f_s}{2}} N_Q \cdot |H(f)|^2 \cdot df \\ &= \int_{-f_b}^{+f_b} \frac{\Gamma^2}{12f_s} \cdot 1 \cdot df \\ &= \frac{\Gamma^2}{12 \cdot M} \end{aligned} \quad (3.8)$$

Combining equations (3.2), (3.3), (3.7), and (3.8), Signal-to-noise ratio (SNR) of the over-sampled quantizer is defined by equation (3.9).

$$SNR = 10 \log_{10} \left(\frac{S_{in}}{N_{QM}} \right) \quad (3.9)$$

$$= 10 \log_{10} \left(\frac{12 \cdot 2^{2B} \cdot M}{8} \right)$$

$$= 1.76 + 6.02B + 10 \log_{10}(M) \text{ dB}$$

3.3 Over-sampling Noise shaping Data Converters

The benefits of over-sampling data converters can be increased by shaping the quantization noise such that the noise power spectrum is highly attenuated within the signal bandwidth and shaped away from the band of interest. A typical noise shaping over-sampling converter is the delta sigma modulator. The delta sigma modulator has the ability of attenuating the quantization noise within the signal band without affecting the signal strength of the ADC due to its negative feedback. A first order delta sigma modulator can be seen in Figure 3.7.

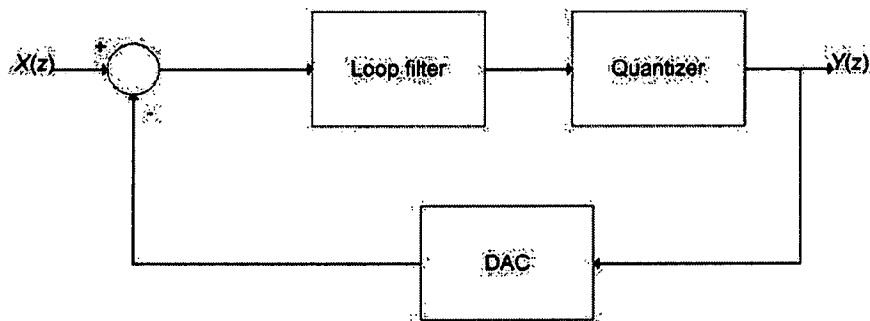


Figure 3.7 First order delta sigma modulator.

It consists of a loop filter followed by a 2^N bit ADC and DAC in the feedback path. The DAC converts the digital output signal of the modulator into discrete analog signal and subtracts this signal from the sampled input signal. This difference between the input

signal and the output signal (error signal) is passed through a loop filter, which is typically a discrete integrator. The integrator accumulates this difference signal, and the 2^N bit ADC compares the integrator output with 2^N-1 fixed reference voltages to generate an N -bit digital signal. The decimation filter that follows the delta-sigma modulator helps to attenuate out-of-band noise and improves the resolution of the converter. The delta sigma modulator derives its name from the difference and the summation operation and because the difference operation precedes the summation operation these modulators are termed as delta-sigma modulators ($\Delta\Sigma$). A linear model of the single-bit first order $\Delta\Sigma$ modulator is presented in Figure 3.8.

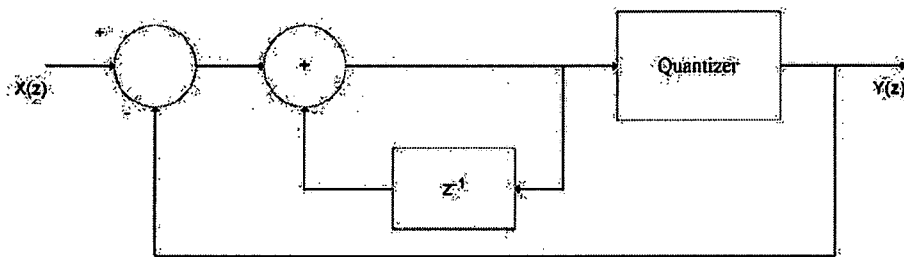


Figure 3.8 Linear model of first order delta sigma modulator.

The following equation (3.10) will describe the linear operation of the single-bit first order $\Delta\Sigma$ modulator.

$$Y(z) = H(z) \cdot [X(z) - Y(z)] + E(z) \quad (3.10)$$

Where, $H(z) = \frac{z^{-1}}{1 - z^{-1}}$ = transfer function of the loop filter or integrator,

$E(z)$ = the quantization noise

To obtain the signal transfer function (STF) given in equation (3.11), we set $E(z)$ to 0

$$STF = \frac{Y(z)}{X(z)} = z^{-1} \quad (3.11)$$

To obtain the noise transfer function (NTF) given in equation (3.12), we set $X(z)$ to 0

$$NTF = \frac{Y(z)}{E(z)} = 1 - z^{-1} \quad (3.12)$$

3.3.1 SNR of First-Order Over-sampling Noise Shaping Data Converters

In case of over-sampling noise shaping data converters, the output is feedback to the input. If the input signal is larger in amplitude than the output signal, the modulator is said to be unstable. The maximum input signal is made equal or less than the maximum output signal to have unity linear gain for the quantizer. The input signal power of the first order single bit is given by equation (3.13)

$$S_{in} = \left(\frac{S}{2\sqrt{2}} \right)^2 = \left(\frac{\Delta \cdot (2^B - 1)}{2\sqrt{2}} \right)^2 \quad (3.13)$$

From equation (3.12), quantization noise resembles a high-pass filter function. The magnitude of high-pass filter is determined by substituting the equation (3.14) in (3.12).

$$z = e^{-j2\pi \frac{f}{f_s}} = \cos(-2\pi \frac{f}{f_s}) + j \cdot \sin(-2\pi \frac{f}{f_s}) \quad (3.14)$$

The magnitude of frequency response of high-pass filter is given in equation (3.15)

$$\begin{aligned} |H_N(f)| &= \sqrt{\left((1 - \cos(-2\pi \frac{f}{f_s}))^2 + (\sin(-2\pi \frac{f}{f_s}))^2 \right)} \\ &= \sqrt{2(1 - \cos(2\pi \frac{f}{f_s}))} \end{aligned} \quad (3.15)$$

The above equation can be further simplified from the trigonometric identity $\cos(2x) = 1 - 2\sin^2(x)$, and since the sampling frequency f_s is much larger than the input signal frequency f , we get equation (3.16)

$$|H_N(f)| = 2\sin(\pi \frac{f}{f_s}) = 2\pi \frac{f}{f_s} \quad (3.16)$$

The noise power is deduced by integrating the product of the noise variance found by equation (3.8) and the square of the magnitude of frequency response. This is given in equation (3.17), as explained by [39].

$$\begin{aligned} N_{QM} &= \int_{-\frac{f_s}{2}}^{+\frac{f_s}{2}} N_Q \cdot |H_N(f)|^2 \cdot df \\ &= \int_{-f_b}^{+f_b} \left(\frac{\Gamma^2}{12f_s}\right) \cdot \left(2\pi \frac{f}{f_s}\right)^2 df \\ &= \frac{\pi^2 \Gamma^2}{36M^3} \end{aligned} \quad (3.17)$$

From equations (3.13) and (3.17), we get the SNR of the single-bit first order modulator as given below

$$\begin{aligned} SNR &= 10\log_{10}\left(\frac{S_{in}}{N_{QM}}\right) = 10\log_{10}\left(\frac{\Gamma^2(2^B - 1)^2}{8} \cdot \frac{36M^3}{\pi^2 \Gamma^2}\right) \\ &= 10\log_{10}\left(\frac{9}{2\pi^2}\right) + 30\log_{10}(M) + 20\log_{10}(2^B - 1) \end{aligned} \quad (3.18)$$

This equation shows that the SNR of over-sampling noise shaping data converters is increased by 9 dB for every doubling of sampling frequency while that for a typical over-sampling data converter is 3 dB. Thus, a 6 dB increase in SNR can be obtained by using over-sampling noise shaping data converters.

3.3.2 SNR of Second-Order Over-sampling Noise Shaping Data Converters

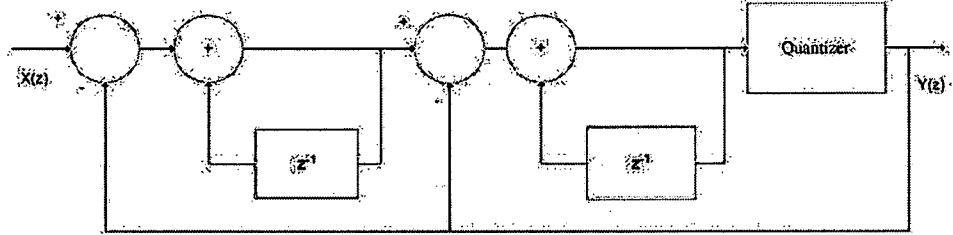


Figure 3.9 Linear model of second order modulator.

A typical single-bit second order modulator is shown in Figure 3.9. The second-order modulator integrates the signal twice and employs double differentiation of the quantization noise. The second order modulator output is given by equation (3.19).

$$Y(z) = z^{-2}X(z) + (1 - z^{-1})^2 E(z) \quad (3.19)$$

To obtain the signal transfer function (*STF*), we set $E(z) = 0$ in equation (3.19).

$$STF = \frac{Y(z)}{X(z)} = z^{-2} \quad (3.20)$$

To obtain the noise transfer function (*NTF*), we set $X(z) = 0$ given in equation (3.12).

$$NTF = \frac{Y(z)}{E(z)} = (1 - z^{-1})^2 \quad (3.21)$$

The input signal power of the second order modulator is same as the one for a first order modulator, if a similar sinusoidal input signal with peak-to-peak amplitude of S is applied. This power is given by equation (3.13). The magnitude of frequency response of a second order high-pass filter $(1 - z^{-1})^2$ is given in equation (3.22).

$$\begin{aligned}
|H_N(f)| &= \left(\sqrt{\left(1 - \cos\left(-2\pi \frac{f}{f_s}\right)\right)^2 + \left(\sin\left(-2\pi \frac{f}{f_s}\right)\right)^2} \right)^2 \\
&= 2 \left(1 - \cos\left(2\pi \frac{f}{f_s}\right) \right)
\end{aligned} \tag{3.22}$$

The noise power of the second order noise shaping data converter is calculated by integrating the product of the noise variance and the square of the magnitude of frequency response given by equation (3.22), as given by [39].

$$N_{QM} = \int_{-\frac{f_b}{2}}^{+\frac{f_b}{2}} N_Q \cdot |H_N(f)|^2 \cdot df \tag{3.23}$$

Using trigonometric identities, we simplify equation (3.23).

$$\begin{aligned}
&= \int_{-f_b}^{+f_b} \left(\frac{\Gamma^2}{12f_s} \right) \cdot 4 \left(1 - \cos 2\pi \left(\frac{f}{f_s} \right) \right)^2 df \\
&= \int_{-f_b}^{+f_b} \left(\frac{\Gamma^2}{12f_s} \right) \cdot 4 \sin^2 \left(\pi \frac{f}{f_s} \right) df \\
&= \int_{-f_b}^{+f_b} \left(\frac{\Gamma^2}{12f_s} \right) \cdot 4 \left(\pi \frac{f}{f_s} \right)^2 df \\
&= \frac{\pi^2 \Gamma^2}{\sqrt{12} \sqrt{5M}^{5/2}}
\end{aligned} \tag{3.24}$$

Using equation (3.13) and equation (3.23), we can obtain the SNR of the second order converter as

$$SNR = 6.02N + 1.76 - 12.9 + 50 \log_{10}(M) \tag{3.25}$$

There is an increase of 15 dB or 2.5 bits of resolution for every doubling of over-sampling factor. Thus, a 12 dB increase in SNR can be obtained by using over-sampling noise shaping data converters instead of over-sampling converters.

3.4 Higher Order Modulators

The theory applied to single bit first order and second order modulators can be extended to higher order modulators with more than two feedback loops. Higher order or N^{th} order modulators can be realized to obtain very high SNR. However these modulators have a tendency to become unstable at higher input amplitudes. For a general N^{th} order modulator shown in Figure 3.10, noise power is calculated by equation (3.26).

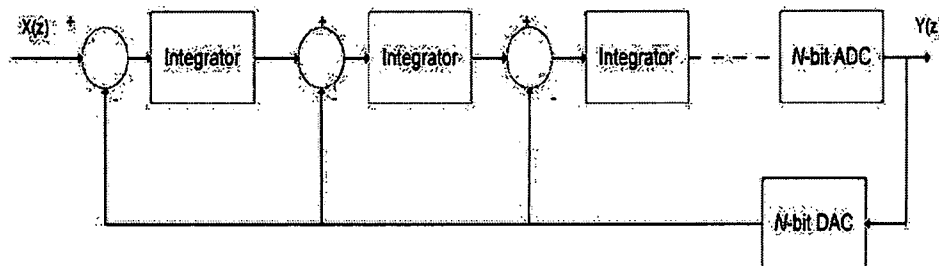


Figure 3.10 N^{th} order delta sigma modulator.

$$N_{QM} = \int_{-\frac{f_b}{2}}^{+\frac{f_b}{2}} N_Q \cdot |H_N(f)|^N \cdot df \quad (3.26)$$

Using trigonometric identities, we simplify equation (3.27)

$$= \int_{-f_b}^{+f_b} \left(\frac{\Gamma^2}{12f_s} \right) \cdot 2^N \left(1 - \cos 2\pi \left(\frac{f}{f_s} \right) \right)^N df \quad (3.27)$$

$$= \frac{\pi^N \Gamma^2}{\sqrt{12} \sqrt{2N+1} M^{N+1/2}}$$

SNR of a general N^{th} order modulator is given in [39] by equation (3.28).

$$SNR = 6.02N + 1.76 - 20 \log_{10} \left[\frac{\pi^N}{\sqrt{2N+1}} \right] + [20N + 10] \log_{10}(M) \quad (3.28)$$

The above equation reveals the fact that for every doubling in over-sampling ratio M , the resolution improves by $M + 0.5$ bits.

3.5 Cascaded Noise Shaping Modulators

In order to get around the stability issues in single stage higher order modulators, the concept of cascaded multi-stage noise shaping converters (MASH) was introduced [12]. In MASH topology, higher noise shaping is achieved by cascading two inherently stable modulators. The quantization noise of the first stage is fed-forward to the next stage and a noise cancellation logic (NCL) is employed at the digital outputs to perfectly cancel the unwanted noise.

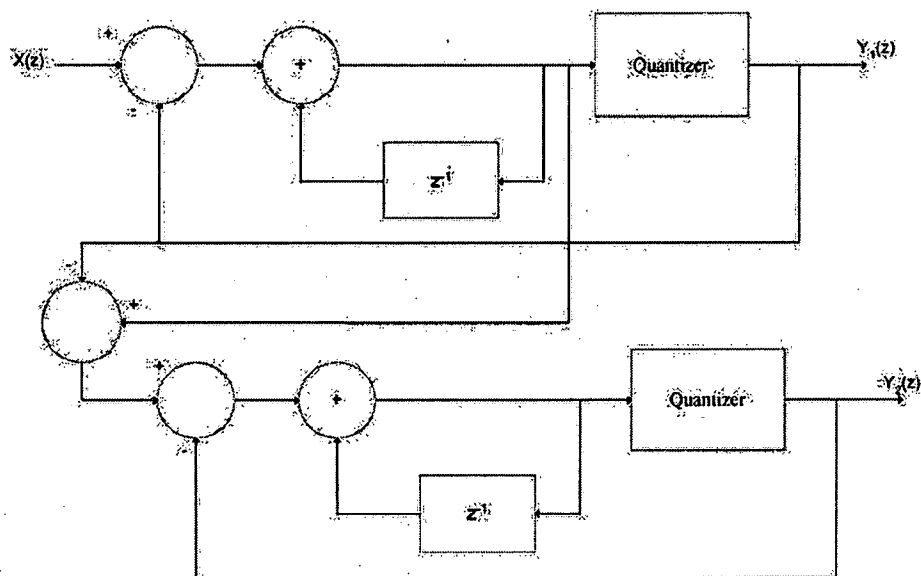


Figure 3.11 Two-stage 1-1 MASH modulator.

In two-stage 1-1 MASH architecture as shown in Figure 3.11, the analog noise transfer function (ANTF) of the first stage ($1-z^{-1}$) should match exactly the digital noise transfer function (DNTF) of the second stage to completely eliminate the quantization noise from the system. If ANTF is not equal to DNTF then serious degradation of performance results due to leakage of quantization noise through the second stage to the final output [40]. In practical MASH modulators, there always exists an inequality between the ANTF and DNTF because of the mismatch of analog and digital gains. This leads to leakage of quantization noise through the second stage to the output. The goal of a designer is to minimize the leakage of quantization noise in improving the performance of the modulator. A second order modulator can deal with the leakage of quantization more effectively than a first order modulator because of its better noise shaping. A first order modulator is never preferred as the first stage of the MASH modulator for this very

reason. Also higher order modulators such as third order modulator are avoided for stability reasons, since every modulator in the cascaded modulator architecture should be stable to obtain desirable designs. A cascaded modulator can be implemented using various combinations of second order and first order modulators. A second order modulator followed by a first order modulator is termed as 2-1 modulator. Some of the recent configurations of cascaded modulators include 2-1 modulators, 2-1-1 modulators, 2-2 modulators, and 2-2-2 modulators. From previous work [41] and [42], it is understood that a three-stage MASH modulator does not exhibit performance as good as a two stage modulator after taking into account considerations like power consumption, hardware complexity, and speed. Although a 2-2 modulator and the previously mentioned three-stage modulators have better resolution than 2-1 modulators, they also have very stringent design requirements which cannot be satisfied without additional circuit and layout complexities. We have selected a 2-1 modulator over its counterparts for its simplicity in design and optimum balance in terms of resolution, speed, power and area. A comprehensive study of different noise shaping feedback topologies can be found in [43]. To minimize the effect of quantization noise leakage and obtain optimum noise shaping, we need to determine the correct analog and digital gain coefficients.

3.6 Derivation of an Empirical Formula for Coefficients of a Cascaded Third Order (2-1) Feedback Topology for Optimum Noise Shaping

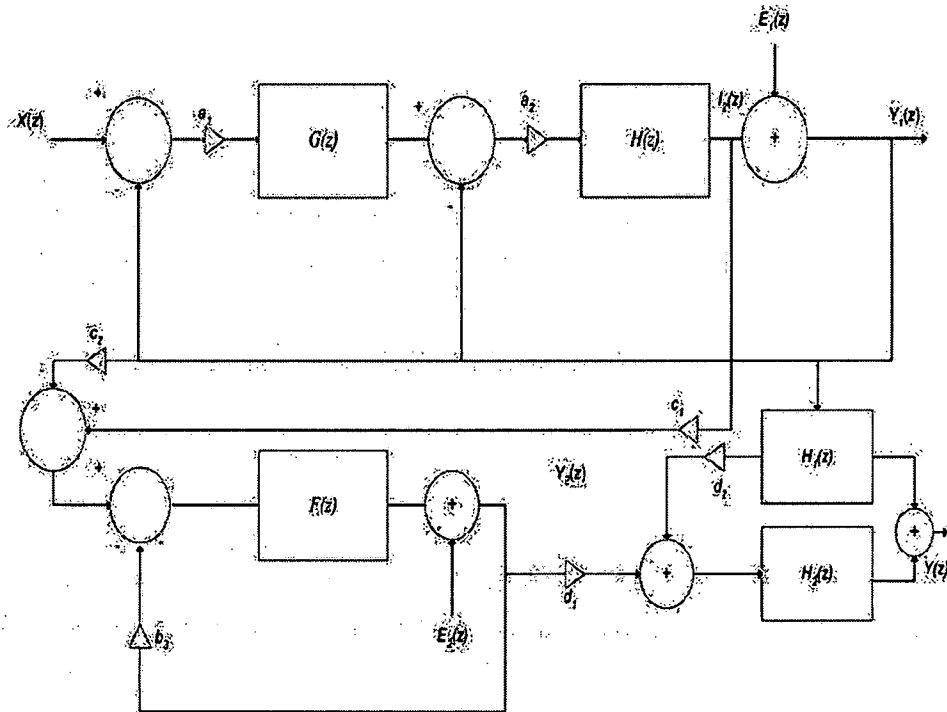


Figure 3.12 Cascaded 2-1 third order feedback modulator.

Consider a linear system implementation of a typical cascaded third order feedback modulator shown in Figure 3.12. The first stage consists of a single bit second order feedback modulator followed by a single-bit first order modulator as in [44]. First let us define some of the gain coefficients and transfer functions of the systems involved in the second order feedback modulator. $X(z)$ and $Y_1(z)$ are the input and output of the second order feedback modulator, respectively. $G(z)$ and $H(z)$ represent transfer functions of the

integrators used to implement the second order modulator. These are defined in equations (3.29) and (3.30).

$$G(z) = \frac{z^{-1}}{1 - z^{-1}} \quad (3.29)$$

$$H(z) = \frac{z^{-1}}{1 - z^{-1}} \quad (3.30)$$

The sub-unity gain coefficients a_1 and a_2 are used to limit the gain of the integrators within their linear range. For simplicity, the feedback gain coefficients b_1 and b_2 are assumed to be unity and not included in the figure. The single-bit quantizer is a simple comparator with arbitrary linear gain k_1 . For a single bit first order modulator, which is the second stage of the cascaded modulator, the transfer function of the integrator is defined by $F(z)$ in equation (3.31). The gain of the quantizer in the first order modulator is k_2 . $E_1(z)$ and $E_2(z)$ are the quantization errors of the first and second stage, respectively.

$$F(z) = \frac{z^{-1}}{1 - z^{-1}} \quad (3.31)$$

The two parameters c_1 and c_2 are needed to scale the quantization noise to prevent overloading the next stage, which in this case is the first order modulator. The gain coefficient c_1 scales the second integrator output $I_2(z)$ while c_2 scales the output of the second order modulator $Y_1(z)$. These quantization noise scaling parameters need to be appropriately chosen to obtain optimum noise shaping functions. If these parameters are very small, the input of the second stage cannot utilize the entire dynamic range and the SNR is reduced. If they are very large, the second stage input is overloaded and the SNR is lowered due to harmonic distortion and non-linearity. In order to strike a balance between c_1 and c_2 , the arbitrary quantizer gain k_1 should be found experimentally to

appropriately scale the second modulator output. The scaled second modulator output ($c_2 \cdot Y_1(z)$) is then subtracted from the scaled second integrator output ($c_1 \cdot I_2(z)$) and passed to the next stage. Ideally, the value of c_1 should be unity to completely remove the signal and pass the scaled version of quantization noise to the second stage. The next stage input $X_1(z)$ is the estimation of quantization error of the first stage. The derivation for determining the gain coefficients of second order feedback is given below in the following equations. From Figure 3.12, we can write the linear equations for cascaded feedback modulator as

$$\left((X(z) - Y_1(z)) a_1 \frac{z^{-1}}{1 - z^{-1}} - Y_1(z) \right) a_2 k_1 \frac{z^{-1}}{1 - z^{-1}} + E_1(z) = Y_1(z)$$

After simplifying the above equation we get,

$$a_1 a_2 k_1 z^{-2} X(z) + E_1(z) (1 - z^{-1})^2 = Y_1(z) \left((1 - z^{-1})^2 + k_1 a_2 z^{-1} + k_1 a_1 a_2 z^{-2} \right)$$

$$Y_1(z) = \frac{a_1 a_2 k_1 z^{-2} X(z) + (1 - z^{-1})^2 E_1(z)}{1 + (k_1 a_2 - 2) z^{-1} + (1 + k_1 a_1 a_2 - k_1 a_2) z^{-2}} \quad (3.32)$$

The ideal second order noise shaping equation is

$$Y_1(z) = a_1 a_2 k_1 z^{-2} X(z) + (1 - z^{-1})^2 E_1(z) \quad (3.33)$$

Comparing equations (3.32) and (3.33), we get

$$\begin{aligned} k_1 a_1 a_2 &= 1 \\ k_1 a_2 &= 2 \\ (1 + k_1 a_1 a_2 - k_1 a_2) &= 0 \end{aligned} \quad (3.34)$$

If $a_1 = 1/2$; $a_2 = 1/2$; then $k_1 = 4$

There are other combinations of k_1 , a_1 , and a_2 that satisfy equation (3.34) to obtain ideal second order modulator. Simulations should be performed to select coefficients that

produce the best SNR. To obtain the output of the second stage, we apply linear equations to the first order modulator.

$$((X_1(z) - b_3 Y_2(z))) k_2 \frac{z^{-1}}{1 - z^{-1}} + E_2(z) = Y_2(z)$$

After simplifying the above equation we get,

$$k_2 z^{-1} X_1(z) + E_2(z)(1 - z^{-1}) = Y_2(z) \left((1 - z^{-1}) + b_3 k_2 z^{-1} \right)$$

$$Y_2(z) = \frac{k_2 z^{-1} X_1(z) + (1 - z^{-1}) E_2(z)}{1 - z^{-1} (1 - b_3 k_2)} \quad (3.35)$$

where $X_1(z) = I_2(z) - Y_1(z)$

$$= c_1 \left(\frac{Y_1(z) - E_1(z)}{k_1} \right) - c_2 Y_1(z)$$

After further simplification,

$$Y_2(z) = \frac{k_2 \left(\frac{c_1}{k_1} - c_2 \right) z^{-1} Y_1(z) - \frac{k_2 c_1}{k_1} z^{-1} E_1(z) + (1 - z^{-1}) E_2(z)}{1 - z^{-1} (1 - b_3 k_2)} \quad (3.36)$$

Comparing with the ideal equation of first order modulator given below

$$Y_2(z) = z^{-1} Y_1(z) + (1 - z^{-1}) E_2(z) \quad (3.37)$$

We get,

$$b_3 k_2 = 1; \quad b_3 = \frac{1}{k_2} \quad (3.38)$$

For the first order multi-bit modulator, typically $b_3 = 1$, hence $k_2 = 1$.

From equation (3.33) we have,

$$E_1(z) = \frac{Y_1(z) - a_1 a_2 k_1 z^{-2} X(z)}{(1 - z^{-1})^2} \quad (3.39)$$

Replacing $E_1(z)$ in equation (3.36) by equation (3.39),

$$Y_2(z) = \frac{a_1 a_2 k_2 c_1 z^{-1} X(z)}{(z - 1)^2} + E_2(z)(1 - z^{-1}) + Y_1(z) k_2 z^{-1} \left[\left(\frac{c_1}{k_1} - c_2 \right) - \frac{c_1}{k_1 (1 - z^{-1})^2} \right] \quad (3.40)$$

Figure 3.13 shows a model of a digital error correction logic to obtain the final output from the outputs $Y_1(z)$ and $Y_2(z)$ of the second order and first order modulators, respectively. The $H_1(z)$ and $H_2(z)$ in equation (3.41) are DNTF functions of the NCL for the first stage and second stage of a cascaded third order modulator, respectively.

$$\begin{aligned} H_1(z) &= z^{-1} \\ H_2(z) &= (1 - z^{-1})^2 \end{aligned} \quad (3.41)$$

They are chosen such that ANTF of the first stage (second order modulator), which in this case is $(1 - z^{-1})^2$, should match exactly the DNTF of the second stage (first order modulator) and analog signal transfer function (ASTF) of the second stage z^{-1} should match exactly the DNTF of the first stage [40]. The digital gain coefficients d_1 and d_2 scale the DNTF, which then should be combined with $Y_2(z)$ and $Y_1(z)$ of the MASH modulator to cancel out the quantization error $E_1(z)$ from the first stage.

The final output $Y(z)$ is given by equation by the following NCL

$$\begin{aligned} Y(z) &= H_1(z)Y_1(z) - d_1 H_1(z)Y_1(z)H_2(z) + d_2 Y_2(z)H_2(z) \\ Y(z) &= a_1 a_2 k_2 c_1 d_2 z^{-3} X(z) + E_2(z)(1 - z^{-1})^3 \\ &\quad + Y_1(z) \left[z^{-1} \left(1 - d_2 \frac{k_2 c_1}{k_1} \right) - z^{-1} (1 - z^{-1})^2 \left(d_1 - d_2 k_2 z^{-1} \left(\frac{c_1}{k_1} - c_2 \right) \right) \right] \end{aligned} \quad (3.42)$$

Ideally, the output of NCL should contain a delayed version of input signal and third order shaped quantization error $E_2(z)$ from the second stage.

Comparing equation (3.42) with the ideal third order equation in (3.43),

$$Y_1(z) = z^{-3}X(z) + (1 - z^{-1})^3 E_2(z) \quad (3.43)$$

$$d_2 a_1 a_2 k_2 c_1 = 1;$$

$$1 - d_2 c_1 \frac{k_2}{k_1} = 0;$$

$$d_2 = \frac{k_1}{k_2 c_1} = \frac{b_3}{a_1 a_2 c_1}; \quad (3.44)$$

$$d_1 - d_2 k_2 \left(\frac{c_1}{k_1} - c_2 \right) = 0;$$

$$d_1 = 1 - \frac{c_2}{a_1 a_2 c_1} \quad (3.45)$$

3.7 Derivation of an Empirical Formula for Coefficients of the Proposed Cascaded Third Order (2-1) Feed-forward for Optimum Noise Shaping

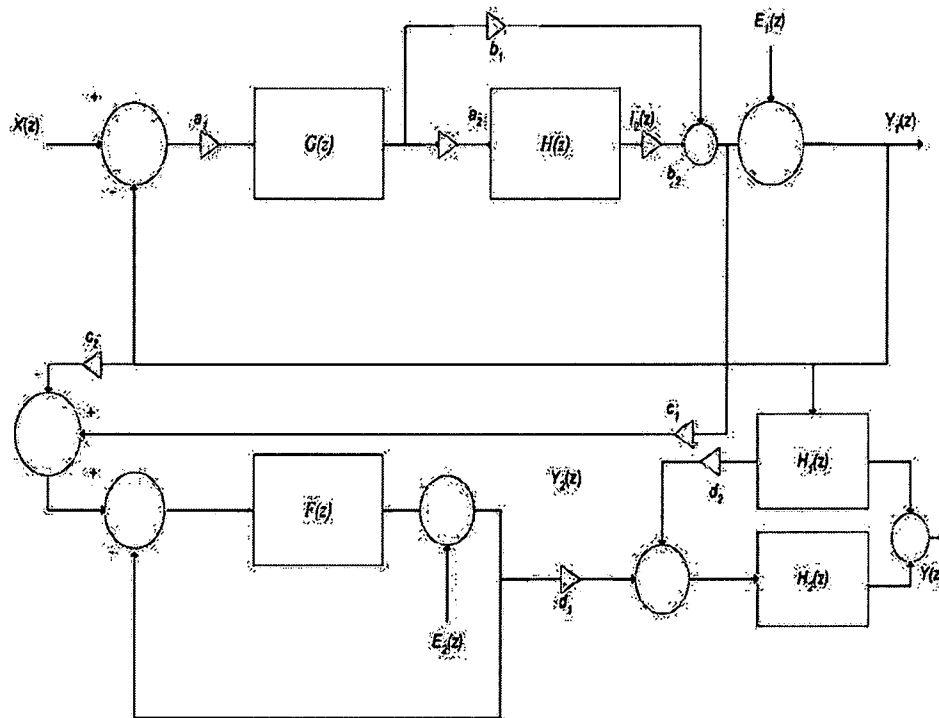


Figure 3.13 Cascaded 2-1 third order feed-forward modulator.

Consider a linear system implementation of the proposed cascaded third order feed-forward modulator shown in Figure 3.14. The first stage consists of a single bit second order feed-forward modulator followed by a single-bit first order modulator. The transfer functions of the systems $G(z)$ and $H(z)$ involved in the second order feed-forward modulator also appear in equations (3.29) and (3.30). $X(z)$ and $Y_1(z)$ are the input and output of the second order feed-forward modulator, respectively. The sub-unity gain coefficients a_1 and a_2 are used to limit the gain of the integrators within linear range of the integrators as in the case of the second order feed-back modulator. The feed-forward gain coefficients b_1 and b_2 are responsible for the noise shaping of the second order feed-forward modulator. The single bit quantizer is a simple comparator with arbitrary linear gain k_1 . For a single bit first order modulator, which is the second stage of the cascaded modulator, the transfer function of the integrator is defined by $F(z)$ in equation (3.31). The gain of the quantizer in the first order modulator is k_2 . $E_1(z)$ and $E_2(z)$ are the quantization errors of the first and second stage, respectively. The purpose of parameters c_1 and c_2 is to scale the quantization noise from overloading the next stage. The optimum values of c_1 and c_2 must ensure that correct noise shaping takes place and that best SNR is obtained. The scaled second modulator output ($c_2 \cdot Y_1(z)$) is then subtracted from the scaled quantizer input ($c_1 \cdot I_2(z)$) and passed as an input to the next stage $X_1(z)$. The derivation for determining the coefficients of the second order feed-forward modulator is given below in the following equations. From Figure 3.13, the linear equation of the cascaded feed-forward modulator can be given as

$$\left((X(z) - Y_1(z)) a_1 \frac{z^{-1}}{1-z^{-1}} \right) a_2 b_2 k_1 \frac{z^{-1}}{1-z^{-1}} + \left((X(z) - Y_1(z)) a_1 \frac{z^{-1}}{1-z^{-1}} \right) b_1 k_1 + E_1(z) = Y_1(z)$$

After simplifying the above equation we get,

$$\begin{aligned} & k_1 a_1 a_2 b_2 z^{-2} X(z) + k_1 a_1 b_1 z^{-2} X(z) + k_1 a_1 b_1 z^{-1} X(z) + E_1(z)(1-z^{-1})^2 \\ &= Y_1(z) \left((1-z^{-1})^2 + k_1 a_1 b_1 z^{-1} + k_1 a_1 a_2 b_2 z^{-2} \right) \\ & Y_1(z) = \frac{k_1 a_1 b_1 z^{-1} X(z) - (k_1 a_1 b_1 - k_1 a_1 a_2 b_2) z^{-2} X(z) + (1-z^{-1})^2 E_1(z)}{1 + (k_1 a_1 b_1 - 2) z^{-1} + (1 + k_1 a_1 a_2 b_2 - k_1 a_1 b_1) z^{-2}} \end{aligned} \quad (3.46)$$

$$Y_1(z) = \frac{k_1 (a_1 b_1 - z^{-1} (a_1 b_1 - a_1 a_2 b_2)) z^{-1} X(z) + (1-z^{-1})^2 E_1(z)}{1 + (k_1 a_1 b_1 - 2) z^{-1} + (1 + k_1 a_1 a_2 b_2 - k_1 a_1 b_1) z^{-2}}$$

The ideal second order noise shaping equation is

$$Y_1(z) = k_1 (a_1 b_1 - z^{-1} (a_1 b_1 - a_1 a_2 b_2)) z^{-1} X(z) + (1-z^{-1})^2 E_1(z) \quad (3.47)$$

Comparing equations (3.46) and (3.47), we get

$$\begin{aligned} (1 - k_1 a_1 b_1 + k_1 a_1 a_2 b_2) &= 0 \\ k_1 a_1 b_1 &= 2 \\ k_1 a_1 a_2 b_2 &= 1 \end{aligned} \quad (3.48)$$

If $a_1 = 1; a_2 = 1$; then $k_1 = 1; b_2 = 1$ and $b_1 = 2$

$$b_1 = 2a_2 b_2$$

There exist several combinations of k_1, a_1, a_2, b_1 , and b_2 that satisfy equation (3.48). After performing several experiments the combination that yields the best SNR should be chosen. To obtain the output of the second stage, a similar linear system analysis was performed on the first order modulator.

$$((X_1(z) - b_3 Y_2(z))) k_2 \frac{z^{-1}}{1 - z^{-1}} + E_2(z) = Y_2(z)$$

If $b_3 = 1$;

After simplifying the above equation we get,

$$k_2 z^{-1} X_1(z) + E_2(z)(1 - z^{-1}) = Y_2(z)((1 - z^{-1}) + k_2 z^{-1})$$

$$Y_2(z) = \frac{k_2 z^{-1} X_1(z) + (1 - z^{-1}) E_2(z)}{1 - z^{-1}(1 - k_2)} \quad (3.49)$$

where $X_1(z) = I_2(z) - Y_1(z)$

$$= c_1 \left(\frac{Y_1(z) - E_1(z)}{k_1} \right) - c_2 Y_1(z)$$

After simplifying further,

$$Y_2(z) = \frac{k_2 \left(\frac{c_1}{k_1} - c_2 \right) z^{-1} Y_1(z) - \frac{k_2 c_1}{k_1} E_1(z) + (1 - z^{-1}) E_2(z)}{1 - z^{-1}(1 - k_2)} \quad (3.50)$$

Comparing with the ideal equation of first order modulator given below

$$Y_2(z) = z^{-1} X_1(z) + (1 - z^{-1}) E_2(z) \quad (3.51)$$

We get,

$$k_2 = 1; \quad (3.52)$$

From equation (3.47) we have,

$$E_1(z) = \frac{Y_1(z) - k_1 (a_1 b_1 - z^{-1} (a_1 b_1 - a_1 a_2 b_2)) z^{-1} X(z)}{(1 - z^{-1})^2} \quad (3.53)$$

Replacing $E_1(z)$ from equation (3.39) in equation (3.50),

$$Y_2(z) = \frac{a_1 a_2 k_2 c_1 z^{-1} X(z)}{(z - 1)^2} + E_2(z) \frac{z^{-1}}{(1 - z^{-1})^2} + Y_1(z) \left[z^{-1} k_2 \left(\frac{c_1}{k_1} - c_2 \right) - k_2 \frac{c_1}{k_1 (1 - z^{-1})^2} \right] \quad (3.54)$$

A similar noise cancellation scheme used in cascading of third order feedback modulators is applied to the third order (2-1) feed-forward modulator. The NCL for the third order (2-1) feed-forward modulator is modeled in Figure 3.13. The DNTF functions $H_1(z)$ and

$H_2(z)$ mentioned in equation (3.41) are also used for the cascaded feed-forward modulator. The digital gain coefficients d_1 and d_2 scale the DNTF, which are correctly combined with $Y_2(z)$ and $Y_1(z)$ of the MASH modulator to cancel out the quantization error $E_1(z)$ from the first stage.

The final output $Y(z)$ is given by the following NCL

$$\begin{aligned}
 Y(z) &= H_1(z)Y_1(z) - d_1 H_1(z)Y_1(z)H_2(z) + d_2 Y_2(z)H_2(z) \\
 Y(z) &= z^{-2}X(z) \left(d_2 k_2 c_1 (a_1 b_1 - z^{-1} (a_1 b_1 - a_1 a_2 b_2)) \right) + E_2(z)(1 - z^{-1})^3 \\
 &\quad + Y_1(z) \left[\frac{1}{z} \left(1 - d_2 \frac{k_2 c_1}{k_1} \right) - \frac{(z-1)^2}{z^3} \left(d_1 - d_2 k_2 z^{-1} \left(\frac{c_1}{k_1} - c_2 \right) \right) \right] \quad (3.55) \\
 Y(z) &= X(z) \left(d_2 k_2 c_1 a_1 b_1 z^{-2} - z^{-3} d_2 k_2 c_1 (a_1 b_1 - a_1 a_2 b_2) \right) + E_2(z)(1 - z^{-1})^3 \\
 &\quad + Y_1(z) \left[\frac{1}{z} \left(1 - d_2 \frac{k_2 c_1}{k_1} \right) - \frac{(z-1)^2}{z^3} \left(d_1 - d_2 k_2 \frac{1}{z} \left(\frac{c_1}{k_1} - c_2 \right) \right) \right]
 \end{aligned}$$

Comparing equation (3.55) with ideal third order equation in (3.43),

$$\begin{aligned}
 1 - d_2 c_1 \frac{k_2}{k_1} &= 0; \\
 d_2 &= \frac{k_1}{k_2 c_1} = \frac{1}{a_1 a_2 c_1}; \quad (3.56)
 \end{aligned}$$

$$\begin{aligned}
 d_1 - d_2 k_2 \left(\frac{c_1}{k_1} - c_2 \right) &= 0; \\
 d_1 &= 1 - \frac{c_2}{a_1 a_2 c_1} \quad (3.57)
 \end{aligned}$$

For correct reproduction of signal $X(z)$, scaling of the signal should be performed by using a suitable value of gain coefficient d_{21} . The following value of d_{21} is obtained from the above derivation by equating the term $X(z)$ to 1 such that equation (3.43) is satisfied. The term $(d_{21} k_2 a_1 b_1 c_1 z^{-2} - d_{21} k_2 a_1 b_1 c_1 z^{-3})$ is a first order differentiation of the input signal and can be eliminated from the derivation of the gain coefficient d_{21} .

$$d_{21}k_2a_1a_2b_2c_1 = 1;$$

$$d_{21} = \frac{1}{k_2a_1a_2b_2c_1} \quad (3.58)$$

The above derivation is a generic method or an empirical formula for finding gain coefficients of the proposed cascaded modulator. In practice, the delta sigma modulators are non-linear systems with arbitrary quantizer gain. The equations derived for the cascaded feedback and feed-forward delta sigma modulators are based on a linear model, which is an approximation to the non-linear delta sigma modulator. The coefficients were normalized and slightly adjusted to obtain best SNR values. Simulations were performed using the normalized coefficients and satisfactory results complying with Matlab were obtained. These coefficients were therefore used to design and implement the cascaded feed-forward delta sigma modulator.

4 ARCHITECTURES OF DELTA SIGMA MODULATORS

There is extensive use of analog-to-digital converters (ADCs) in various applications such as wireless receivers, telemetry, and instrumentation. Different types of ADCs are available for various applications. Appendix A reviews basic ADC design, such as flash ADC, two-step flash ADC, successive approximation (SAR) ADC, and pipeline ADC. In wireless receivers, high accuracy, low power, and low noise are some of the key attributes required of an ADC. The designs discussed in Appendix A are not suitable for high-performance wireless applications. The sigma-delta ADC introduced in Chapter 3 is the closest to meeting requirements for wireless applications. In this chapter, various architectures of sigma-delta modulators will be described. The sigma delta modulators are classified into two categories feedback modulators and feed-forward modulators. A comprehensive survey of various feedback and feed-forward delta sigma modulator topologies is provided. A detailed discussion of the proposed cascaded feed-forward third order delta sigma modulator along with its linear model is presented. This linear model is simulated using Matlab in Appendix C. The performance evaluation of ADCs in terms of stability, power consumption, accuracy, and desired SNR will be addressed.

4.1 First Order Single-bit Delta Sigma Modulator

Gray provided detailed information about first-order single-bit sigma-delta converter in [1] and [2]. Various issues such as noise shaping, stability, accuracy were dealt with. Figure 4.1 shows the basic structure of a first-order single-bit sigma-delta modulator. The figure shows a single-feedback loop with an integrator/loop filter, a quantizer (1-bit ADC) in the forward path, and a 1-bit DAC in the feedback path. The 1-bit ADC is a comparator and the 1-bit DAC simply switches between positive and negative reference values. The first order delta sigma modulator is inherently stable, since it uses only one loop filter. The feedback loop has just one level DAC; as a result, linearity is preserved. Single loop single-bit modulators are compact with low power consumption but have low resolution, low noise shaping, and therefore are not suitable for high performance applications.

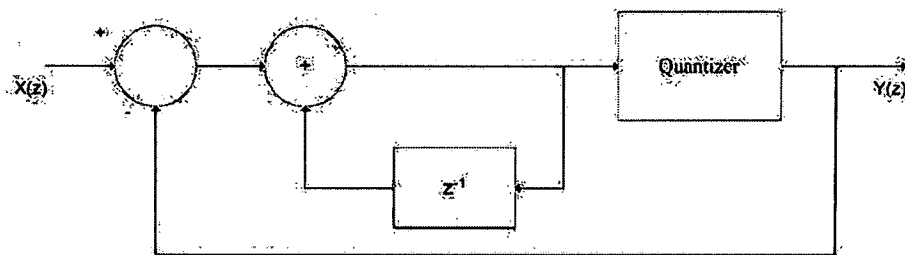


Figure 4.1 First order single-bit delta sigma modulator.

4.2 Second Order Single-bit Delta Sigma Modulator

The second order modulators, shown in Figure 4.2, presented by (He *et al.* [3] and Candy [4]) are a little more complex in terms of hardware and consume more power, since they

have two loop filters instead of just one as in the case of first order modulators. However, they have better resolution and noise shaping compared to the first order modulators. Second order modulators are generally stable, but too much increase in gain error will cause instability. They do not provide enough noise shaping and resolution for our broadband wireless application.

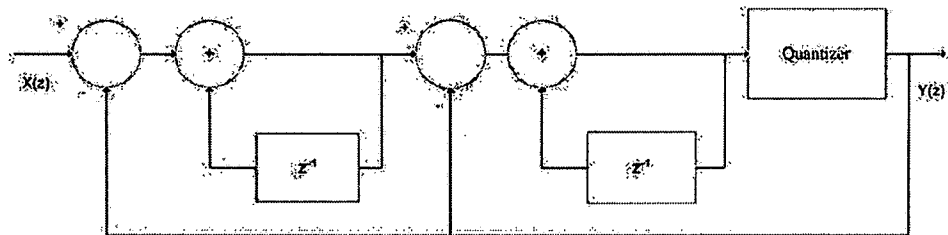


Figure 4.2 Second order single-bit delta sigma modulator.

4.3 Second Order Modulator with Multi-bit Quantizer

The second order modulator [5] with multi-bit quantizer, seen in Figure 4.3, adds additional complexity to the design because of potential non-linearity in multi-level DACs. The multi-bit quantizer increases noise-shaping and resolution but needs a dynamic matching or a digital correction element depending upon the nonlinearity introduced by DAC at input of each integrator.

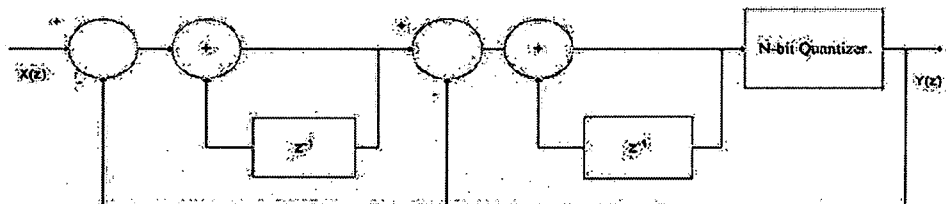


Figure 4.3 Second order modulator with multi-bit quantizer.

4.4 Higher order Single-bit or Multi-bit Modulators

Figure 4.4 shows the architecture of higher order single/multi-bit sigma-delta modulators that can be used to obtain the required accuracy and noise shaping. The problem with higher-order single-bit modulators is stability as mentioned by Brandt *et al.* [5]. Higher order single/multi-bit converters have more than two loop filters or integrators. Because of additional integrators, the output becomes prone to instability. The resolution and noise shaping increases but so does the power and hardware required to design these modulators. More noise shaping can be obtained by using a multi-bit quantizer. However, the use of multi-level DAC in the feed-back path places additional constraints on the higher order modulators. Higher order multi-bit single stage modulators not only have stability problems but also have non-linearity problems due to the multilevel DAC. Dynamic element matching (DEM) and digital correction are two of the techniques to counteract the non-linearity of the DAC. This is shown by Carley [6], Walden *et al.* [7] and Yasuda *et al.* [8]. The errors generated by using a multi-level DAC in these systems are expressed by Adams *et al.* [9,11] and Galton *et al.* [10].

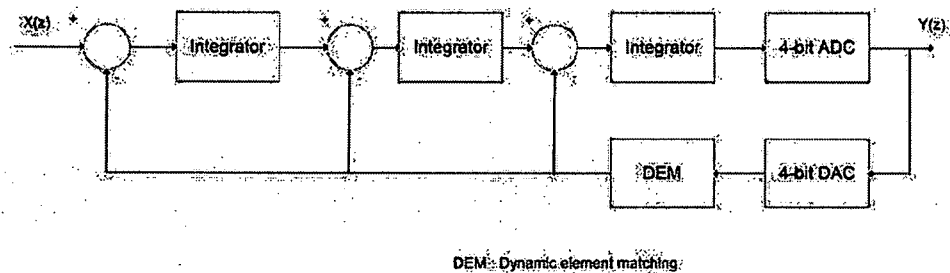


Figure 4.4 Higher order single-bit or multi-bit modulators.

4.5 Cascaded Single-bit Delta Sigma Modulator

Matsuya *et al.* [12], in order to get around the stability problem, has cascaded inherently stable first order sigma-delta architectures. The nonlinearity and instability in single stage higher order modulators can be eliminated by cascading stable single order single-bit modulators as shown in Figure 4.5. The first stage is cascaded with the second stage to form higher order modulators. The linearity of the system is preserved by the single bit DAC in the feedback path. The power and hardware of cascaded higher order modulator is the same as the single stage higher order modulator. A second order modulator can be formed by cascading two first order modulators. However, these modulators do not provide enough stop-band attenuation due to the use of single bit quantizers.

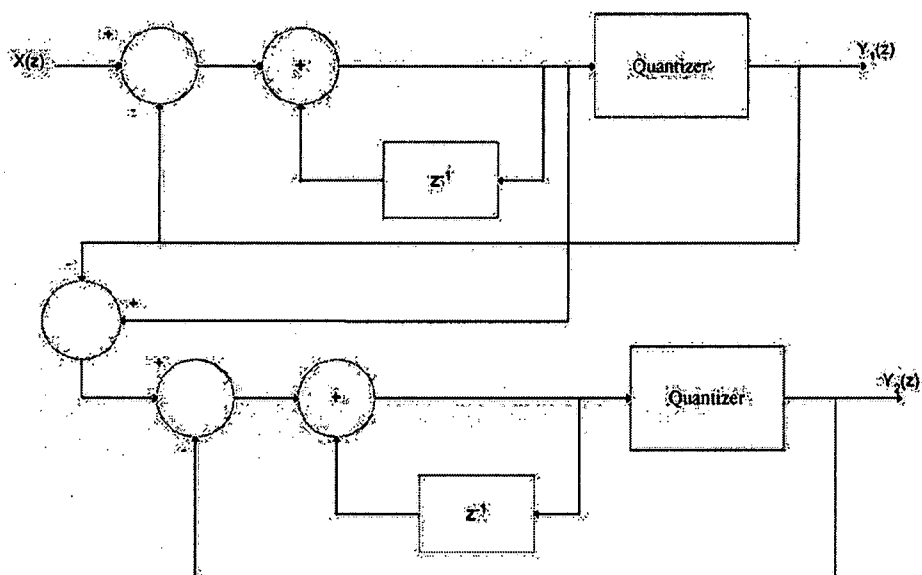


Figure 4.5 Cascaded single-bit delta sigma modulator.

Higher order modulators can be obtained by cascading several stages of first or second order modulators. Rebeschini *et al.* [13] performs cascade of three first order delta sigma modulator to obtain third order shaping as shown in Figure 4.6. The use of more than three stages should be avoided. There is a serious problem of cascading three or more stages if there are gain errors and noise leakage. Higher noise shaping is not advisable when noise leakage and gain errors are dominant.

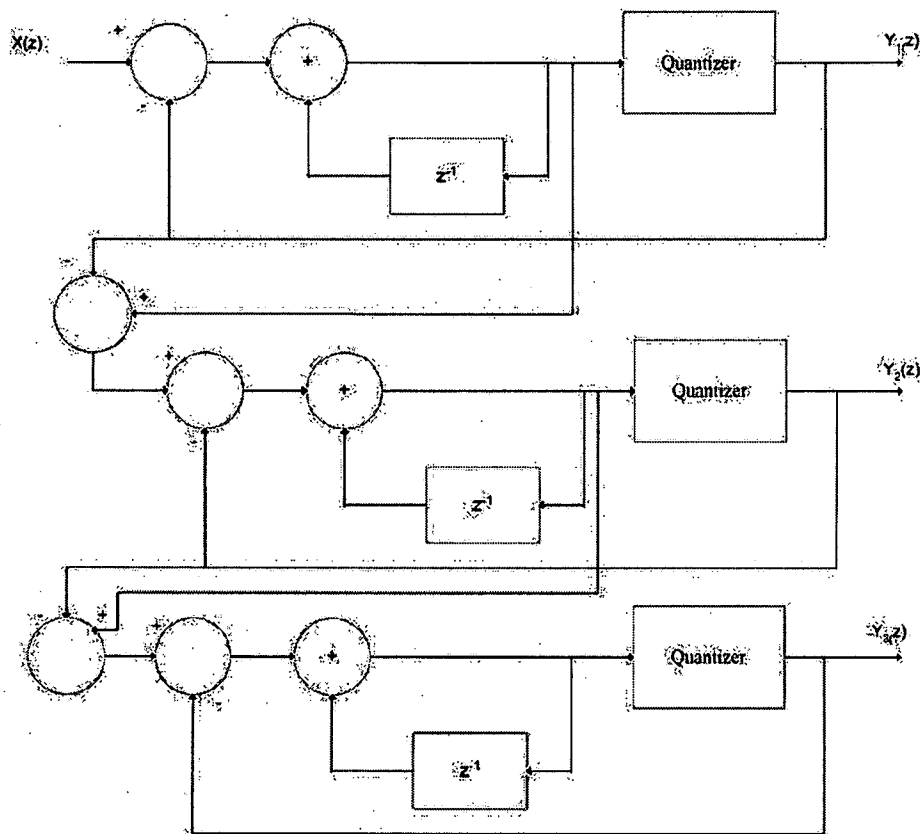


Figure 4.6 Cascaded single-bit higher order delta sigma modulator.

The architectures in [12] and [13] use a first-order sigma-delta loop in the first stage. For these designs, the noise fed-forward to next stage in the cascade is higher and in presence of gain errors detrimental to the entire system.

4.6 Cascaded Multi-bit Higher Order Modulators

The cascaded multi-bit higher-order modulator, designed using a cascade of second-order modulators, is very complex because they use two integrators in each stage. More noise shaping and high resolution is obtained by using multi-bit quantizer in each stage as given by Longo *et al.* [14]. Furthermore, considerable area and power is required to implement the higher-order modulators. A fourth order modulator, shown in Figure 4.7, is designed using cascade of two second order modulators. To reduce the non-linearity problems, one should have only 1-bit quantizer in the first stage. If there is a multi-bit quantizer in the first stage, then one has to deal with nonlinearity of multi-level DAC in the first stage. On the other hand, one can have a multi-bit quantizer in the second-stage, since the cascade shapes the noise away from the signal bandwidth.

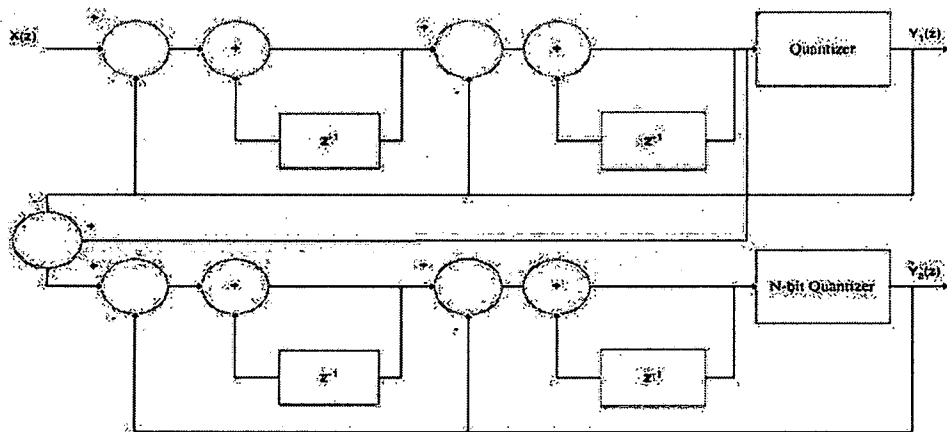


Figure 4.7 Cascaded multi-bit higher order delta sigma modulator.

Longo *et al.* [14] cascaded a second-order and first-order single bit stages to get third-order noise shaping and the desired resolution. By using second-order delta sigma modulator in the first stage, the gain errors are reduced and additional noise shaping is possible. Higher order single-loop delta sigma modulators are not used due to stability problems. Since these architectures are using single-bit quantizer to avoid non-linearity problems, there was not enough noise shaping. The concept of shaping noise using dual quantization architecture was introduced by Brandt *et al.* [11] and Williams *et al.* [15]. ADCs for various wireless receiver applications are designed in [17, 18, 19, and 20]. ADCs for broadband applications like ADSL are designed in [21, 22].

The ADC architectures, previously mentioned, have been implemented using conventional topologies with distributed feedback. The feedback topologies put many constraints on the internal nodes. In feedback architectures, the DAC is fed back to the input of each integrator. The integrators have infinite gain at DC and since the DAC has a DC output; there are additional constraints on the integrators to counteract the DC output and avoid instability. Larger integrators can have larger swings which may exceed supply voltage limitations. The instability in integrators can be alleviated by using resistors in parallel with the feed-back capacitors. This introduces non-idealities in the integrators since these resistors need to be small to reduce the DC offsets that cause instability. The feedback integrators are therefore power hungry because they need large switched capacitors to compensate for the swings generated by integrators.

4.7 Feed-forward Architecture with Feedback Coefficients

The feed-forward delta sigma modulators can be designed with feedback coefficients [23, 24] as seen in Figure 4.8. The gain of each loop can be adjusted independently and system can be made very stable. The noise shaping can be improved but the order of loop filter has to be increased since it is single loop architecture. Increasing the order of the loop filters also increases complexity because more integrators are required. The internal feedback paths limit the gain of the last two integrators and effectively reduce the resolution.

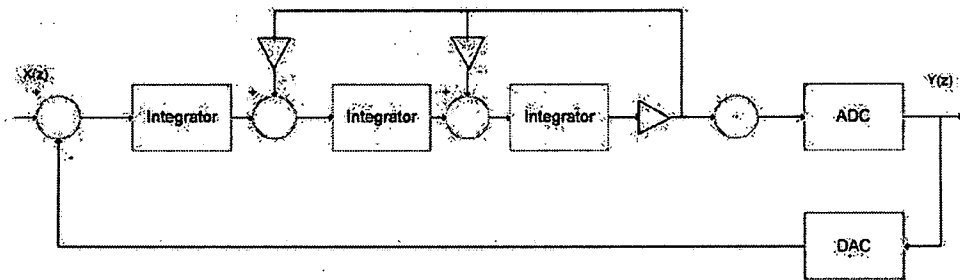


Figure 4.8 Feed-forward Architecture with feedback coefficients.

4.8 Hybrid Feed-forward Topology

The Hybrid feed-forward topology shown in Figure 4.9 is also a single-loop modulator but uses two or more feedback DACs [24]. This is a major disadvantage in the hybrid architecture. Sensitivity and complexity is also an issue in these architectures. The noise shaping, power and area required is same as the single loop feed-back architectures.

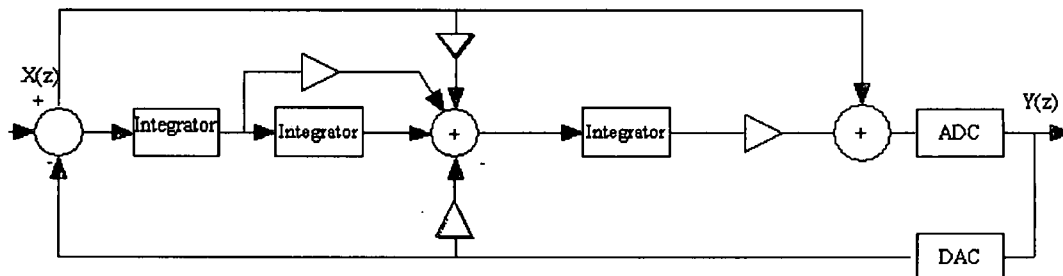


Figure 4.9 Hybrid feed-forward topology.

4.9 Simple Feed-forward Architecture

The simple feed forward architecture shown in Figure 4.10 provides a simple zero in the transfer function of each integrator [45], but the gain of each loop filter cannot be adjusted independently; in addition, it is not possible to implement any transfer function because of the position of the zeros. The noise shaping, power and area required is the same as the single loop feed-back architectures, but the complexity is less since there is only a single DAC.

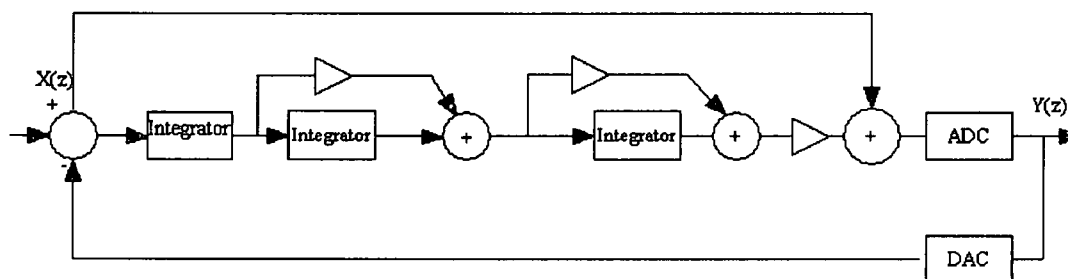


Figure 4.10 Simple feed-forward architecture.

None of these architectures provide a balance in terms of power consumption, area, and resolution. A multi-bit quantizer or a cascade architecture, which improves noise shaping and resolution at relatively low power and hardware are not included in these designs. Our proposed cascaded multi-bit third order feed-forward delta sigma converter will be explained in the following section.

4.10 Proposed Cascaded Third Order Feed-forward Delta Sigma ADC

A linear model of the cascaded third order modulator with feed-forward elements and multi-bit quantizer is a novel approach in this dissertation shown in Figure 4.11.

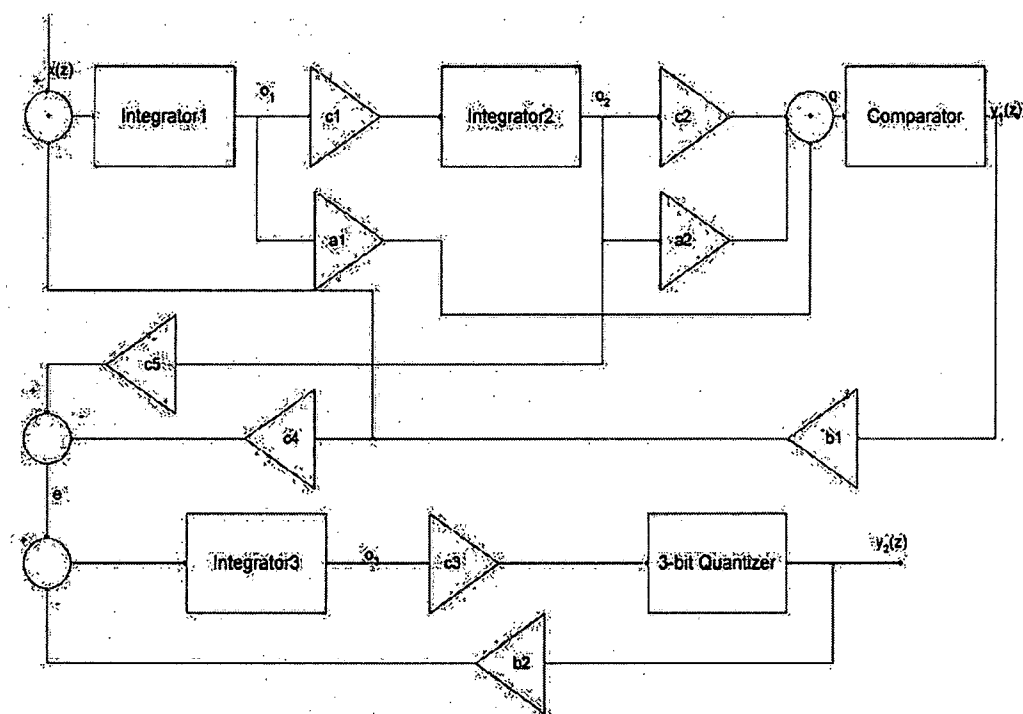


Figure 4.11 Cascaded third-order feed-forward delta sigma modulator.

There is considerable reduction in noise due to cascade of second order and first order ADC; in addition, the simple feed-forward elements with just one feedback path, makes this ADC architecture attractive for high performance ADCs in wireless applications. The advantages of this architecture over other architectures are:

1. The second order modulator is placed in the first stage of the cascade rather than the first order modulator. The noise that needs to be canceled is second order shaped instead of first order, so there is less in-band noise to be canceled [26]. If noise leaks from the first stage of the cascade, it will be second order shaped, and hence ADC has better tone and dither performance.
2. The first stage in the cascaded modulator has 1-bit ADC which exhibits linear quantization. Modulators with order more than two along with an N -bit ADC are complex and tend to get unstable. The second stage can have N -bit quantizer, since the input to the second stage modulator is linear. The non-linearity produced by N -bit quantizer is shaped away by the second order noise shaping of the first stage. This avoids the need for dynamic element matching. Third order single loop architectures have considerable non-linearity due to single loop and need dynamic matching elements [27]. Third order loops can become unstable due to too many feedbacks, whereas first-order and second-order modulators in the cascade are inherently stable.
3. The 3-bit quantizer in the second stage provides about 18-dB of additional SNR than a single bit quantizer. Increasing the order of modulation at low OSR does not improve the SNR by much, but increasing the quantizer bits at low OSR is very effective to an extent of 3 bits. If quantizer has more than 3 bits, there is not much improvement in the SNR at

the expense of more complexity. An increase in the quantizer bits is independent of the OSR [26].

4. Feed-forward (FF) architecture has better performance, stability and less complexity compared to its feedback counterpart. In a feed-forward topology, the output of the quantizer is fed back only to the input node, and input to the quantizer is obtained by summing the output of each integrator. The main feature of the FF architecture is that it has only one global feedback and hence a single DAC. This is useful in multi-bit architectures where the implementation of a multi-level DAC is quite complicated. FF architectures can be shown to have better suppression of the disturbances generated at the loop filter internal nodes than the FB architectures [27]. Hence a simple FF architecture is chosen to implement the proposed ADC in Figure 4.11.

4.11 Sub-Components within the Proposed ADC

This section will describe some of the sub-components used in the proposed delta sigma ADC. The discrete time integrator is a key sub-component of the ADC. In switched capacitor (SC) integrators, the resistor in the continuous-time integrators is replaced by NMOS switches and capacitors. The gain of the SC integrator is a ratio of the two capacitors. Capacitance value in CMOS technology can be matched more closely than resistance values. Thus the gain of SC integrators is more accurate than that for the continuous-time integrators. A high performance operational amplifier (op-amp) in the integrators acts strongly in avoiding gain and leakage errors. The operational amplifier needs to have good slewing rate and considerable gain to reduce the nonlinearity of the

integrator and maintain high SNR of the modulator. An op-amp should have good bandwidth and settling time to avoid gain errors that lead to leakage of noise [27].

A comparator acts as 1 bit ADC to compare the analog input signal with a predetermined reference signal and output a digital signal (1 or 0). The offset and hysteresis of the comparator will be shaped away by the second order noise shaping [16]. Nevertheless a high performance comparator is better since it can track differences between small signals. A clocked comparator is used for this purpose. 2^N-1 comparators are present in N -bit quantizer because one comparator is needed for each bit conversion. The input transistors of the comparators should not be too large otherwise the input capacitance will be large and consequently serious loading effects will slow down its operation. The 3-bit ADC/DAC will be implemented using a single resistor string to save area and power. The 3-bit ADC is a typical flash design for high speed conversion in a single clock cycle and the 3-bit DAC is a simple differential resistor array type design.

4.12 Linear Model of the Cascaded Feed-forward Delta Sigma Modulator

The designed cascaded third-order feed-forward delta sigma modulator is shown in Figure 4.11. The second-order section is cascaded with the first-order loop to obtain third-order delta sigma architecture. A frequency which is an integer multiple of the sampling frequency must be used for coherent sampling. If the coherent sampling principle is not satisfied, side effects such as picket fence and spectral leakage take place reducing the SNR of the system [29].

The a_1 and a_2 parameters, as shown in the Figure 4.11, are the feed-forward elements.

These are parameters of a low pass Butterworth or Chebyshev filter. They are generally obtained using a recursive algorithm to generate a desirable stop-band cut-off frequency and reasonable pass-band gain. The frequency response of this filter is a high pass filter with a gain normalized to 1.5. The feedback factor b_1 and b_2 of both the modulators is chosen as unity in this design. The parameters c_1 , c_2 , and c_3 are the gain factors used to scale the output of the integrators within the finite linear range of the operational amplifiers. The noise shaping parameters c_4 and c_5 are employed to scale the quantization noise. This coarse quantization noise is passed through a multi-bit first order modulator to convert it into fine quantization noise. The c_4 and c_5 parameters are very critical in shaping the quantization noise and determining the SNR for optimum performance.

Low signal amplitudes decrease the signal strength, increase the quantization noise and drop the SNR. The signal strength should be improved by increasing c_5 to get better SNR. Also the c_4 gain term which is multiplied with the digital output must be scaled appropriately. Large quantization noise e , which is the difference between the output of second order modulator and the second integrator output causes saturation and ultimately decreases the SNR. To keep the quantization noise or the input to the next stage within the linear range of operation, c_4 and c_5 must be appropriately chosen. Several simulations were performed to obtain suitable values of c_4 and c_5 for best SNR results.

In hardware implementation, the maximum linear range of operation of integrators for single power supply of 2.5 V is typically between 0.4 V - 2.1 V, limited by the threshold voltage of 0.36V for the NMOS and -0.41V for PMOS transistors on either

side of the supply voltage. We are using NMOS input transistors for the op-amp, and since NMOS transistors have strong conduction of low voltage, they serve two purposes: 1. they can accept low input amplitudes, and 2. they can operate at high speeds. The input common mode voltage can be slightly decreased to have a better dynamic range for the input, while maintaining the linear range of operation. The operation of this architecture is as follows. The output produced by the first integrator is o_1 , which is the sum of the analog input signal and the error signal. The error signal is the difference between the analog input and the analog output of DAC. The output of the second integrator o_2 is the sum of its delayed version and the scaled output of the first integrator. The output of the quantizer q is the summation of the scaled first integrator output and the scaled second integrator output. The quantization noise e , the input to the next stage is subtracted by the DAC output and accumulated in the third integrator. The output of the third integrator o_3 is quantized using a 3-bit quantizer.

The second order modulator output and the first order modulator output undergo digital error correction process as shown in Figure 4.12. The output of the first order modulator is scaled and differentiated twice to counteract the integration process in the second order modulator. The digital output of the second order modulator is scaled and delayed to obtain synchronization with output of the first order modulator. The scaling of the digital outputs is needed because sub-unity parameters c_4 and c_5 are used to obtain the quantization noise input to the next stage. In order to obtain unity signal transfer function, digital outputs also have to be scaled appropriately. This can be seen from the Matlab code presented in Appendix C.4.

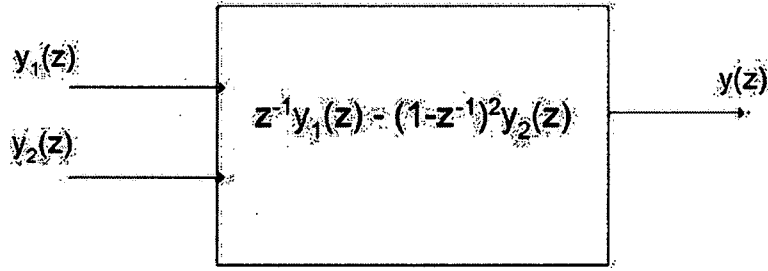


Figure 4.12 Digital error correction.

Equations (4.1) and (4.2) express the output of the second and first order modulator, respectively. Simplifying equations (4.1) and (4.2), we get equation (4.3), which shows that the quantization noise of the second stage is attenuated in the base-band by third order shaping. Equation (4.4) shows how digital error correction logic is applied to get the cascaded output y .

$$y_1(z) = z^{-1}x(z) + (1 - z^{-1})^2 E_1(z) \quad (4.1)$$

$$y_2(z) = z^{-1} [E_1(z) - E_3(z)] + (1 - z^{-1}) E_2(z) \quad (4.2)$$

$$y(z) = z^{-2}x(z) + z^{-1} (1 - z^{-1})^2 E_3(z) - (1 - z^{-1})^3 E_2(z) \quad (4.3)$$

where $E_1(z)$ = quantization noise of the first stage 1-bit quantizer,

$E_2(z)$ = quantization noise of the second stage 3-bit quantizer,

$E_3(z)$ = non-linearity error of 3-bit DAC.

$$y(z) = z^{-1}y_1(z) + (1 - z^{-1})^2 y_2(z) \quad (4.4)$$

The cascaded output was subjected to signal processing to validate the performance of the modulator. A list of the static and dynamic parameters for ADC/DAC is given in Appendix B. The output was analyzed to verify whether the requirements for the dynamic performance of the system are satisfied. The following are the performance

parameters which can be derived from the modulator.

1. SFDR

SFDR is the spurious free dynamic range of the modulator and is the difference between the highest signal component and the highest noise component of the noise floor.

2. SINAD

SINAD is ratio of the signal to noise plus distortion. The noise plus distortion includes all the noise present in the system due to harmonics and distortion surrounding it.

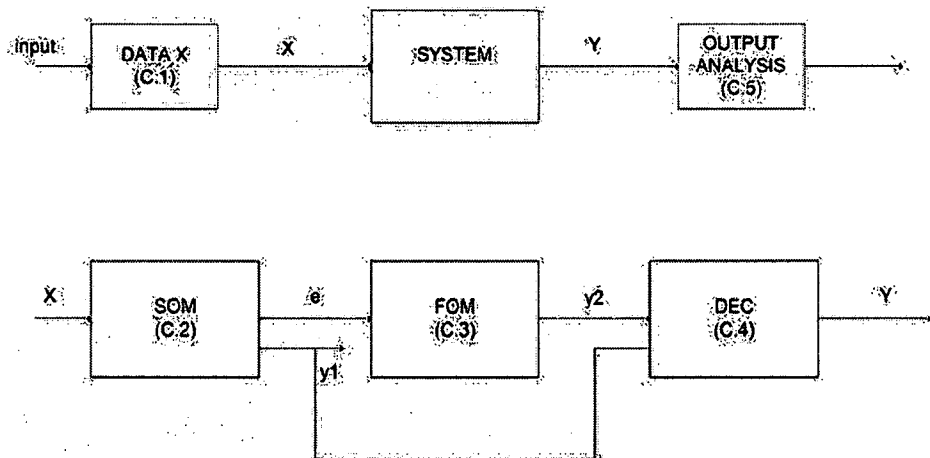
3. SNR

SNR is the signal to noise ratio. The noise floor, in this case, is the sum of the noise present in the system, excluding the harmonics.

4. ENOB

The ENOB is the effective number of bits or simply resolution. It signifies the performance of the modulator.

The linear model for the proposed architecture is shown in Figure 4.13(a) and (b).



SOM: Second order modulator,
 FOM: First order modulator,
 DEC: Digital error correction.

Figure 4.13(a) Testing of delta sigma modulator. (b) System design of delta sigma modulator.

Figure 4.13 (a) shows the entire testing process from the data input to the system to the output analysis. A sinusoidal input signal with a frequency of 156.25 KHz was generated using a sample code shown in Appendix C.1, and was fed to the system. The signal frequency was chosen such that it obeys the coherent sampling principle, where the signal frequency must be an integer of the sampling frequency to avoid spectral leakage. In order to maintain consistency with the Simulink model, design and implementation in Cadence, the Matlab algorithm of the proposed cascaded delta sigma architecture use the same gain coefficients and the digital error correction logic. The system in Figure 4.13 (a) consists of a second order modulator, first order modulator, and the digital error correction logic. This realization is shown in Figure 4.13 (b). The second order modulator is modeled using the linear equation given in equation (4.1), and whose Matlab code can be seen in Appendix C.2. The first order modulator is obtained using

equation (4.2) with the corresponding code in Appendix C.3. Equation (4.3) shows the digital error correction logic employed to obtain the cascaded output. The Matlab code for this function is given in Appendix C.4. The cascaded output is processed using signal processing algorithm to analyze various dynamic performance parameters. The signal processing algorithm written in Matlab is given in Appendix C.5. The Matlab code and plots for the output spectra of the second-order modulator, the first-order modulator, and the power spectral density of the cascaded modulator are included in Appendix C.6. The SNR and SINAD calculated of the proposed delta sigma modulator from the Matlab algorithm is 74.26 dB and 69 dB, respectively. The resolution obtained from the Matlab algorithm is 12.04 bits.

5 INTEGRATED CIRCUIT DESIGN

In this chapter, we will discuss several integrated circuits used in the design of the overall architecture of the delta sigma modulator. These components include operational amplifiers (op-amp), comparators, switched capacitor integrators, high speed flash analog-to-digital converters (ADC), and digital-to-analog converters (DAC). A complete description and detailed analysis of each component follows next.

5.1 Operational Amplifier Design

The CMOS operational amplifier plays a very important role in the overall design of any integrated circuit. In this dissertation, operational amplifier is an integral part of a switched capacitor integrator. The operational amplifier is responsible in determining the power dissipation, dynamic range of the overall system, and hardware requirements. Furthermore, an operational amplifier or simply an op-amp limits the frequency of operation of the entire circuit.

5.1.1 Properties of Operational Amplifier

Ideally, this active device is a voltage controlled voltage source (VCVS) with infinite voltage gain, infinite input impedance and zero output impedance. An ideal op-amp is temperature independent, free from noise distortion and has no limitations on the frequency of operation. Practically, there are several factors which create differences between the ideal op-amp and the practical device. Most of these differences are

enumerated below as in [49].

1. DC gain

An ideal op-amp has an infinite DC gain but real op-amp devices have low frequency DC gain of around 10^3 to 10^6 .

2. Unity gain bandwidth

A typical CMOS op-amp can have a unity gain bandwidth, which can extend anywhere from tens of MHz to hundreds of MHz. The practical op-amp is affected by loading effects of the parasitic and stray capacitances which decrease the unity gain bandwidth.

3. Linear range of operation

An ideal op-amp has full range of linear operation from the positive DC power supply to the negative power supply. However, in practical op-amps this linear range of operation is limited by $V_{ds_{sat}}$ which decreases the linear range by a few hundredths of volts below the positive power supply and increases by a similar amount above the negative power supply.

4. Slew rate

Slew rate is the maximum rate of change of voltage dV/dt . Slew rate is generally calculated for large input voltages. A large input voltage can drive the op-amp out of its finite linear range of operation; this hampers the op-amps ability to follow the input, finally affecting the speed of operation. A typical CMOS operational amplifier has slew rates ranging from 100 to 1000 V/ μ s.

5. Settling time

Settling time is the time taken for charging and discharging a capacitor to reach steady state value after the transients have transpired. The settling time directly affects the unity

gain frequency and limits the maximum clock frequency. As a general rule, it takes at least five times the time constant τ for correct settling within the desired period of operation.

6. Input offset voltage

In the ideal op-amp the two input terminals are short circuited and the input offset voltage is zero. In real devices, since the input impedance is finite, there is a difference of a few tens of mV between the two terminals. This difference is the input offset voltage and is modeled by a voltage in series with one of the input terminals depending upon the polarity of the voltage. The typical input offset voltage of CMOS op-amps is 2 to 10 mV.

7. Nonzero output resistance

In real op-amp devices, the output impedance is not zero. This nonzero output resistance is of the order of 100 to 5k Ω in buffered op-amps and 1 to 4 M Ω in un-buffered op-amp. The non-zero output resistance affects the speed with which the output capacitance can be charged; therefore the highest input signal frequency.

8. Noise distortion

The input transistors of the op-amp have in-built switch resistance which generates noise at the output of the op-amp. This distortion can be thought of noise voltage V_n/A in series with the input voltage. This voltage can be large in MOSFETS than in bipolar transistors.

9. Dynamic range

Dynamic range is the difference in the maximum input voltage and the minimum detectable input voltage considering non-ideal effects such as noise distortion, capacitive and clock feed-through. Dynamic range is usually specified in dB scale with respect to

the input signal. It is given as $20\log_{10}(V_{imax}/V_{imin})$. The typical values for dynamic range are 70 to 100 dB.

10. Common-mode rejection ratio (CMRR)

This parameter determines the suppression of noise since it establishes a ratio between the differential gain A_d and the common mode gain A_c . The common mode gain is the gain due to presence of voltages common to both input terminals of the op-amp. Ideally the differential gain is infinite and common mode gain is zero generating an infinite CMRR. Practical op-amps have CMRR in range of 80 to 100 in decibels.

To summarize, careful attention must be paid to the design of op-amps for reasonable performance in terms of hardware utility, power consumption, and efficiency to produce output with minimal non-ideal effects. Operational amplifiers are mainly classified into single-ended output op-amps and differential-ended output op-amps. The differential-ended output op-amps, otherwise known as fully differential operational amplifiers, have several advantages over single-ended output op-amps [26], and are therefore emphasized in this chapter. Some of the benefits of the fully differential design over single-ended op-amps are stable input common mode voltage, reduction of harmonic distortion, doubling of output voltage swing and suppression of coupled noise due to substrate and power lines. Fully differential operational amplifiers have positive and negative polarities for both the input and the output signals whereas the signal-ended output op-amp has differential polarities only at the input terminal. This doubles the voltage swing at the output of the fully differential op-amp and improves the dynamic range of input signals. Fully differential op-amps also reduce the harmonic distortion since the even order terms of distortion will be eliminated. The input common mode voltage of the two input

terminals is maintained at a constant value and increased rejection of noise from substrate and power lines are other features of these op-amps. They have the attribute of canceling all the common-mode signals because of their differential nature on both the input and the output terminals.

This differential op-amp implementation is used in the fully differential design of switched capacitor integrators. The signal to noise ratio (SNR) is dominated by the kT/C thermal noise. In differential implementation of switched capacitor integrator, twice the number of switches and capacitors are needed. This increases the SNR or the noise floor by 3 dB. However, a differential design doubles the signal strength which increases the signal power by 6 dB. For the same SNR, the sizes of the capacitances in the differential implementation can be halved, which reduces the power consumption at no change in the settling time. The area or die size is thus approximately the same as the single ended implementation. To counteract the non-idealities and meet the performance requirements, an appropriate topology for the operational amplifier must be selected. Also, lower power consumption and minimal hardware requirement are other considerations for the operational amplifier design. Thus the goal is to investigate an op-amp topology which satisfies most of the above criteria. A few operational amplifiers, which serve as good candidates for our proposed design will be discussed next.

5.2 Topologies for Operational Amplifiers

The three main architectures for the design of operational transconductance amplifiers (OTA) are Miller compensated, telescopic cascode and folded cascode. The advantages and disadvantages of these architectures are summarized. Again, the need is to

investigate an OTA with low power characteristics without the expense of speed and performance requirements. Since power and noise trade off, and high resolution is desired, we need to strike a balance between power and the SNR for fixed settling time. The required characteristics for a desirable OTA design are necessity of NMOS input transistors for high speed of operation, minimizing power consumption by minimizing the current branches in the architecture, increasing the output dynamic range by using less devices that cause thermal noise, and improving the unity gain bandwidth by utilizing less capacitive elements.

5.2.1 Two Stage Miller Compensated OTA

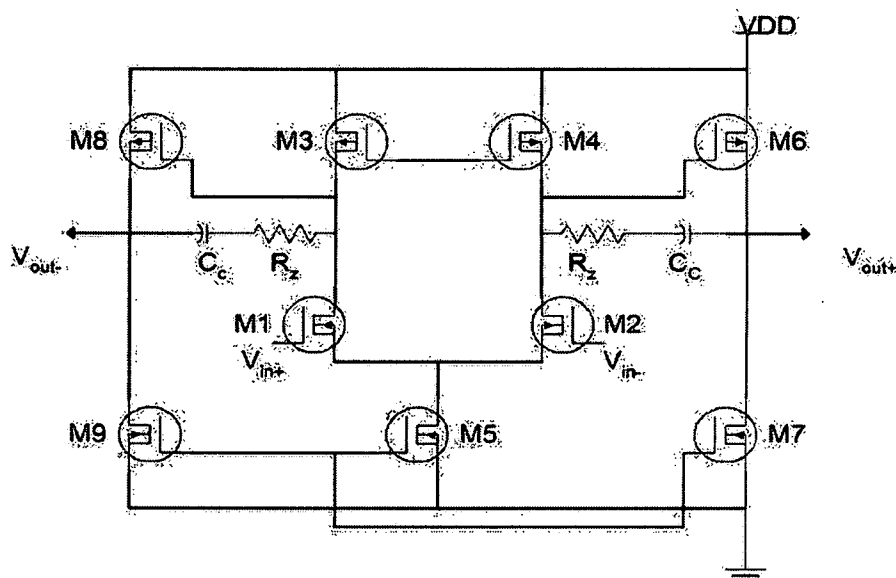


Figure 5.1 Miller compensated fully differential OTA.

Figure 5.1 shows the design of the two-stage Miller compensated OTA as appeared in [50]. This OTA achieves significantly high gain from the differential cascade pair in conjunction with the common source amplifier. The output voltage swing or dynamic range of this design is high since only two transistors are present at the output. This helps in achieving better SNR at power supply well below 2.5 V. However, a compensation

capacitor and a resistor or a MOSFET is needed between the two stages, that is, the differential cascade pair and the common source amplifier for stability during the feedback operation. This is a major drawback of this design because it reduces the unity gain bandwidth and the speed of operation. Moreover, the design has four current branches and requires two common mode feedback circuits, which not only increases the power consumption but also the area of the circuit.

5.2.2 Telescopic Cascode OTA

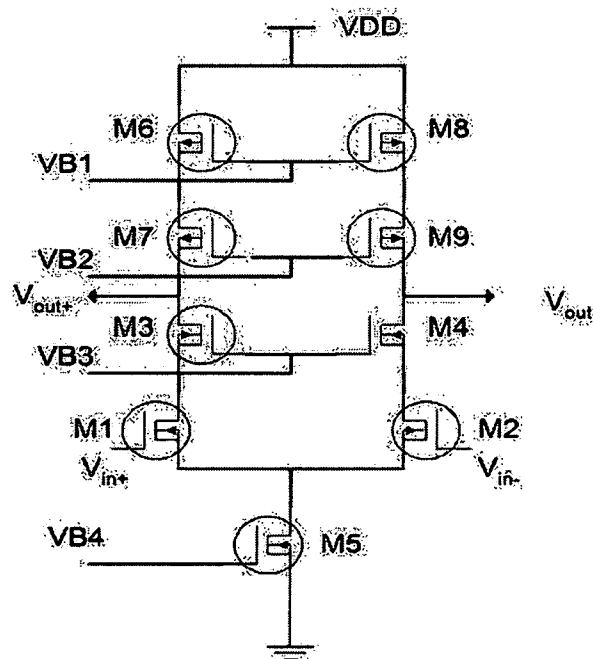


Figure 5.2 Telescopic cascode OTA.

A Telescopic cascode OTA is shown in Figure 5.2 in [51]. The transconductance of the cascode transistors $M3$ and $M4$ along with the parasitic capacitances of the input transistors $M1$ and $M2$ create a high non-dominant second pole [52]. The voltage gain of this design can be very high due high output resistance. There are only two current branches, which substantially improve the power consumption. The main disadvantage

of this design is that the output swing is considerably low because of the number of devices at the output. Also, the noise floor increases and it is difficult to obtain good resolution at voltages lower than 3.3 V. Another drawback of telescopic cascode OTA is that the input common mode level has to be set accurately and has to match the output common mode level. The reduced input and output common mode voltage further reduce the linear range of operation.

5.2.3 Folded Cascode OTA

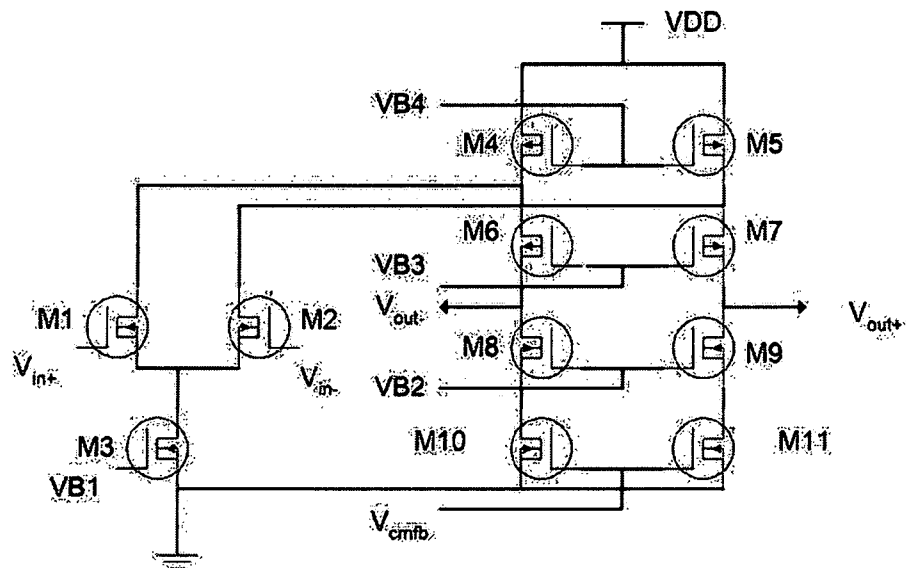


Figure 5.3 Folded cascode OTA.

The folded cascode OTA, shown in Figure 5.3, is similar to the telescopic cascode OTA, and has gain that is obtained by multiplying the input transconductance with the output resistance [51]. The folded cascode OTA has a much improved output signal swing compared to the telescopic cascode OTA since it has fewer transistors at the output stage. The other advantage over the previous design is that the input common mode and the output common mode voltage need not be identical; hence, the output dynamic range can

be further improved. Since it is a single-stage op-amp, the output capacitance acts as a compensation capacitor to maintain stability, and no additional capacitors or MOSFETS are needed. Although both compensation techniques maintain stability in feedback mode of operation, the one using output capacitance increases the speed of operation compared to the compensation capacitor of the two-stage OTA. The folded cascode OTA has a little more power consumption than the telescopic design but it has low noise capabilities and high SNR to provide the required resolution of 12-bits at a low power supply voltage of 2.5 V. The folded cascode design fits well in the scheme of things for our application and is elected over other architectures.

5.3 Common Mode Feedback Circuit

The disadvantage of using a fully differential amplifier is the need for the common mode feedback circuit (CMFB). Since the input voltages of the op-amp have equal bias at a common mode input voltage, the two output terminals of the operational amplifier must also be placed at a common mode output voltage. A circuit called common mode feedback (CMFB) is employed to sense the average value of the op-amp outputs. The output of the CMFB must be fed back into the op-amp to adjust the average value of the output terminals to the output common mode voltage. The common mode feedback makes the average of the outputs and the common mode voltage equal. There are two types of CMFB [51].

5.3.1 Continuous CMFB Using Resistor Divider

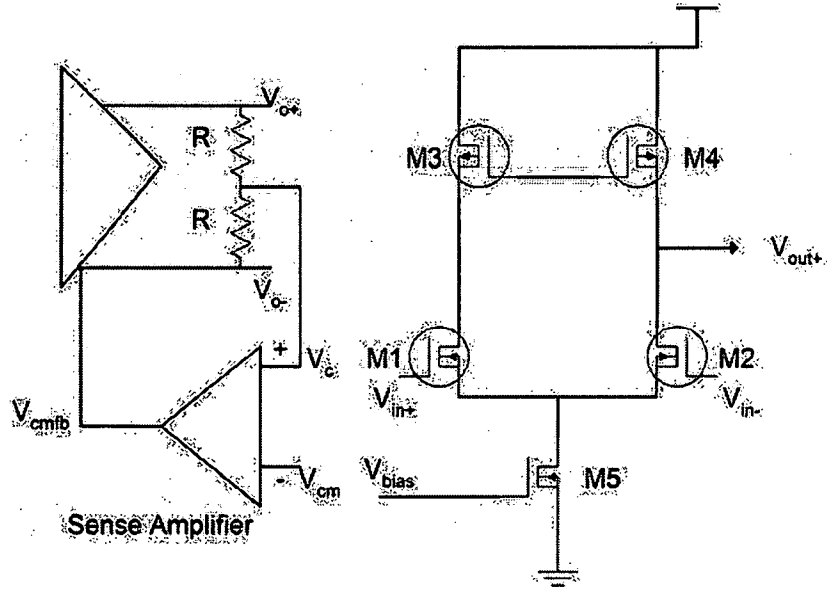


Figure 5. 4 (a) Continuous CMFB. (b) Sense amplifier.

Figure 5.4(a) and 5.4(b) show the continuous CMFB and sense amplifier circuits. In this CMFB design, two equal resistors R are used to obtain the average V_c of the two op-amp outputs. This voltage V_c is subtracted from the desired common mode output voltage V_{cm} and amplified by a sense amplifier. The sense amplifier consists of a source coupled pair $M1$ and $M2$, diode connected loads $M3$ and $M4$, and tail current source $M5$. The output of this amplifier V_{cmfb} is fed back into the op-amp to adjust the average value of the two output terminals. The equation which governs this relationship is given by equation (5.1).

$$V_{cmfb} = A(V_c - V_{cm}) + V_{bias} \quad (5.1)$$

If $V_c = V_{cm}$ then $V_{cmfb} = V_{bias}$. The V_{bias} voltage is set up $V_{bias} = V_{gs1} - V_{ss}$, where V_{gs1} (gate-source voltage of $M1$) is chosen such that the tail current $I_5 = I_3 + I_4$. The

disadvantage of this circuit is that the resistor R and the input capacitance of the sense amplifier introduce a pole in the transfer function which affects the output at high frequencies. The output swing is also limited by this circuit. Continuous CMFB designs have another disadvantage of resistor loading effect. The resistors R load the op-amp output and this reduces their differential gain unless the resistors are of a much higher value than the output resistance. This problem can be alleviated by adding source followers, however source followers introduce DC offsets which limit the output swing.

5.3.2 Switched Capacitor CMFB

To overcome resistive loading and reduced output swing, capacitors can be used to detect the common mode output voltage. The resistive output loading is eliminated, but the capacitors are open circuits at dc. To avoid dc bias problems, switched capacitors are used to detect output voltage and subtract it from the desired common mode output voltage. Figure 5.5 shows a typical switched capacitor CMFB.

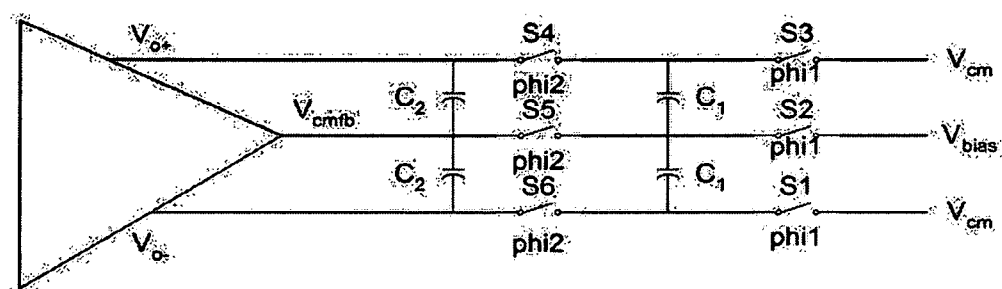


Figure 5.5 Switched capacitor CMFB.

Switches $S1$ - $S6$ are implemented using MOSFETS and identical capacitors C_1 and C_2 are used as voltage divider instead of resistors. When ϕ_1 is high, C_1 charges to $V_{cm} - V_{bias}$. When ϕ_2 is high, C_2 connects between V_c and V_{cmfb} . V_c is constant because V_{cm} and

V_{bias} are both steady state DC values and switched capacitor integrator operates in negative feedback mode. After V_c becomes constant, ϕ_{i1} does not transfer charge onto C_2 , when ϕ_{i2} is high. The charge conservation should hold true for switched capacitor CMFB. The charge transferred onto C_1 during ϕ_{i1} is same as the charge transferred onto C_2 during ϕ_{i2} then by equation (5.2)

$$Q(\phi_{i1}) = C_1 (V_c - V_{cm}) = Q(\phi_{i2}) = C_1 (V_c - V_{cmfb}) \quad (5.2)$$

The equation (5.2) reduces to equation (5.3)

$$V_{cm} - V_c = V_{bias} - V_{cmfb} \quad (5.3)$$

$V_c = V_{cm}$, if the bias voltage V_{bias} is similar to V_{cmfb}

5.4 Non-idealities in OTA

In practice, OTA experiences several non-idealities that degrade its performance and ability to achieve better results. The non-idealities of OTA such as finite DC gain, finite slew rate, finite linear settling time which affects the dominant pole, finite unity gain bandwidth, thermal noise, switch-on resistance, and loading effects are discussed next.

5.4.1 Finite DC Gain

By applying the charge conservation principle and combining the results obtained during the sampling and integrating phases as shown in Figures 5.6(a) and 5.6(b), respectively we can write the output of the switched capacitor integrator as in equation (5.4) [44].

$$V_{out}(z) = C_s \cdot P_2 \frac{(z^{-1}V_i(z) - z^{-1/2}V_{out}(z))}{C_i \left(1 - \frac{P_2}{P_1}\right)} z^{-1} \quad (5.4)$$

Where $V_i(z)$ and $V_{out}(z)$ are the input and the output signals in z domain. C_i and C_s are the

integrating and the sampling capacitors; p_1 , p_2 are closed loop static errors and f_{dc1} and f_{dc2} are capacitive feedback factors during sampling and integrating phases. They are given by equations (5.5), (5.6), (5.7), and (5.8).

$$P_1 = A * \frac{(f_{dc1})}{(1 + f_{dc1})} \quad (5.5)$$

$$P_2 = A * \frac{(f_{dc2})}{(1 + f_{dc2})} \quad (5.6)$$

Where

$$f_{dc1} = \frac{(C_i)}{(C_i + C_p)} \quad (5.7)$$

$$f_{dc2} = \frac{(C_i)}{(C_i + C_p + C_s)} \quad (5.8)$$

and C_p = parasitic capacitance, C_L = load capacitance of next stage

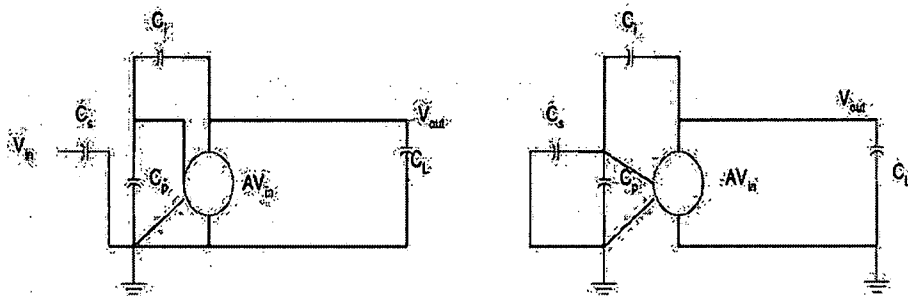


Figure 5.6 (a) Sampling phase and (b) Integration phase.

The finite OTA gain introduces gain and pole errors in the switched capacitor integrator. The gain error reduces the gain of the OTA by p_2 and the pole error moves the pole from DC ($z = 1$) to $z = p_2/p_1$. Both these errors depend upon the product of the OTA gain and

the capacitive feedback factors. The model described above does not take into account other parameters such as switch on resistance, closed loop dominant pole, nonlinearity of the gain and hence it is recommended [16] to expect gain A close to 60 dB. At 60 dB or above the charge transfer errors due to finite DC gain are almost eliminated and only charge loss due to capacitor mismatch remains.

5.4.2 Linear Settling Time and Finite Unity Gain Bandwidth

The finite unity gain bandwidth introduces a gain error in the switched capacitor integrator due to incomplete settling of op-amp outputs. The OTA needs sufficient bandwidth so that the signal can settle linearly with 1% accuracy within half the clock period. Consider the following transfer function of integrator during sampling period given in equation (5.9) [26]:

$$V_o(t) = V_i(1 - e^{\left(\frac{-T}{\tau}\right)}) \quad (5.9)$$

Where T = sampling period

$$\tau = \text{settling time constant} = \frac{1}{w_b}$$

w_b = unity gain bandwidth

$V_i(z)$ and $V_{out}(z)$ are the input and the output signals in z -domain. As stated in [16], at a fixed sampling rate, the term in parentheses reduces the gain of the integrator. About five periods of settling time constant will reduce the integrator gain by less than 1%. This criterion will be sufficient to avoid significant errors due to incomplete settling of op-amp outputs and produce high resolution circuits.

5.4.3 Slew Rate

Figure 5.6(b) shows the integration phase for the switched capacitor integrator since in this phase; conditions on slew rate limitations are more stringent. The slew rate (SR) phenomenon occurs mostly during the transfer of charge between the sampling period and the integration period, when the integrator is in feedback mode of operation. The slew rate during the integration phase is given by equation (5.10) [44]:

$$SR = \frac{I}{C_{eq}} \quad (5.10)$$

Where

$$C_{eq} = C_s + C_p + \frac{(C_i + C_p + C_s) \cdot C_L}{(C_i)}$$

C_i and C_s are the integrating and the sampling capacitors; C_p is parasitic capacitance, C_L is load capacitance of next stage.

From the above equation it can implied that the SR depends on the large overdrive voltage of input transistors because current is proportional to the square of the overdrive voltage. If the slew rate does not satisfy the requirements, then op-amp output does not settle properly and the entire circuit undergoes harmonic distortion [53]. The slew rate, being a non-linear effect, can produce harmonic distortion in the output. The harmonic distortion is a most serious and unwanted occurrence in the output spectrum. To avoid such problems the slew rate should be three times the sampling frequency.

5.4.4 Thermal Noise

Thermal noise directly adds to noise floor of the overall system. Consider a typical design of a fully differential switched capacitor integrator. If an ideal input voltage source is available during the sampling phase, when *phil* is closed, then a noise voltage with variance of $2*kT/C$ (kT/C on each of the differential sampling capacitors) is induced. During the integration phase, when the charge is transferred from sampling capacitors to feedback capacitors, another noise voltage with variance of $2*kT/C$ (kT/C on each of the differential feedback capacitors) is induced. The total input referred thermal noise power induced is given by equation (5.11) [43]:

$$S_n = 4 * \frac{kT}{C} \quad (5.11)$$

Where k is the Boltzmann's constant, T is the temperature in Kelvin and C is the sampling capacitor. For practical fully differential designs, the input referred thermal noise should be close to the above ideal value.

5.4.5 Switch on-resistance and Dominant Closed Loop Pole of OTA

In practice, the switches in the switched capacitor integrator are realized with NMOS or/and PMOS transistors which have some non-zero resistance during the ON-period. In ideal case, switch on-resistance is zero, but when we have non-zero switch resistance the RC time constant increases and affects the gain and pole errors in a switched capacitor integrator. The parasitic capacitance of the switches will contribute to the load capacitance and degrade the settling time of the OTA. This switch on-resistance, especially during the integration phase, plays a vital role because the settling time requirements are stringent. The switch on-resistance degrades the dominant closed loop pole and further limits the speed of the settling time process, thereby introducing more

gain and pole errors in the circuit. Equation (5.12) specifies modeling of the settling error [44]:

$$\delta = e^{\left(-p_{cl} \cdot \frac{t_2}{p_2}\right)} \quad (5.12)$$

Where, p_{cl} = closed loop pole = gm / C_{eq} ,

t_2 = time during integration phase,

p_2 = closed loop pole error.

The switch on-resistance R varies with the input voltage and causes harmonic distortion.

In [48] the relation between the total harmonic distortion (THD) and the switch on-resistance is mentioned in equation (5.13).

$$THD = \frac{e^{[-4R \cdot C_s \cdot f_s] - 1}}{\left(1 - e^{[-4R \cdot C_s \cdot f_s] - 1}\right)} \quad (5.13)$$

Where, C_s is the sampling capacitor and f_s is the sampling frequency.

The effective gain-bandwidth (GBW) of the integrator during integration is given [48] in equation (5.14).

$$GBW = \frac{GBW}{\left(1 + (2\pi \cdot GBW \cdot 2R \cdot C_s)\right)} \quad (5.14)$$

The gain-bandwidth of the integrator should not be degraded or smaller than twice the gain-bandwidth of the OTA.

5.4.6 OTA Capacitive Loading

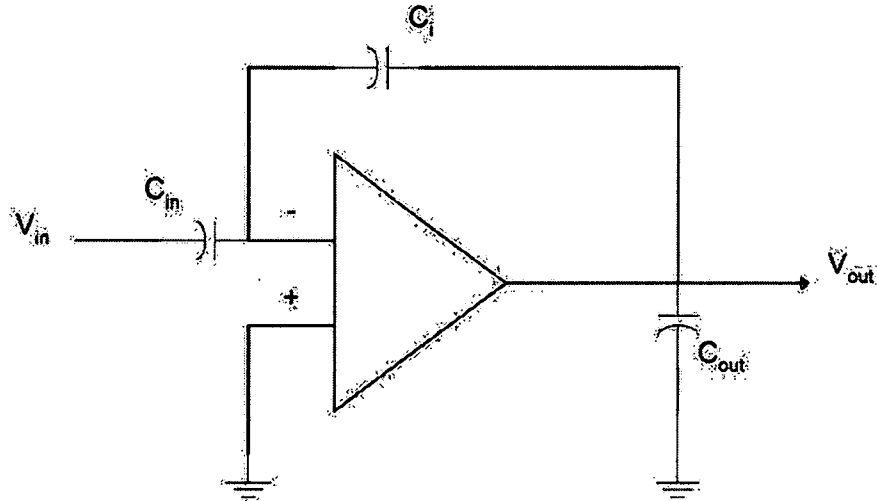


Figure 5.7 OTA capacitive loading.

Figure 5.7 shows a typical loading situation of OTA in switched capacitor integrators [53]. The total input capacitance C_{in} consists of sampling capacitance C_s , DAC feedback capacitance C_{dac} , and the OTA input parasitic capacitance. The total output capacitance C_{out} consists of the feedback capacitor, OTA output parasitic capacitance, and the load capacitance of the following stage (integrator or an ADC). For a folded cascode OTA, the unity gain bandwidth is given by equation (5.13)

$$\omega_b = g_m / C_{eq1} \quad (5.13)$$

Where g_m is transconductance of the input transistors, C_{eq1} = effective load capacitance and C_i is the integrating capacitor. The -3 dB frequency of the OTA depends upon the unity gain bandwidth and the feedback factor β . The feedback factor is given by equation (5.14):

$$\beta = \frac{C_i}{C_i + C_{in}} \quad (5.14)$$

The load capacitance is given by equation (5.15):

$$C_1 = C_{out} + \frac{(C_i C_{in})}{(C_i + C_{in})} \quad (5.15)$$

The unity gain bandwidth can be expressed as in equation (5.16):

$$w_b = \beta * \frac{g_m}{C_1} = \frac{g_m}{C_{eq1}} \quad (5.16)$$

We obtain the equivalent capacitive load of the OTA in feedback configuration as in equation (5.17) [44]:

$$C_{eq1} = C_{in} + C_{out} + \frac{(C_{in} C_{out})}{(C_i)} \quad (5.17)$$

Thus the settling time constant can now be stated as in equation (5.18):

$$t = \frac{C_{eq1}}{g_m} \quad (5.18)$$

5.5 Design of the Folded Cascode OTA

As stated earlier, the folded cascode OTA was selected to be the amplifier topology suitable for our application because of its modest gain, high output swing, high dynamic range, high speed, and comparatively less power consumption. The folded cascode OTA is designed in 0.18 μ m technology with a 2.5 V power supply. The transistor sizes of the OTA are specified in Table 5.1. Table 5.2 provides gain, slew rate and unity gain bandwidth in open loop configuration, settling time, offset, current consumption, -3 dB frequency, differential output swing, and phase margin results of the OTA which satisfy the requirements for our application. The simulation results for the parameters mentioned

in Table 5.2 for 150fF load are presented in Appendix F.1. Appendix F.2 includes the design of wide swing current mirror used for biasing the folded cascade OTA. The size of the transistors used for designing wide swing current mirror circuit is placed next to each transistor. The extracted results for the implemented op-amp are presented in Table 5.3 for 750fF load.

Table 5.3 Transistor sizes of designed folded cascode OTA.

Transistors	W/L in μm
<i>M1</i>	16/0.18
<i>M2</i>	16/0.18
<i>M3</i>	33/0.18
<i>M4</i>	73/0.35
<i>M5</i>	73/0.35
<i>M6</i>	17/0.35
<i>M7</i>	17/0.35
<i>M8</i>	49/0.35
<i>M9</i>	49/0.35
<i>M10</i>	37/0.35
<i>M11</i>	37/0.35

Table 5.2 Results of the designed folded cascode OTA.

Results	Folded cascode OTA
DC gain	58 dB
Slew rate	486 V/ μ s
Bias current I_{ss}	246 μ A
Unity gain BW	1 GHz
Differential o/p swing	3.18 V p-p
Phase Margin	60 degrees
-3 dB frequency	1.5 MHz
Input offset voltage	0.293 μ V
Settling time (0.1%)	6 ns
Power Consumption	1.875mW

Table 5.3 Results of the implemented folded cascode operational amplifier.

Results	Folded cascode OTA
DC gain	54 dB
Slew rate	268 V/ μ s
Bias current I_{ss}	1.1mA
Unity gain BW	440 MHz
Differential o/p swing	6 V p-p
Phase Margin	51 degrees
-3 dB frequency	1.27 MHz
Input offset voltage	9.876 μ V
Settling time (0.1%)	9.05 ns
Power Consumption	15.975mW

5.6 Fully Differential Comparators

Fully differential comparators are used in high resolution applications because they reduce offset due to clock feed-through and charge injection. The fully differential scheme not only reduces the clock feed-through but also eliminates the common mode signals like power supply noise and flicker noise [49]. The charge injection errors are unwanted charges injected into the circuit due to the turning off of transistors. Consider the arrangement of the fully differential comparator in switched capacitor integrator in Figure 5.8.

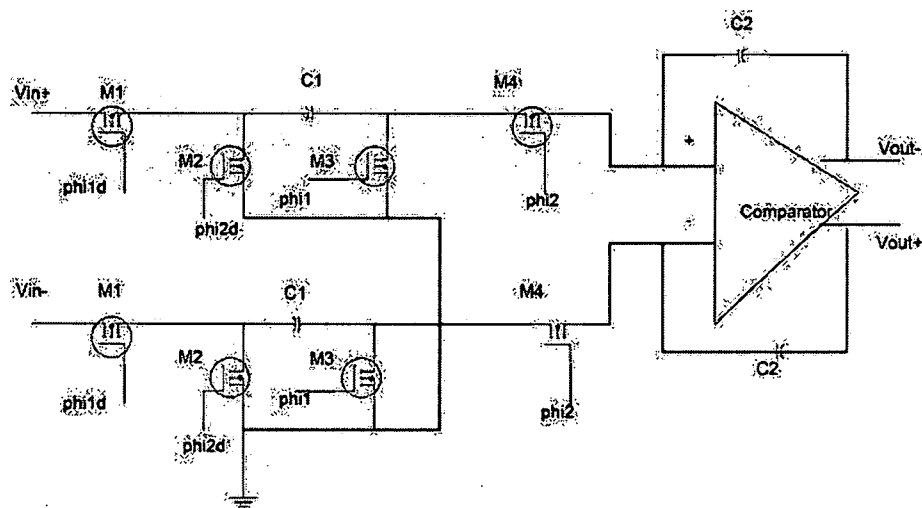


Figure 5.8 Fully differential comparator in switched capacitor integrator.

The switches are constructed using transistors $M1$ and $M2$ are the signal conducting transistors, which should be turned off slightly later ($\phi 1d$ and $\phi 2d$) than the summing junction transistors $M3$ and $M4$ ($\phi 1$ and $\phi 2$). This is done to avoid temporary glitches produced due to charge injection errors when $M3$ and $M4$ are turned at the same time or slightly after $M1$ and $M2$. After the summing junction switches have been turned off, the right hand side of the capacitor does not conduct signal to the comparator, resulting only in a dc offset of the signal, which can be removed by fully differential scheme. More importantly, the charge injection produced by $M3$ and $M4$ is signal independent and does not cause any harmonic distortion. The charge injection caused due to transistors $M1$ and $M2$ does not affect signal transmission or the charge stored on the capacitor $C1$ because the right side of the capacitor is open circuited. When $M1$ and $M2$ turn on, the input signal will settle regardless of previous charge injection.

5.6.1 Regenerative Latch Comparators

The regenerative latch comparator is insensitive to hysteresis and the dc offset since it is attenuated by the gain of the previous stages [27]. The noise is highly attenuated due to the second order noise shaping employed before the comparator. Figure 5.9 shows the regenerative latched comparator as described by [54].

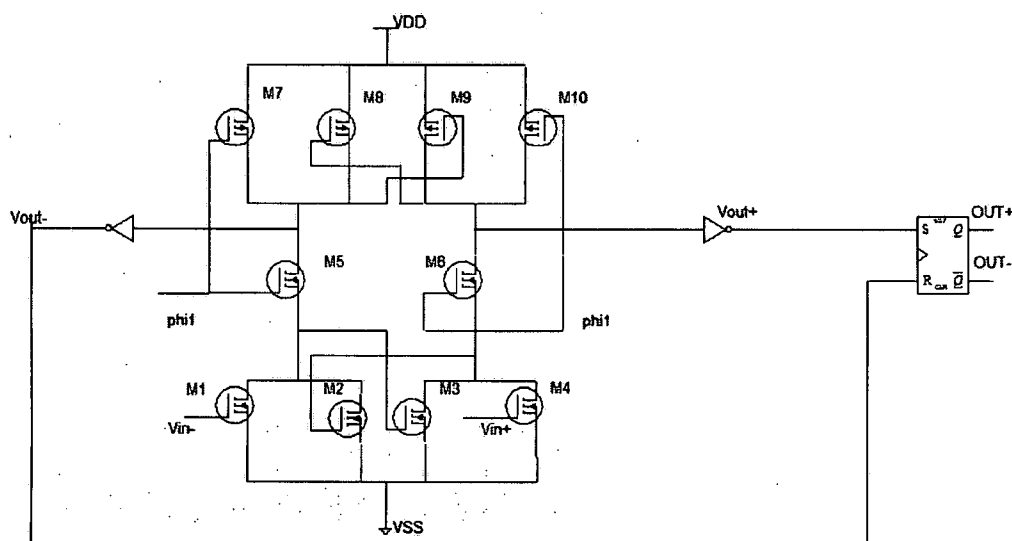


Figure 5.9 Regenerative latch comparator.

The regenerative positive feedback latch is pulled up to V_{DD} during the latch phase when ϕ_{l1} goes low. The positive feed-back latch is evaluated at the beginning of the sampling phase where ϕ_{l1} goes high and the differential inputs are compared. The regenerative comparator is reset after the sampling phase or after the comparison is done for the next set of input values for comparison. This is done in order to eliminate memory effects or hysteresis in which charge can be stored from one decision cycle to other. During track phase, comparison is performed and the positive feedback along with the S - R latch drives the analog output into full digital output. Generally for moderate to high gains a

preamplifier is used, but if high speed is needed, the preamplifier can be replaced by a unity gain buffer. High gain and thus longer time constants can reduce the speed during the tracking or sampling phase. The latch mode time constant is given by equation (5.19) [55].

$$\tau_{latch} = \frac{(k_1)}{(k_2)} \left(\frac{L_2}{u_n V_{eff}} \right) \quad (5.19)$$

Where, k_1, k_2 are constants, $k_1/k_2 = 2$,

u_n = mobility of the transistor,

V_{eff} = the overdrive voltage,

L_2 = length of the transistors.

This time determines the maximum clock frequency of the comparator. If very high resolution is required that is very small input voltage difference needs to be resolved then the latch mode time constant needs to be increased, otherwise meta-stability may occur due to undecided outputs. The inverters have a low switching threshold, because if the decision cannot be made before *phil* goes low then the *S-R* latch can hold the previous output sample rather than making an improper decision [27]. The input transistors and cross-coupled transistors are designed with minimum length to obtain high speed and prevent hysteresis.

5.6.2 Non-idealities in Comparators

This section explains some of the non-idealities present in comparators. These non-idealities are not as detrimental to the performance of the data converters as are the non-idealities of the OTA because they are highly attenuated by the preceding stages. The non-idealities such as offset and hysteresis are described below.

1. Comparator Offset

Due to component mismatch, the threshold voltage at which the comparator toggles or makes a decision is slightly altered. The amount of voltage by which the threshold voltage is altered is called offset voltage. The offset can be reduced by using the auto zeroing technique in comparators. But this complicates the design. Moreover, the offset will be greatly reduced by the gain of the preceding stages. The comparator is preceded by at least one integrator, whose gain is typically large. The offset does not play a critical role in determining the SNR of the system. The offset of the designed regenerative latch comparator is 20 mV.

2. Hysteresis

The inability of the comparator to make proper decision after track or comparison stage is termed as hysteresis. To eliminate hysteresis, we need to reset the comparator completely before it makes decision for the next input sample. If the comparator is not reset completely, the comparator retains memory from the previous state and hysteresis results causing the comparator to make an incorrect decision. To prevent hysteresis from occurring, minimum length transistors should be used for faster resetting of the comparators.

5.7 Integrators

Integrators may be either discrete-time or continuous-time. In continuous time integrator (CT), the signal is sampled at the input of the quantizer after the loop filter, while in the discrete time integrator (DT) architecture the signal is sampled at the input of the modulator. There are many tradeoffs between discrete time and continuous time integrators which makes it difficult to choose one over the other. DT loop filters are

implemented using the switched capacitor (SC) technique, thus employing very precise coefficients (capacitor ratios). CT loop filters are implemented by charging the capacitance with a resistor or a constant current source for a precise period of time. Thus CT systems depend upon accurate pulse shaping and are very sensitive to clock jitter since they need precise period of time for their operation. Since in usual CT implementations the duration of the current pulses is defined by the clock signal, the clock jitter produces a small random variation in the charge transferred during a clock period. In CT systems, the digital output has to be converted to continuous domain which imposes additional constraints on the CT systems and causes errors. Since these errors take place at the modulator input node, which is the most sensitive node, this is one of the reasons for preferring the DT architecture over their CT counterpart [62]. The CT architectures are sensitive to gain errors because their gain is dependent on values of R and C , which are sensitive to process and temperature variations. The gain of switched capacitor (SC) integrators is a ratio of the integrating and summing capacitors. The harmonic distortion of continuous time systems depend on linearity of the resistor values, which is generally poor. CT systems have stringent requirements like accurate RC time constants, sensitivity to clock jitter and noise, high op-amp linearity, which makes the design challenging for high resolution applications. The other most significant reason for choosing a DT loop filter is its compatibility with CMOS technology. DT integrators can be easily realized in a low cost, high density, low power CMOS technology [27].

5.7.1 Switched Capacitor Integrators

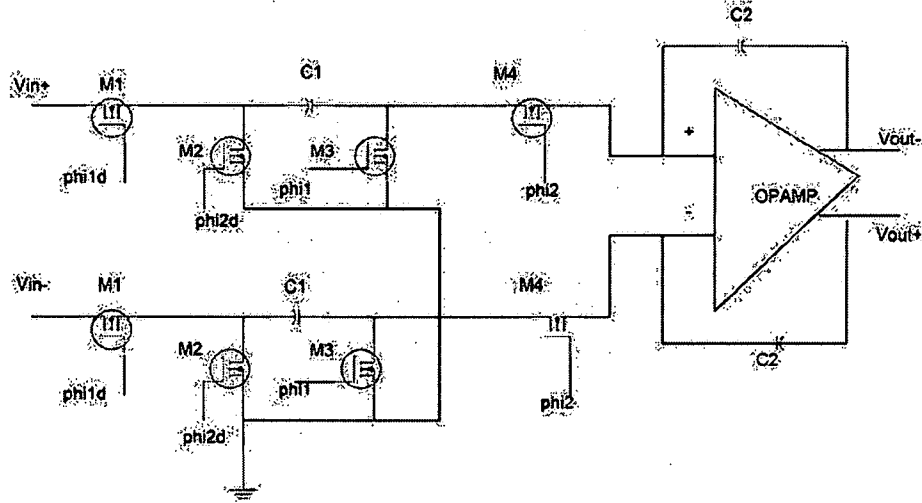


Figure 5.10 Switched capacitor integrator.

Figure 5.10 shows the circuit for a fully differential delaying switched capacitor integrator. The switches $M1$ and $M2$ are delayed and switches $M3$ and $M4$ are advanced to eliminate the non-idealities due to charge injection and capacitive feed-through. If $(n-1)t$ to $(n-1/2)t$ is duration of phase ϕ_{i1} and $(n-1/2)t$ to nt is duration of phase ϕ_{i2} , then the transfer function of the SC integrator is given as follows:

During phase ϕ_{i1} the voltage across each capacitor is expressed as in equation (5.20.1) and (5.20.2) [50]:

$$V_{C1}(n-1)t = V_{in}(n-1)t \quad (5.20.1)$$

$$V_{C2}(n-1)t = V_{out}(n-1)t \quad (5.20.2)$$

Where V_{C1} = voltage across capacitor $C1$ during ϕ_{i1} ,

V_{C2} = voltage across capacitor $C2$ during ϕ_{i1} ,

V_{in} = input voltage and V_{out} = output voltage.

During phase ϕ_{i2} , the output is given by equation (5.21)

$$V_{out}(n-\frac{1}{2})t = \frac{C1}{C2} V_{in}(n-1)t + V_{out}(n-1)t \quad (5.21)$$

If the period is advanced from $(n)t$ to $(n+1/2)t$; then there is no change in the output voltage and this is expressed in equation (5.22).

$$V_{out}(n)t = V_{out}(n-\frac{1}{2})t \quad (5.22)$$

Combining the above equations we get the following equations

$$V_{out}(n)t = \frac{C1}{C2} V_{in}(n-1)t + V_{out}(n-1)t \quad (5.23)$$

$$V_{out}(z) = \frac{C1}{C2} z^{-1} (V_{in}(z)) + z^{-1} V_{out}(z) \quad (5.24)$$

$$\frac{V_{out}(z)}{V_{in}(z)} = \frac{C1}{C2} * \frac{1}{(z-1)} \quad (5.25)$$

The switched capacitor response for small input amplitude of 0.2 V (p-p) is shown in Appendix F.4 for input frequency $f = 1$ MHz, sampling frequency $f_s = 80$ MHz should ideally have a magnitude gain of 12.73. But due to non-ideality and limited output swing, the gain reduces to 10. The magnitude response of the integrator is given in equation

$$|H(f)| = \frac{1}{\sqrt{2(1 - \cos(2\pi \frac{f}{f_s}))}} \quad (5.26)$$

$$\angle H(f) = -\frac{\pi}{2} + \pi \frac{f}{f_s}; 0 < f < f_s$$

(5.26) in [39].

$$H(f) = \frac{1}{\sqrt{2(1 - \cos(2\pi \frac{f}{f_s}))}} \quad (5.26)$$

5.8 Non idealities in Switched Capacitor Integrator

The non-idealities in switched capacitor integrator have been discussed next. Detailed information about these non-idealities can found in [27].

5.8.1 Settling Time

Settling time is an important characteristic of a switched capacitor network. An output signal in response to the input should settle approximately within half the clock period. There are two factors that determine the settling time: 1. The RC time constant of the switches and the switched capacitor, and 2. the response time of the operational amplifier. If the settling time is signal independent then it is termed as linear settling time and if it is signal dependent it is called as non-linear settling time. If linear settling time is not satisfied it results in a gain error and if nonlinear settling time is not satisfied it causes distortion, which is detrimental to the entire system as it degrades the performance of the modulator.

5.8.2 Gain Errors

There are a number of different causes for gain error. Capacitor mismatch is a direct source of gain error, since the gain of the switched capacitor integrator is the ratio of sampling capacitor to the integration capacitor. Another cause of gain error is finite op-amp gain, incomplete settling due MOS switch resistance, and finite op-amp bandwidth. Gain error causes the noise to leak from one stage of cascaded modulator to the other stage and the overall noise shaping of the modulator will be the noise shaping of the first

stage modulator. The transfer function of the integrator with finite gain is given by equation (5.27) in [27].

$$H(z) = \frac{1}{(1 - (1 - A_{dc}^{-1})z^{-1})} \quad (5.27)$$

Where, A_{dc} is the finite gain of the op-amp.

5.8.3 Pole Errors

Integrator pole error is caused by finite op-amp gain. In cascaded modulators, pole error causes the leakage of noise and the overall noise is shaped to the order of the first modulator in cascade. The linearity, finite dc gain, settling time, and finite bandwidth of the first op-amp should be satisfied in order to get maximum performance out of the system because noise is subsequently shaped by this op-amp before entering the next stage and hence the conditions on the remaining op-amps become less stringent.

5.8.4 Thermal Noise

Spectral density due to the thermal noise of the switches is inversely proportional to the switched input capacitance. The sampling frequency f_s is present because the thermal noise is aliased down to the band from 0 to $f_s/2$. The kT/C factor is multiplied by four because; two capacitors are present during each clock phase, and four capacitors in a single clock period. It is given by equation (5.28):

$$S_n = 4 * \frac{kT}{f_s C} \quad (5.28)$$

Where k is the Boltzmann's constant, T is the temperature in Kelvin and C is the sampling capacitor.

5.9 Analog-to-digital and digital-to-analog converter (ADC/DAC)

The various types of ADCs and DACs can be found in Appendix A. The 3-bit ADC/DAC has been realized using a fully differential scheme. The differential output of the second integrator is compared with seven differential reference voltages in a 3-bit differential flash ADC. A flash ADC design is chosen over the other types of ADCs for its speed and its ability to convert the analog input to digital output in a single clock cycle. In a differential flash ADC shown in Figure 5.11, the comparison is done as follows:

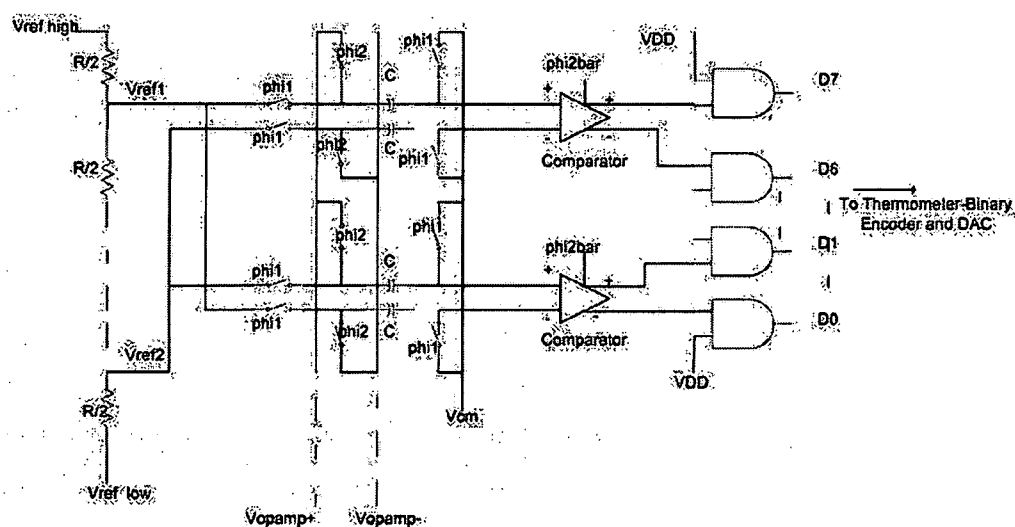


Figure 5.11 Flash analog-to-digital converter.

During phase *phi1*, unique differential reference voltages are sampled on to the left side of the capacitors, while the right side of the capacitors are tied to analog ground, which is typically the input common mode voltage. During phase *phi2*, the differential output voltage of the integrators is sampled on to the left side of the capacitors. The right side of

The DAC uses a combination of transmission gate switches to convert the differential digital outputs to differential analog output. The differential analog output is fed-back to the negative input of the modulator.

5.9.1 Multi-bit ADC and DAC Non-idealities

The multi-bit ADC, in this case, flash ADC has differential and integral non-linearity; in addition, to offset and gain errors. These non-idealities are discussed in detail in Appendix B. A single-bit DAC has just two threshold levels and is inherently linear. The multi-bit DAC, on the other hand, has more than two levels; and hence is susceptible to non-linearity. The non-linearity of DAC in the feedback path is the most defining phenomenon on determining the SNR of the modulator because the DAC is connected directly to the input of the modulator. The linearity of the DAC should be at least within 0.5 LSB to provide desired resolution of the entire modulator. To avoid errors due to non-linearity, the DAC is realized using resistor array architecture with identical resistor values to generate monotonic differential reference voltages. The maximum and minimum DNL values for the designed resistor array DAC architecture are 0.25 LSB and -0.28 LSB, respectively for 256-point histogram. The maximum and minimum INL values for the designed resistor array DAC architecture are 0.11 LSB and -0.09 LSB, respectively for 256-point histogram. The DNL and INL plots for the 3bit DAC are given in Appendix F.3.

5.10 Novel *NMOS-PMOS* Thermometer-to-binary Encoder

The novel design of a *NMOS-PMOS* thermometer-to-binary encoder is shown in Figure 5.13 [65]. We use a row of AND gates to locate the leading one and generate a one-hot bit output. We pass the 8-bit one-hot output to an array which generates the correct 3-bit binary output that corresponds to the position of the one-hot bit which is equal to the leading one in the thermometer code. The array can be designed with transmission gates to pass zeros and ones to the output, but using the transmission gates will increase the bit line capacitance of b_0 , b_1 , and b_2 lines. To reduce each bit line capacitance by about 50 %, we use *NMOS* to pass a strong zero and a *PMOS* to pass a strong one to the output. The *NMOS-PMOS* array is structured based on a binary truth table, where an *NMOS* is used when a "0" is the input and a *PMOS* is used when a "1" is the input. The worst case delay of the *NMOS-PMOS* array is only one *MOS* transistor for any N -bit array. As a result, this novel encoder can be extended to higher bits high-speed and low-power thermometer-to-binary encoders.

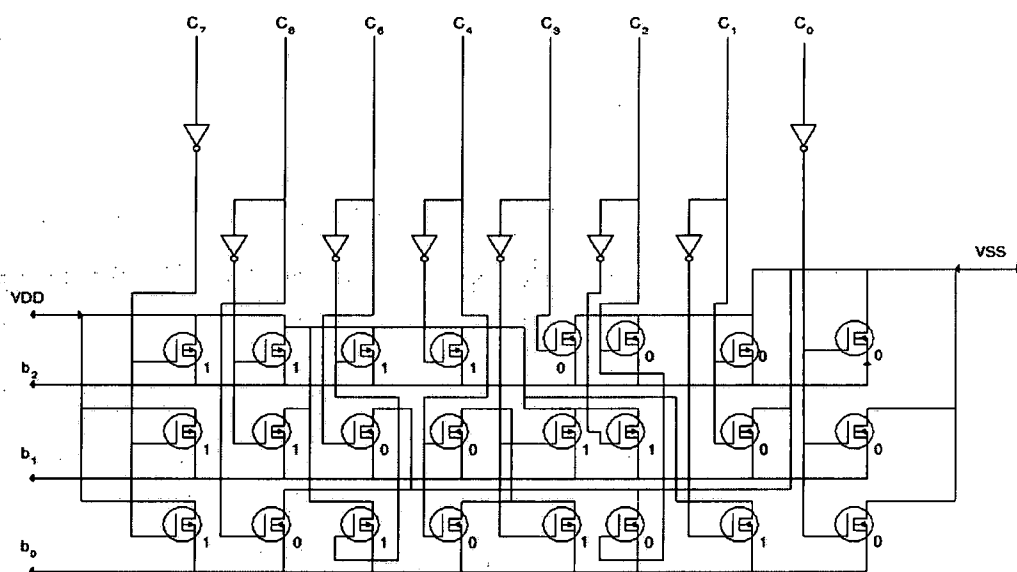


Figure 5.13 A novel *NMOS-PMOS* thermometer-to-binary converter.

6 VLSI CIRCUIT IMPLEMENTATION

In the previous chapter, various circuits used in the design of the delta sigma modulator were discussed. This chapter concentrates on the implementation issues related to some of these circuit elements. The VLSI implementations of these designed circuits focus not only on maintaining a low power and a compact design but also on improving the performance of the circuits. We provide discussion regarding to the selection we made to implement the proposed ADC.

6.1 Differential 1-Bit DAC

A DAC is used in the feedback path of the delta sigma modulator to convert the digital output back to the analog form to be subtracted from the analog input signal of the modulator. The overall resolution of the ADC is determined by the feedback accuracy of the DAC. To increase the resolution of an ADC, multi-bit DAC can be used instead of a 1-bit DAC; however, the linearity of the multi-bit DAC must match the overall linearity of the system. A 12-bit ADC would require the DAC to have matching requirements between any two steps as stringent as that for a 12-bit DAC. This imposes strict demands on the DAC and its implementation is not possible without the use of techniques such as dynamic element matching, calibration, and trimming. Even though it has low resolution, a single-bit DAC is preferred in the first stage of the cascaded modulator over the multi-

bit DAC because of its inherent linearity. As the output of the DAC is a product of the digital input and the reference voltage, the implementation of the reference voltage is critical in producing a noise-free and linear output. The reference voltage signal should be devoid of any high frequency spectral component. The non-idealities in a feedback DAC are further complicated when inappropriate charge is taken from the reference voltage and delivered to the integrator. In switched capacitor delta sigma modulators, the non-idealities in delivering charge to the integrator not only depend on the reference voltage but also on the comparator's input voltage as explained by [56]. If the amount of charge and the instant at which it is taken from the reference is different for each clock cycle, then the reference voltage is sampled at a different potential at each instant resulting in unwanted signals on the reference. If the amount of charge delivered depends on the comparator's input voltage, then reference voltage is subjected to signal dependency, which will create signal distortion. In order to circumvent these problems imposed by reference voltage and comparator, a commercially implemented differential 1-bit DAC is presented [27].

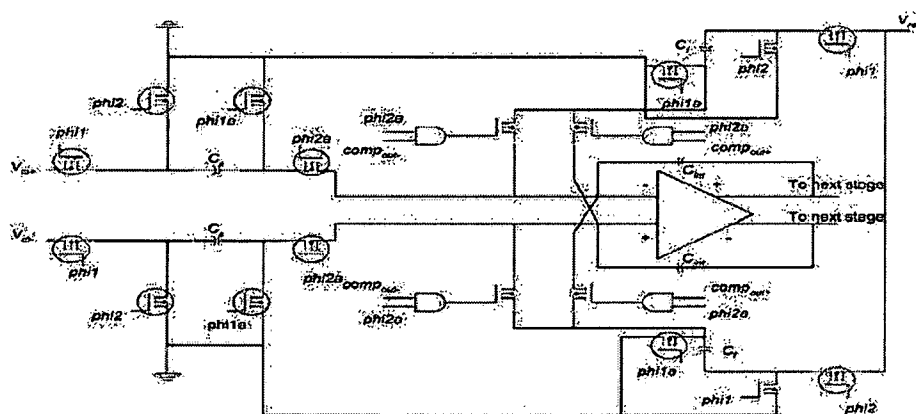


Figure 6.1 Commercially implemented fully differential 1-bit DAC with single polarity reference voltage[27].

Figure 6.1 shows a fully differential 1-bit DAC with a single reference voltage V_{ref} . C_f represents the feedback capacitor, C_{int} represents the integrating capacitor and C_s is the sampling capacitor. The outputs from the comparator is feedback to the input of the AND gates, whose other input is the advanced clock phase ϕ_{2a} . The two non-overlapping clock phases ϕ_{1a} and ϕ_{2a} , which are advanced versions of their respective clock phases are used to eliminate charge injection. During phase ϕ_{1a} , the upper feedback capacitor is charged to the reference voltage and the lower feedback capacitor discharges to analog ground. During ϕ_{2a} , based on the decision of the comparator, the capacitors are charged with either positive charge $C_f V_{ref}$ or with negative charge $-C_f V_{ref}$. If the comparator output is high, the non-inverting and inverting terminals of the operational amplifier receive charge opposite to the charge across the sampling capacitor. If the comparator output is low, then the same polarity of charge is delivered across the sampling and the feedback capacitors. The commercially implemented differential 1-bit DAC ensures that the capacitors are charged between the reference and analog ground every clock cycle. Also since there is no dependency on the comparators input voltage because of the non-overlapping clocks and switched capacitor mechanism, these DACs do not have problems like spurious unwanted signals and harmonic distortion [27].

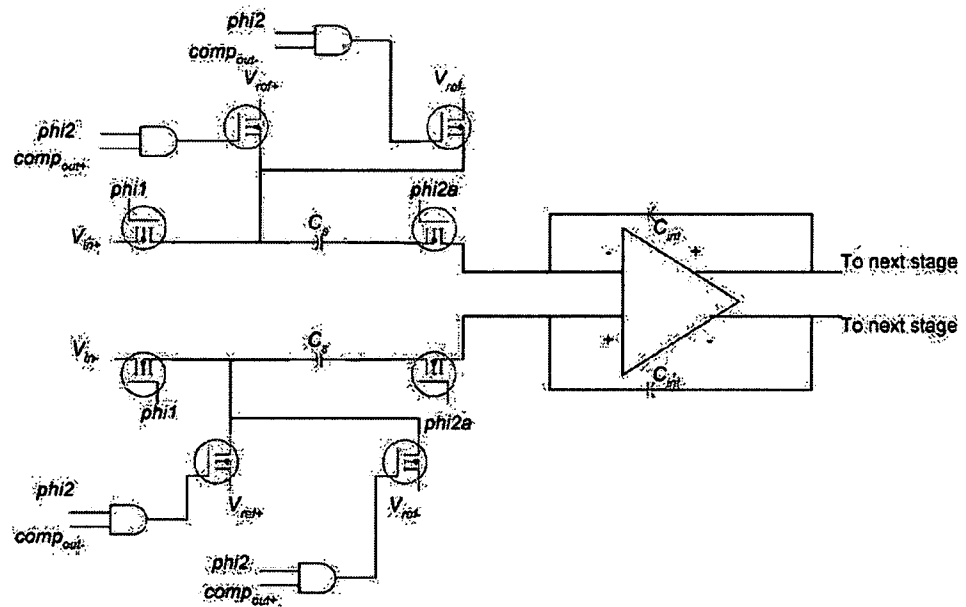


Figure 6.2 Fully differential 1-bit DAC with dual polarity reference voltages.

In the above 1-bit DAC implementation, a single polarity reference voltage was used. Figure 6.2 shows the DAC with dual polarity reference voltages [44]. During phase ϕ_{i1} the input is sampled on the sampling capacitors and during ϕ_{i2} V_{ref+} or V_{ref-} is sampled onto the integrating capacitor based on the comparator's decision. The two non-overlapping clock phases ϕ_{i1a} and ϕ_{i2a} , which are advanced versions of their respective clock phases are used to eliminate charge injection. The dual polarity reference voltage has smaller capacitive load and faster settling of charge transfer. Since only one capacitor is used by both the reference voltage and the input signal, power consumption is less compared to the single polarity reference voltage. However, dual polarity reference voltage has to provide a charge to the sampling capacitor C_s , which is charged by the input signal during the sampling phase; the charge delivered by the dual polarity reference voltage is signal dependent causing distortion. Signal distortion has

the potential to drastically reduce the SNR of the system. Therefore single polarity reference voltage is chosen over the dual polarity reference voltage to trade power consumption for resolution.

6.2 Fully Differential Implementation

In the fully differential implementation shown in Figure 6.1, there are two signals having the same magnitude but 180° out of phase with each other, and measured with respect to analog ground. The signal information is transferred by the difference of the two signals. In the single-ended implementation there is only one signal, which is measured with respect to analog ground. The fully differential implementation has several advantages over the single-ended implementation as will be discussed next.

In fully differential implementation since the signal is transferred by the difference of the two signals, any common mode disturbance will not affect the differential signal. Thus a fully differential architecture has a better common mode rejection than its single-ended counterparts. Common mode disturbances like substrate noise and power supply noise will not interfere with the operation of differential signals. In the event there is harmonic distortion, the inverted and non-inverted signals will suffer from this distortion symmetrically. As a result the even harmonics will be suppressed and the differential signal will contain only odd harmonics of the signal.

In this dissertation, the delta sigma architecture is realized using a fully differential implementation. The fully differential implementation is particularly useful when combined with the switched capacitor (SC) integrators. The fully differential implementation minimizes the effect of clock feed-through and charge injection in SC

circuits. The fully differential implementation has two single ended circuits to process the inverted and the non-inverted signals separately. Thus one might think that a fully differential architecture has double the area and power compared to a single ended architecture. This assumption is misleading, and is explained as follows.

Thermal noise power or variance across each capacitor is given by kT/C . So for a single ended implementation, kT/C noise power is sampled twice across the sampling capacitors for charging and discharging clock cycles inducing a total of $2*kT/C$ noise power. For a fully differential implementation kT/C noise power is sampled twice across the two sampling capacitors, since two single ended implementations one each for inverted and the non-inverted signals are used. Thus a total of $4*kT/C$ noise power is generated in a fully differential implementation. This reveals that for the same size of capacitors, noise power is increased by 3 dB in fully differential realization over their single-ended counterparts. However, the signal in the fully differential implementation is increased four times over the single-ended implementation thereby increasing the signal power by 6 dB. Thus there is a 3 dB net increase in SNR for fully differential implementations. In order to achieve the same SNR, capacitors in a fully differential implementation can be halved. The other advantage of the switched-capacitor-fully-differential integrator is that there is no need for two single-ended output op-amps. This is because the single-ended output op-amps can be replaced by fully differential op-amps without loss of performance or much increase in power. In fact the fully differential op-amps have improved gain and frequency response since the mirror pole in single-ended output op-amps is removed [44]. However, there is a need for common mode feedback (CMFB) in fully differential op-amps to bias the common mode output at the average

value of the power supply voltages. A dynamic CMFB does not contribute much to the power dissipation. This shows that the increase in area and power consumption in fully differential implementation is mainly due to the doubling of switches. The above discussion suggests that a fully differential implementation is a superior choice than the single-ended one because of its advantages over the single-ended implementation at the expense of some increase in area and power. For the above reasons, we have chosen the fully differential scheme over the single-ended scheme throughout the implementation of the delta-sigma modulator.

6.3 Capacitor Mismatch

The gain coefficients used for scaling the internal swings of the integrators and the noise-shaping coefficients in the delta sigma modulators are implemented by use of proper capacitor ratios. Since the capacitors are implemented by placing a dielectric between poly and poly-2 diffusions, they are susceptible to random variations during fabrication. The deviation in capacitors will either increase or decrease the actual value of the gain coefficients and the noise shaping coefficients. It is interesting to know what impact this deviation has on the overall SNR of the modulator. From [44], we can conclude that up to 5 % deviation in the capacitor values can be tolerated without a significant degradation in the SNR. As the capacitance value gets smaller the vulnerability to imperfections during the fabrication process increases so it is critical to know the smallest value of capacitance that can be allowed by the fabrication process without any performance degradation. An empirical formula to find the minimum sampling capacitance is available in [43].

$$C_{s\min} = C_A \cdot \frac{A^2}{\sigma^2 \left(\frac{\Delta C}{C} \right)} \quad (6.1)$$

where C_A = capacitance density for a given technology

$$\sigma \frac{\Delta C}{C} = \text{capacitance mismatch ratio}$$

A = technology dependent parameter

The minimum capacitance value calculated using the above empirical formula does not take into account second order effects like temperature increase and fringing capacitance. These effects increase the minimum capacitance value to 25fF for a 0.18 μ m technology. This value is termed as a unit capacitance value and in order to avoid problems due to capacitor ratio mismatch, a multiple of this capacitance value is used to form gain coefficients and noise shaping coefficients in our delta sigma modulator design.

6.4 Thermal or kT/C Noise

As discussed in the fully differential implementation of the SC integrators, a thermal noise power of $4 \cdot kT/C$ is sampled onto the sampling capacitor C_s of the first integrator. The noise power sampled onto the sampling capacitors of the succeeding integrators is attenuated due to noise shaping of the preceding integrator. The noise power of the integrators following the first integrator can be neglected. If the input signal is over-sampled then the noise power is further reduced by the over-sampling factor M . After neglecting the $1/f$ flicker noise and denoting the op-amp noise power by γ the total noise power sampled onto the sampling capacitor is given by equation (6.2).

$$S_n = 4 \cdot \frac{kT}{MC_s} (1 + \gamma) \quad (6.2)$$

Equation (6.2) can not only be used to calculate the SNR of the modulator but also can be used to find the minimum sampling capacitance needed to satisfy the required SNR. For the op-amp the excess noise power $(1 + \gamma)$ is considered to be 2. For example, if the SNR = 78 dB, the over-sampling factor $M = 32$, k is Boltzmann's constant $= 1.38 \times 10^{-23}$, and T is Temperature in Kelvin $= 300^\circ$ then the minimum sampling capacitor C_{\min} can be found from (6.2) as given in equation (6.3).

$$C_{\min} \geq 65\text{fF} \quad (6.3)$$

Since the unit capacitance for our technology is 25fF, a sampling capacitance of 75fF was chosen for the first integrator. We can use a larger capacitance value to increase the SNR of the converter, but this comes at the expense of extra power consumption. A SNR of 80 dB requires a sampling capacitance of 100fF at the same over-sampling factor of 32.

6.5 Non-overlapping Clocks

In switched capacitor implementation at least two distinct clock phases ϕ_{i1} and ϕ_{i2} are required for the sampling and the integrating operations. In order to eliminate charge injection, the clock phases should be advanced which result in two more clock phases ϕ_{i1a} and ϕ_{i2a} . If transmission gates are used, inversion of the two clock phases is required. This adds two more clock phases $\phi_{i1\bar{a}}$ and $\phi_{i2\bar{a}}$; in addition, to the previous four clock phases. The true and the inverted clock phases generated by using inverter is not advisable, since they are overlapping. When clock phases overlap they can be high or low at the same time resulting in unwanted leakage of charge. This unwanted leakage of charge can disturb the correct operation of the sampling and the integrating phases. To ensure two distinct clock phases, the clocks should be "non-overlapping".

Non-overlapping clocks are obtained using NOR or NAND gates in cross-coupled manner with a delay inserted in the feedback path to obtain non-overlapping between the two outputs of the NOR gate.

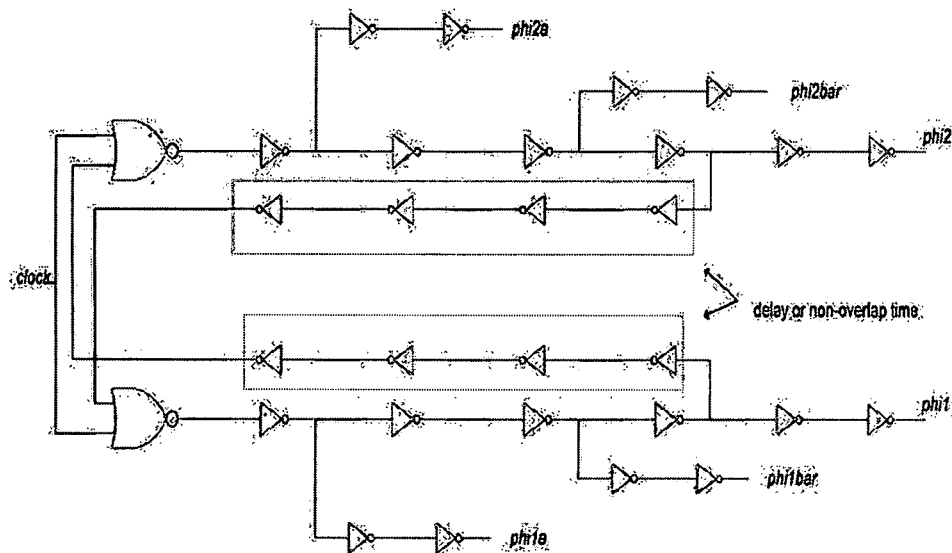


Figure 6.3 Non-overlapping clocks.

Figure 6.3 shows our implementation of the non-overlapping clock scheme and delay balanced using NOR gates in a cross-coupled manner. The delay in feedback path controls the non-overlap time between the two phases. This delay ensures that when output of one of the NOR gates is LOW the output of the other NOR gate becomes HIGH only after the non-overlap time. The non-overlapping clock scheme we developed has four high speed inverters in the delay path to minimize the non-overlapping time and utilize almost 50% duty cycle of the phases. This ensures that non-idealities like finite settling time are satisfied without degradation in performance. The advanced and inverted clock phase can be obtained from the non overlapping clocks. The clock phases

need to be routed throughout the system and should have sufficient driving capabilities. This condition is fulfilled by adding delay matched buffers at the output.

6.6 Determination of the Noise Transfer Function (NTF)

The NTF was determined by the procedure explained in [27]. This methodology is also presented here and is as follows:

1. A modulator order and an NTF filter family between high-pass Butterworth and Chebyshev filter is generally selected. These NTF families have distinct cut-off frequency characteristics determined by the placement of poles and zeros.
2. A suitable filter 3-dB cut-off frequency is selected and the transfer function is scaled so that the first sample of the impulse response is 1. The first loop filter in the delta sigma architecture has a unit delay without which the system is unrealizable [27].
3. Let the noise transfer function be given as

$$\text{NTF} = H(z) = (1 - z^{-1})^n \quad (6.4)$$

where n is the order of the filter, and $h(0) = H(\infty) = 1$,

This requirement imposes the constraint, which is satisfied only if the leading coefficients of the numerator and the denominator polynomials of $H(z)$ are unity.

4. The modulator with this NTF is constructed and simulated to obtain the maximum stable input and peak SNR. If the modulator is unstable then the out-of-band gain of the NTF is reduced. This can be accomplished by lowering the filter cut-off frequency, which reduces the magnitude of the first sample of the impulse response. Because the filter needs to be scaled to make the first sample of the impulse response equal to 1, the resulting cut-off frequency is reduced in comparison with the original cut-off frequency.

As a rule of thumb, a NTF with an out-of-band gain of 1.5 should ensure stability in most designs.

5. If the modulator is stable and the SNR is underachieved then the out-of-band gain of the NTF should be increased until the modulator is on verge of instability. However such aggressive noise shaping can push the modulator in the instability mode; and hence, should be carefully employed. For our second order feed-forward delta sigma delta modulator, the loop filters are given by equation (6.5) in [27].

$$L_0(z) = -L_1(z) = \frac{a_1}{z-1} + \frac{a_2}{(z-1)^2} \quad (6.5)$$

The poles of the loop filter $L_1(z)$ are only present at DC. It can also be said that the NTF has all its zeros at DC. Since Inverse Chebyshev NTFs have the stop-band zeros at non-zero frequencies, this topology cannot be realized. Instead Butterworth high-pass filters are a suitable choice for the implementation of the feed-forward topology. Using the above procedure, the NTF is found in equation (6.6).

$$H(z) = \frac{(z-1)^2}{(z^2 - 1.3281z + 0.5048)} \quad (6.6)$$

The single loop filter $L(z)$ can be found in terms of the desired NTF by

$$L_1(z) = \frac{1-H(z)}{H(z)} \quad (6.7)$$

After substituting (6.6) in (6.7), and using simple partial fractions, we get the coefficients $a_1 = 0.67$, and $a_2 = 0.17$. These are the noise-shaping coefficients of an ideal second order loop filter. In practice, the noise shaping coefficients were selected taking into consideration the derivation of the proposed delta sigma modulator in section 3.7. These gain coefficients need to be implemented using capacitor ratios and every capacitor used

should be a multiple of the unitary capacitor 25fF. Figure 6.4 shows the out of band gain of the NTF, which should be around 1.5 for optimum noise shaping. Figure 6.5 shows pole-zero plot and the stability of the NTF. It can be seen that the second order modulator is stable since its poles are well inside the unit circle. The Matlab algorithm for deriving the noise shaping coefficients is given in Appendix E.

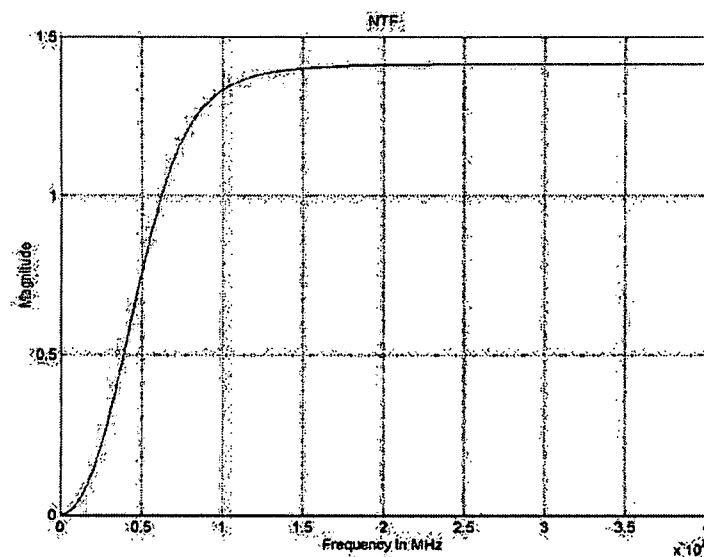


Figure 6.4 NTF of the second order feed-forward modulator.

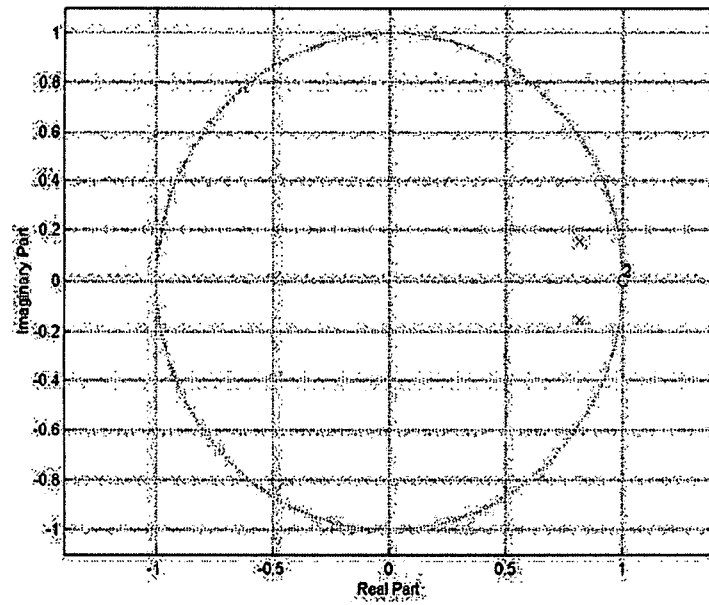


Figure 6.5 Stability of second order feed-forward modulator.

6.7 Implementation of the Feed-forward Summing Junction

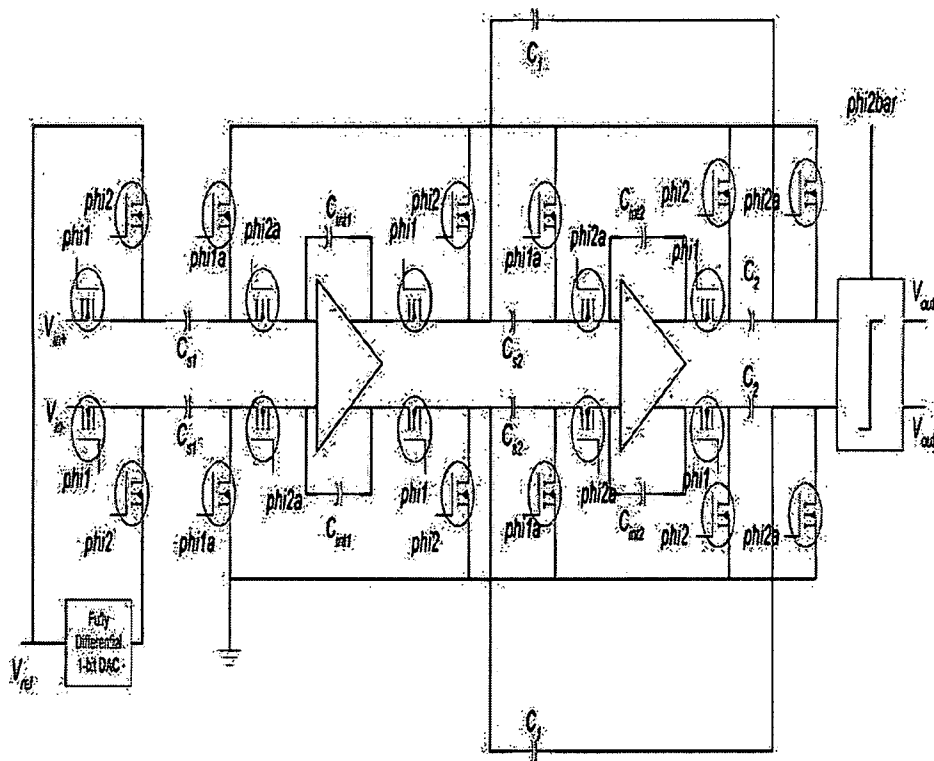


Figure 6.6 Second order feed-forward modulator.

Figure 6.6 shows the feed-forward model of a second order modulator. The noise shaping coefficients determined for the feed-forward modulator from sections 3.7 and 6.6 are implemented using suitable capacitor ratios. When phase ϕ_{i2} is ON, then both the plates of the feed-forward capacitors C_1 , C_2 are connected to analog ground. When phase ϕ_{i1} is ON, then the output of the integrators are connected to the bottom plate of their respective feed-forward capacitors while their top plates are connected to the input of the quantizer. The feed-forward operation is analyzed by noting how the charge is moved across the feed-forward capacitors. The charge movement can be considered for every

feed-forward capacitor acting alone. For example, suppose we want to find the charge developed across feed-forward capacitor C_2 , we need to apply a simple capacitor divider principle. The charge developed across the second feed-forward capacitor is given by the following equations. The total capacitance across the entire feed-forward noise-shaping network is given by

$$C_{total} = C_1 + C_2 \quad (6.8)$$

The charge Q_2 across the second feed-forward capacitor C_2 is given in by

$$Q_2 = Q_{int2} \cdot \frac{C_2}{C_1 + C_2} \quad (6.9)$$

where Q_{int2} is the charge present at the second integrator. Similarly, the charge Q_1 across the first feed-forward capacitor C_1 is given by

$$Q_1 = Q_{int1} \cdot \frac{C_1}{C_1 + C_2} \quad (6.10)$$

As the principle of charge conservation principle demands, we can write the total charge developed across both the capacitors as the sum of the charge stored across each of the feed-forward capacitors C_1, C_2 . As given by [62] this results in equation (6.11)

$$\begin{aligned} C_{total} V_{total} &= Q_1 + Q_2 \\ &= C_1 V_1 + C_2 V_2 \\ V_{total} &= \frac{C_1 V_1 + C_2 V_2}{C_{total}} \\ &= \frac{\sum_{i=1}^2 C_i V_i}{\sum_{i=1}^2 C_i} \end{aligned} \quad (6.11)$$

V_{total} is the total voltage delivered by the summing of voltage across the feed-forward capacitors at the end of phase *phi1*. This voltage represents the input to the quantizer,

which is a comparator in single-bit architecture and a flash ADC in a multi-bit architecture. Since gain coefficients generally used to achieve noise shaping are small, the total voltage V_{total} will be smaller. This will not be a problem for a comparator since it makes its decision based on the polarity of the input. However, the small V_{total} can impose serious constraints on the design of the flash ADC.

7 MODELING OF CASCADED FEED-FORWARD THIRD ORDER DELTA SIGMA MODULATOR

Modeling of the cascaded delta sigma modulator is performed using Simulink. Non-idealities like finite dc gain, finite slew-rate and gain bandwidth, op-amp noise due to switch-on resistance, sampling jitter and thermal noise are introduced step-by-step in the ideal cascaded third order modulator and their effects on the SNR are presented. The result will show that the most critical of the non-idealities are finite slew-rate and gain bandwidth and thermal noise.

7.1 Sampling Jitter

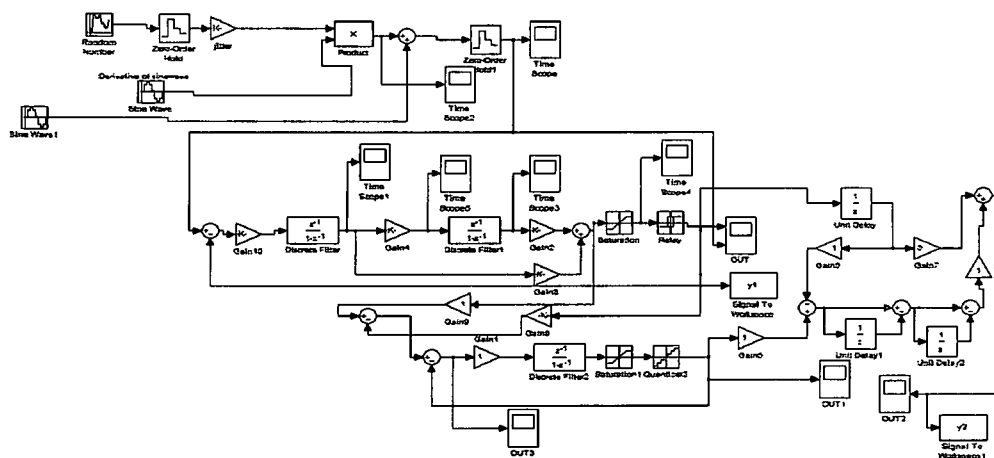


Figure 7.1 Modeling of sampling jitter.

Figure 7.1 shows a Simulink model of the sampling jitter. The sampling jitter non-ideality is represented by Matlab function "jitter" as can be seen in the figure. Sampling

jitter does not have much of an effect on the proposed delta sigma modulator. This sampling jitter occurs due to non-uniformity in sampling time and creates variation in the period of the signal. The variations of the clock period do not have direct effect on the circuit performance (57). The effect of clock jitter is also independent of the order of the modulator. Consider a sine-wave signal with a frequency f_{in} and amplitude A . The uncertainty in sampling or sampling error due to variations in sampling by an amount δ is given by the equation (7.1).

$$x(t) = A \sin(2\pi f_{in} t)$$

$$x(t + \delta) - x(t) = 2\pi f_{in} \delta A (\cos 2\pi f_{in} t) = \delta \frac{d}{dt} x(t) \quad (7.1)$$

Equation (7.1) is modeled using standard Simulink blocks. The sampling uncertainty δ is modeled as random Gaussian noise with zero mean and unity standard deviation. The derivative of the sine-wave signal is derived analytically because of priori knowledge of the signal. The effect of various jitter values on the SNR can be observed in Figure 7.2. It can be seen that for typical jitter values in high resolution delta sigma modulator applications the SNR is hardly affected.

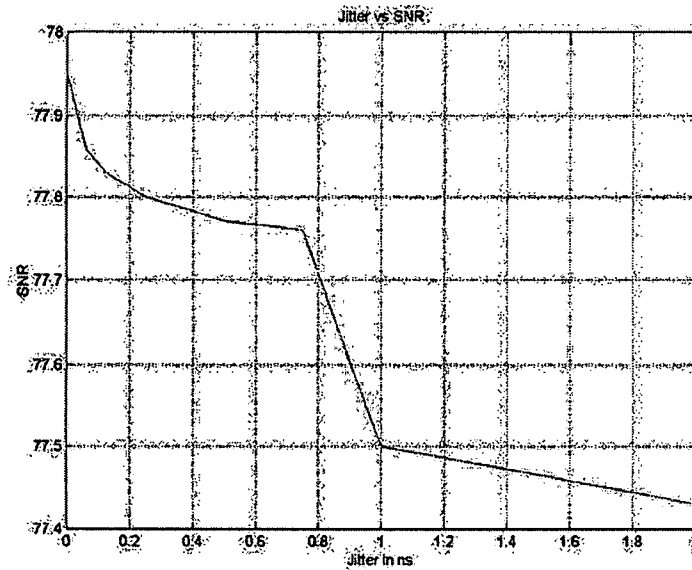


Figure 7.2 Effect of sampling jitter on SNR.

7.2 Thermal kT/C Noise

Thermal kT/C noise is a white noise spectrum and limited by the time constant of the switches and capacitors present in the switched capacitor integrator. Thermal noise can be modeled as a function of Gaussian noise voltage with zero mean and unity standard deviation. The noise variance or power is given by kT/C and its voltage is the square root of kT/C . The input referred noise voltage P_n is given by equation (7.2).

$$P_n = \sqrt{\frac{kT}{C}} \quad (7.2)$$

P_n is modeled using basic Matlab functions and is multiplied by the Gaussian noise voltage. This total noise voltage is added to the input voltage and the noise power is calculated for various capacitance values. The model of thermal noise is presented in

Figure 7.3. In Figure 7.4, the noise power is plotted for various capacitance values and it can be seen that as the capacitance increases the SNR improves.

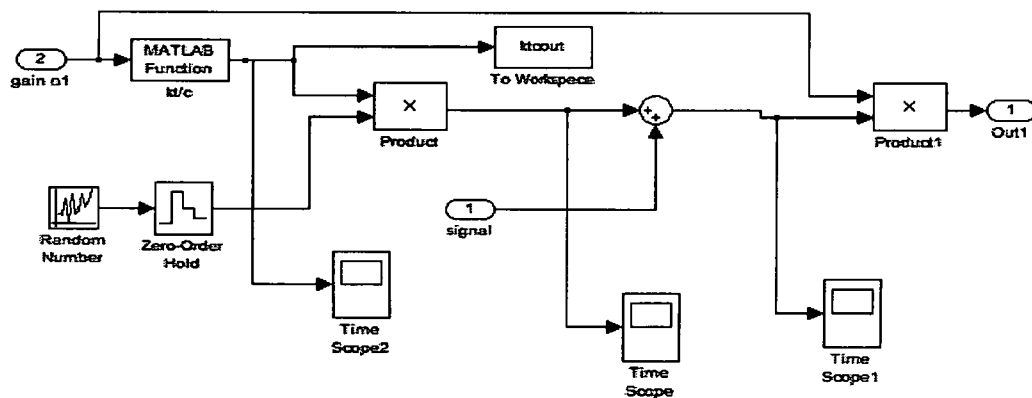


Figure 7.3 Modeling of thermal noise kT/C .

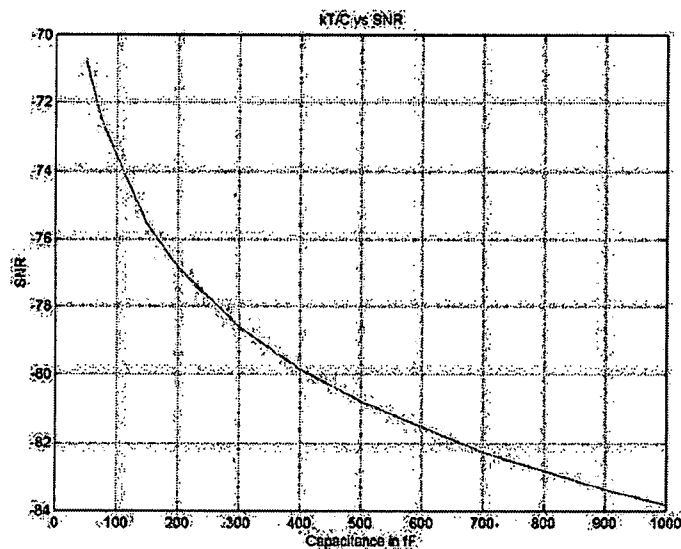


Figure 7.4 Effect of kT/C on noise power.

7.3 Op-amp Noise

Figure 7.5 shows the modulator with noise sources such as kT/C and op-amp noise. V_n is the root mean square (RMS) noise voltage sampled by the operational amplifier on the switched capacitor integrator. This noise voltage generally does not play an important role in reducing noise. The other types of noise sources such as dc offset noise, flicker ($1/f$) noise, shot noise, and gate noise are negligible and are not taken into account [57]. The effect of the total op-amp noise voltage should be verified with actual simulations. The op-amp noise is modeled using the Matlab function “op-amp noise” and can be found in Appendix E.

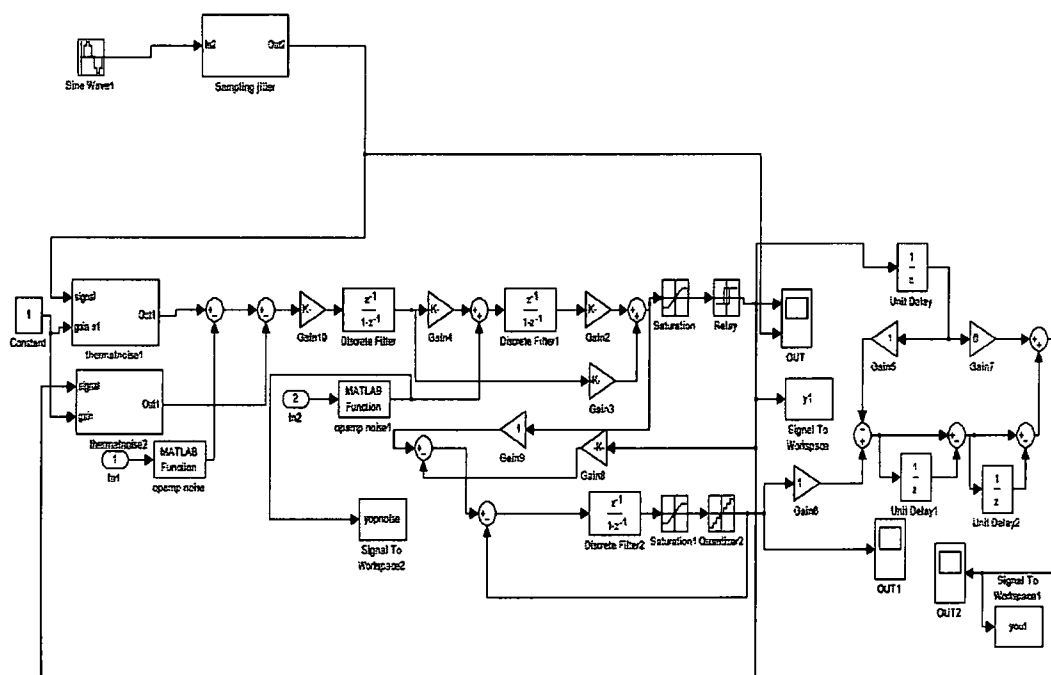


Figure 7.5 Modeling noise sources in ideal modulator.

7.4 Modeling Slew-rate, Finite Gain-bandwidth and Finite DC Gain

The most important consideration for noise analysis and the overall SNR is the modeling of the integrator with non-ideal effects such as finite slew-rate, finite gain band-width and finite gain. These non-idealities generate harmonic distortion and have a profound effect on the signal-to-noise distortion ratio (SNDR). Finite dc gain is modeled by taking into account the input and output parasitic capacitances and the pole, gain errors [58]. The capacitances used in this model are similar to the ones used in simulating the design in Cadence. Such models provide useful insight about the circuit design parameters and can be used to validate some of the approximations. The finite slew-rate and finite gain bandwidth phenomena are realized using actual design parameters to relate the simplified Simulink models to Cadence designs. All these effects are formulated using the Matlab functions in Appendix E. Figure 7.6 shows a complete non-ideal modulator with all the effects acting together. Since slew-rate and bandwidth are inter-related, only the effect of finite slew-rate on SNDR is presented in Figure 7.7, with the bandwidth kept fixed. This is followed by observing the effect of finite dc gain on the base-band noise power in Figure 7.8. These models show that a DC gain of 60 dB, a slew-rate of 200 MHz and gain-bandwidth of 200 MHz would be sufficient to design the proposed cascaded delta sigma modulator.

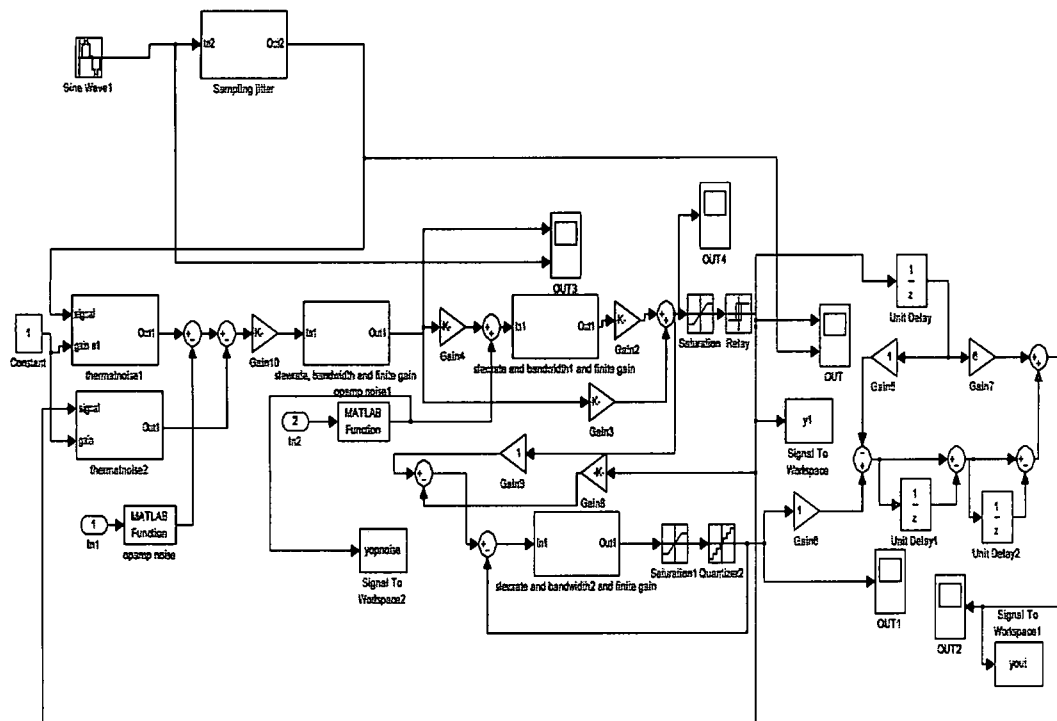


Figure 7.6 Non-ideal cascaded third order feed-forward modulator including finite dc-gain, finite slew-rate and finite gain-bandwidth

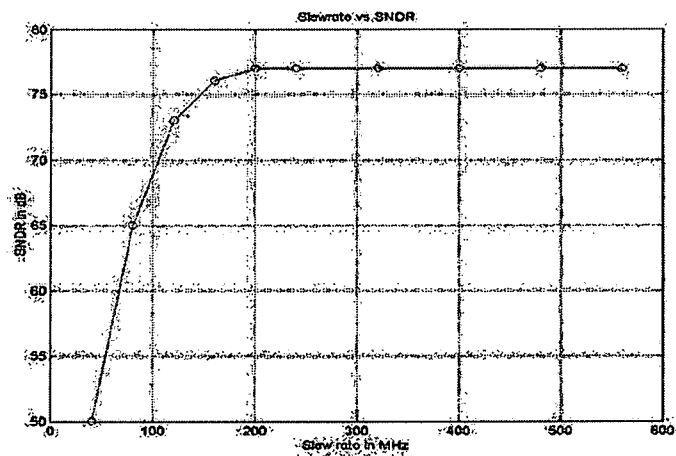


Figure 7.7 Effect of finite slew-rate on SNDR.

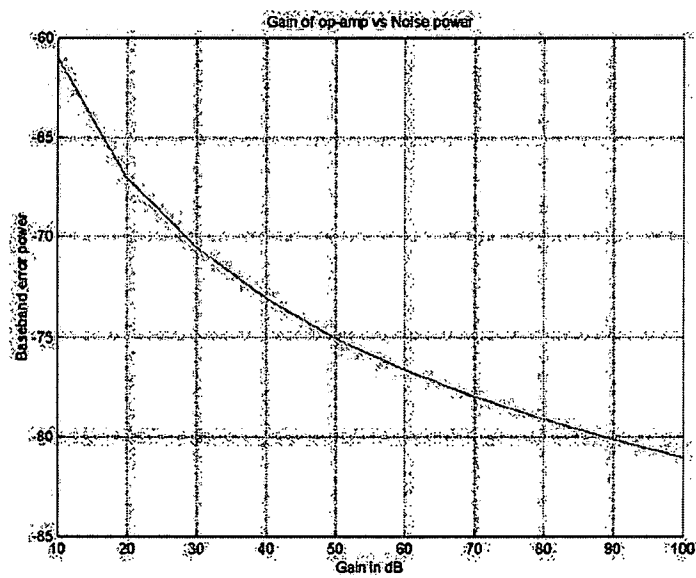


Figure 7.8 Effect of finite DC gain on the noise power.

8 RESULTS

In this chapter, the simulation results and the results obtained by extracting the chip layout of the delta sigma modulator are discussed. A short discussion about quantization noise is provided. The performance of the designed modulator and the physical layout of the cascaded third order delta sigma modulator are summarized. Some of the key techniques to layout analog and mixed signal circuits are presented. The designed delta sigma modulator is compared to recent modulators with respect to the figure of merit (FOM). The FOM states the performance of a modulator in terms of speed, power consumption and resolution.

8.1 Cadence Simulation Results

Figure 8.1 shows the implementation of the cascaded third order (2-1) feed-forward delta sigma modulator. The outputs of the three integrators are given by $I_1(z)$, $I_2(z)$, and $I_3(z)$, respectively. The outputs of the second order feed-forward modulator and first order multi-bit modulator are given by $Y_1(z)$ and $Y_2(z)$, respectively. The non-overlapping clocks *phi1* and *phi2* are used along with their advanced versions *phi1a* and *phi2a*, respectively. The advanced version of non-overlapping clocks is required to eliminate second order effects like clock feed-through and charge injection.

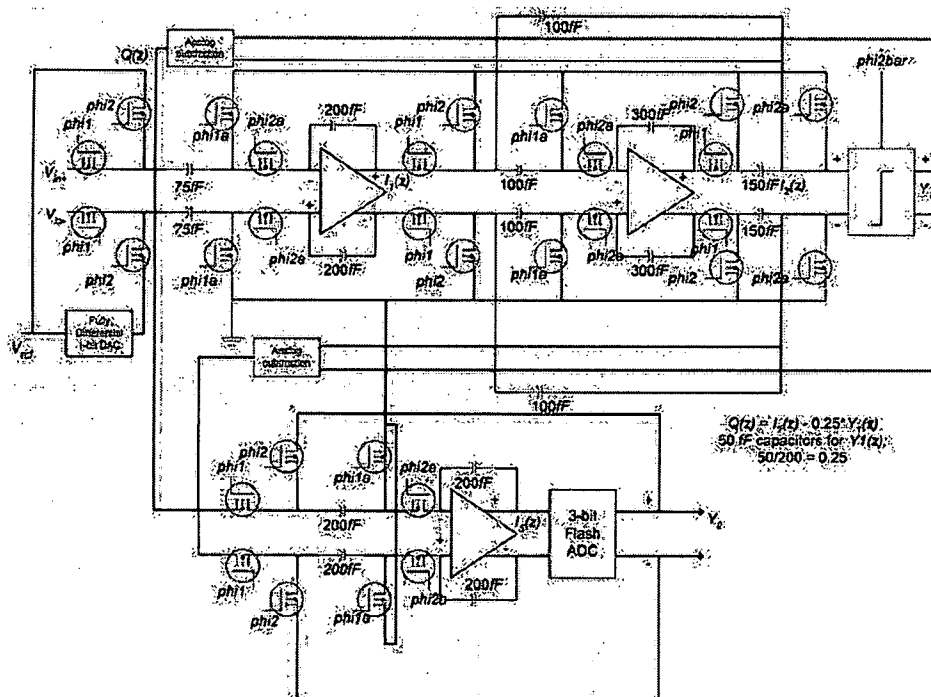


Figure 8.1 Cascaded feed-forward third order (2-1) modulator.

This modulator is realized in Cadence 0.18 μ m technology using the Spectre simulator with power supply $V_{DD} = 2.5$ V. The reference voltage V_{ref} for the second order single bit modulator is chosen to be 2.5 V because the higher the reference voltage the better is the output swing of the integrators. The reference voltages V_{refp} and V_{refn} for the multi-bit first order modulator are 2.0 V and 0.4 V, respectively. These are the maximum and minimum values allowed by the linear output swing of the op-amps. The time domain output of the first integrator $I_1(z)$ using Cadence Spectre simulations is shown in Figure 8.2(a). The gain coefficient a_1 ($75/200 = 0.375$) is chosen such that the first integrator output does not saturate and is bounded within the linear range of first op-amp (0.4 – 2.0 V). The output distribution of the first integrator is shown in Figure 8.2(b).

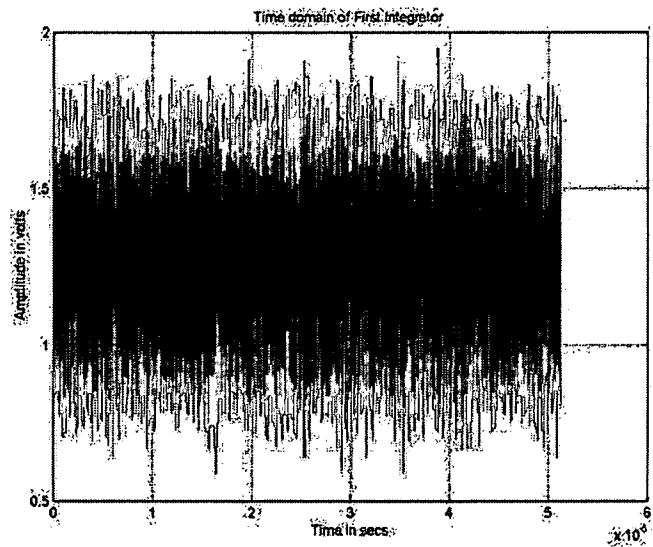


Figure 8.2(a) Time domain output of first integrator output.

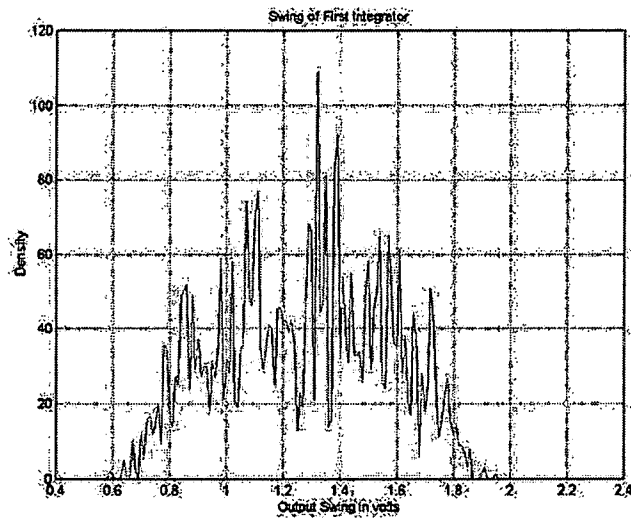


Figure 8.2(b) Output distribution of the first integrator.

The time domain output of the second integrator $I_2(z)$ is shown in Figure 8.3(a). As with the first integrator, the gain coefficient a_2 ($100/300 = 0.333$) is chosen such that the

second integrator output does not saturate and is bounded within the linear range of the second op-amp (0.4 – 2.0 V). The output distribution of the second integrator is shown in Figure 8.3(b). The noise shaping coefficients b_1 and b_2 are determined by the derivation in section 3.7 such that b_1/b_2 (100/150) = 0.66.

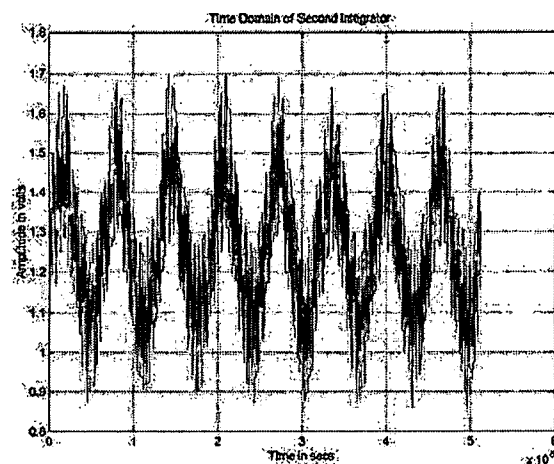


Figure 8.3(a) Time domain output of second integrator.

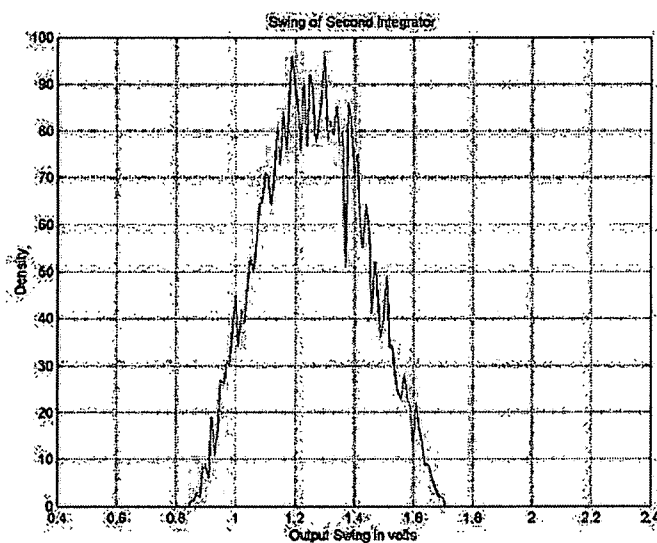


Figure 8.3(b) Output distribution of the second integrator.

The time domain output of the third integrator $I_3(z)$ is shown in Figure 8.4(a). The gain coefficient a_3 ($200/200 = 1$) is unity because the third integrator in the first order modulator is followed by a multi-bit quantizer that has better stability for high amplitude input signals and a fixed unity gain than the arbitrary gain of the single-bit quantizer. The output distribution of the third integrator is shown in Figure 8.4(b). A part of the time domain output of the second order feed-forward modulator is given in Figure 8.5. The time domain output of the first order multi-bit modulator with quantization noise as its input is shown in Figure 8.6.

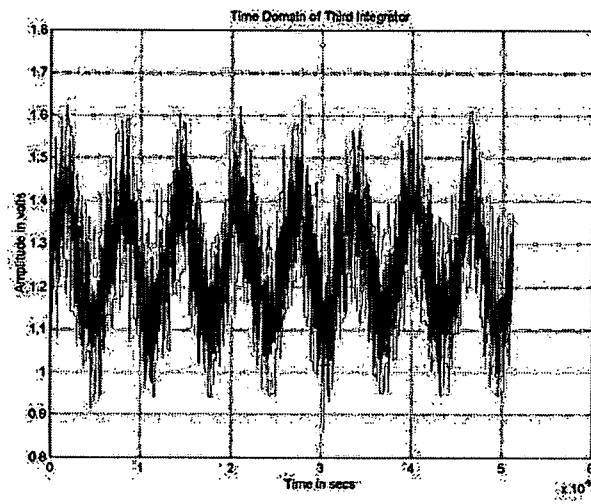


Figure 8.4(a) Time domain output of third integrator.

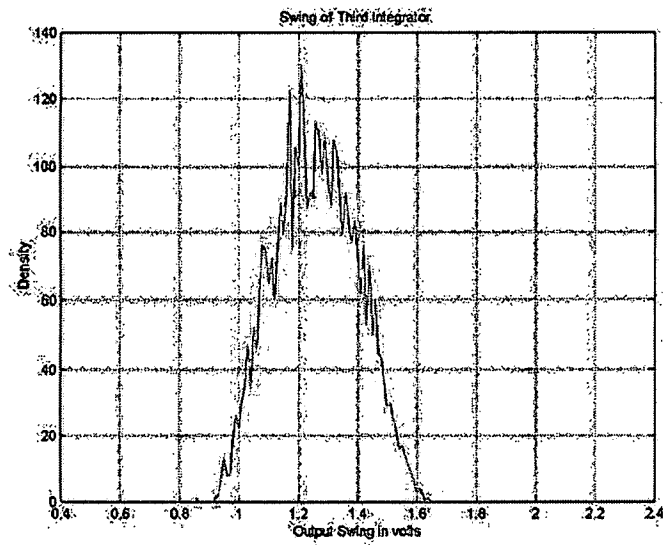


Figure 8.4(b) Output distribution of the third integrator.

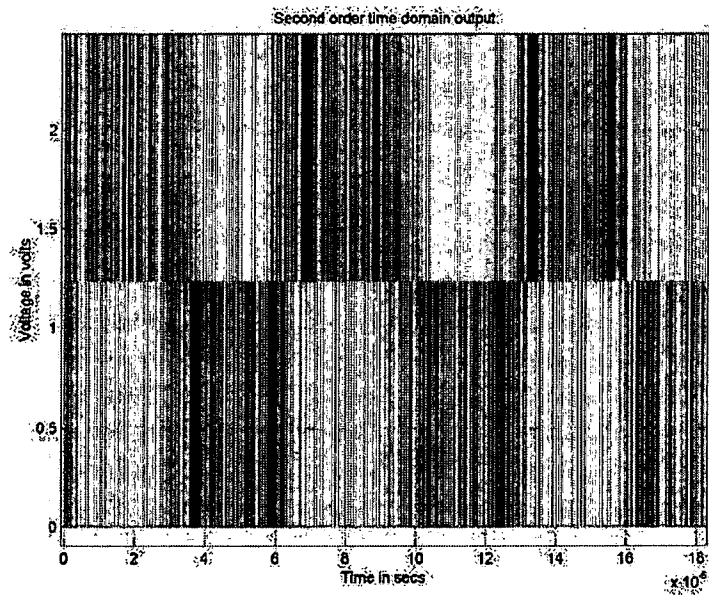


Figure 8.5 Time domain output of the designed second order modulator.

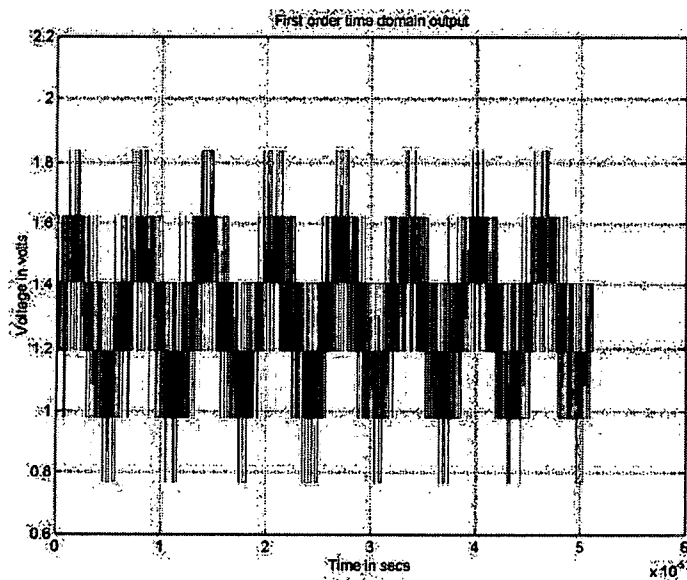


Figure 8.6 Time domain output of the designed first order multi-bit modulator.

The second order modulator output $Y_1(z)$ and the first order modulator output $Y_2(z)$, undergo digital noise cancellation logic (NCL) as shown in Figure 8.7. The digital gain coefficients d_1 (4), d_2 (4), and the gain coefficient for the input signal d_{21} (6) are used in this NCL.

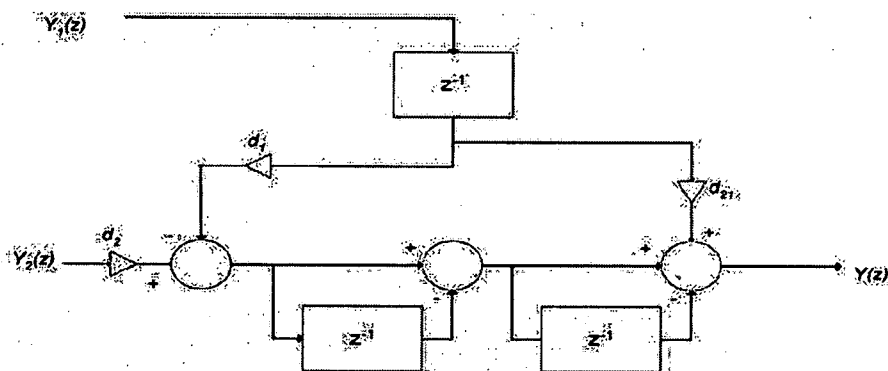


Figure 8.7 Digital noise cancellation logic.

As can be seen from Figure 8.7, $Y_1(z)$ is delayed by one clock cycle (z^{-1}), the signal transfer function (STF) of the first order modulator. It is then scaled (d_1) and subtracted from the scaled version (d_2) of $Y_2(z)$. The difference is then differentiated twice $(1 - z^{-1})^2$, the noise transfer function (NTF) of the second order modulator. The differentiated output is summed with the scaled version (d_{21}) of $Y_2(z)$ to produce the final output $Y(z)$. This entire operation is called digital noise cancellation. The power spectral density (PSD) of the final output $Y(z)$ for SNR and SINAD calculations is shown below in Figure 8.8. The sampling frequency used for simulating the delta sigma modulator is 80 MHz and the desired signal bandwidth is 1.25 MHz. An input signal of -5 dB full scale at a frequency of 156.25 KHz was provided to the delta sigma modulator. That frequency was selected to obey the coherent sampling operation. Coherent sampling is the synchronization of the quantization error with the sampling frequency and is used in order to avoid picket fence and spectral leakage errors. More information about coherent sampling and effects due to non-coherent sampling are explained in [29]. The SNR of the designed cascaded third order feed-forward delta sigma modulator is 75 dB for a 4096-point FFT, which is close to the SNR of 74.26 dB obtained from the Matlab algorithm. The SNDR of the designed cascaded third order feed-forward delta sigma modulator is 70 dB for a 4096-point FFT. The power consumption of the modulator without the digital noise cancellation is 12.74mW and the resolution is 12.16 bits.

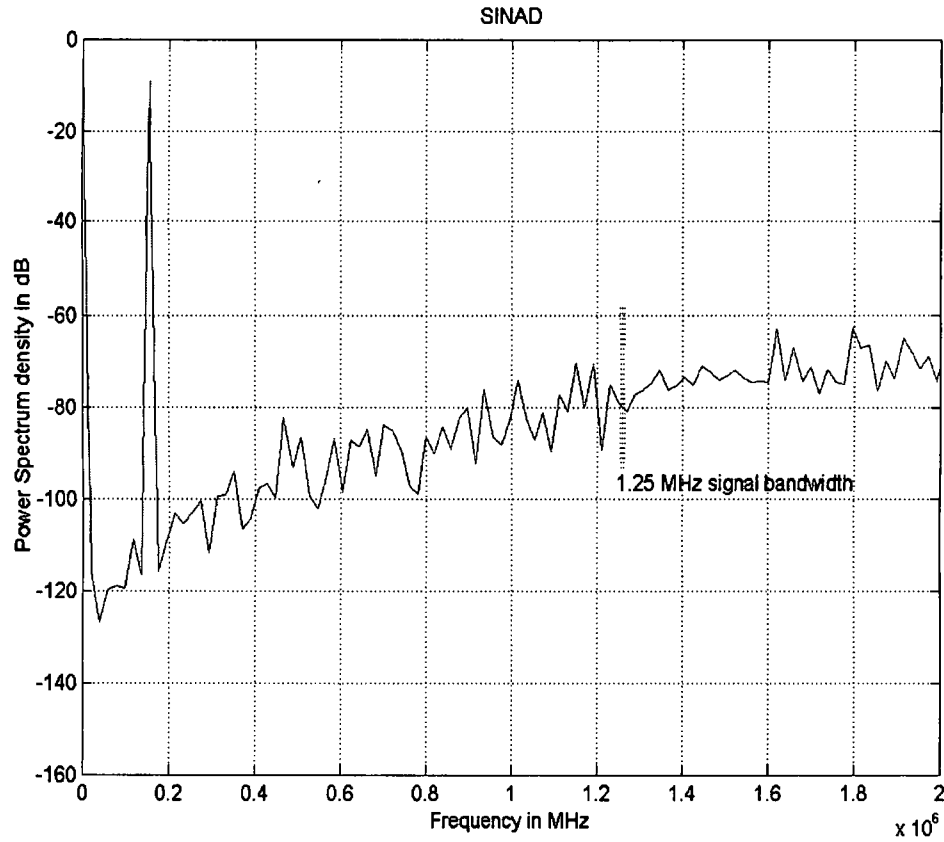


Figure 8.8 PSD of the designed cascaded third order feed-forward delta sigma modulator.

The SNR and SNDR of this modulator are plotted against various input amplitudes. Figure 8.9 shows the plot of SNR, SNDR for various input amplitudes at a fixed frequency of 156.25 KHz and over-sampling ratio $M = 32$.

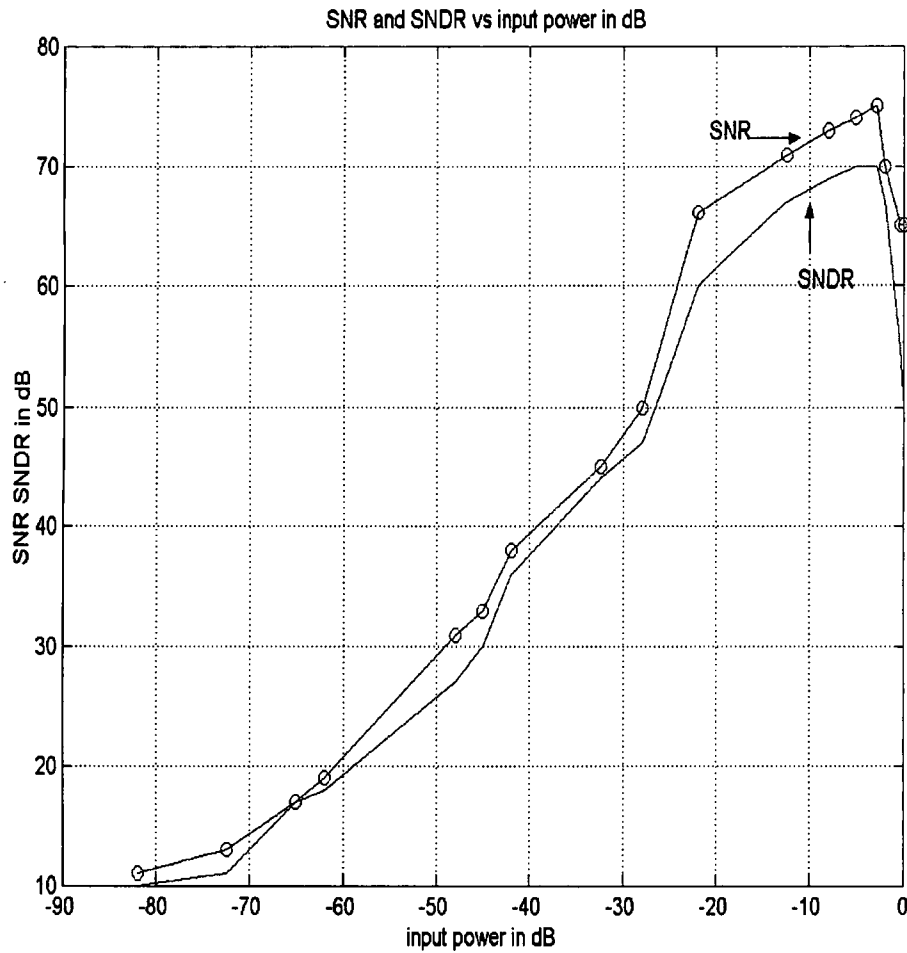


Figure 8.9 SNR, SNDR with respect to various amplitudes at fixed frequency of 156.25 KHz and $M = 32$.

8.2 Quantization Noise

The quantization noise or the quantization error signal, which is the input to the next stage, is obtained by subtracting the scaled version of the feed-forward modulator output $Y_1(z)$ from the output of the second integrator $I_2(z)$. Scaling should be performed to avoid overloading the input to the next stage, else serious harmonic degradation occurs and

SNR is dropped drastically. $Y_1(z)$ should be scaled exactly by the inverse of the quantizer gain k_1 such that the signal is completely eliminated from the next stage and only random quantization noise exists. For example if the modulator is not exactly scaled by c_1 (0.25), a part of the signal is passed through to the next stage. Figure 8.10 shows the frequency domain of the quantization when the modulator output is scaled by 0.27 instead of exact quantizer gain (0.25). Figure 8.11 shows the frequency domain of the quantization noise when the modulator output is scaled by the exact quantizer gain of 0.25.

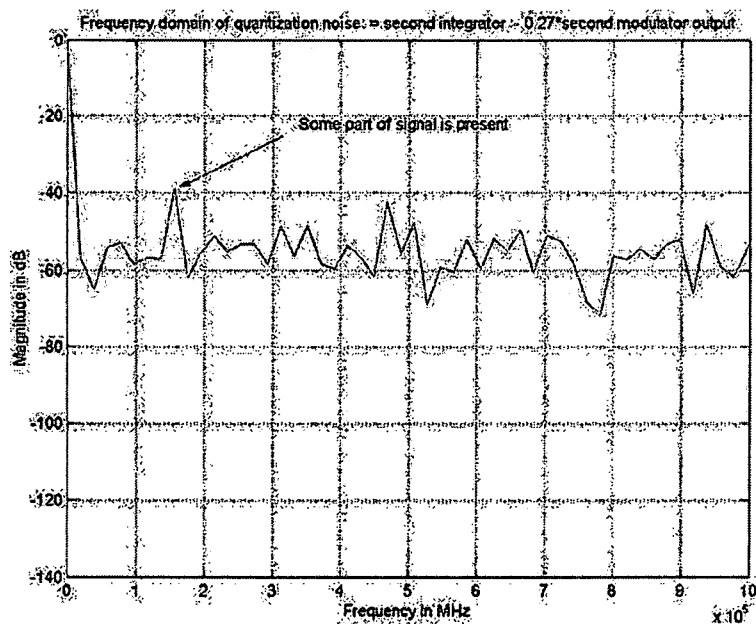


Figure 8.10 Frequency domain of the quantization noise when modulator output is scaled by 0.27.

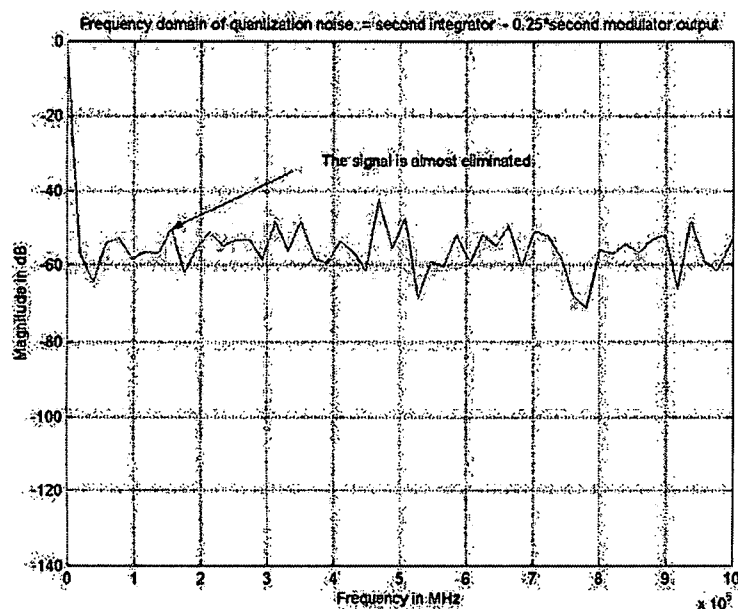


Figure 8.11 Frequency domain of the quantization noise when modulator output is scaled by 0.25.

8.3 Cadence Layout Results

This modulator is realized in Cadence Virtuoso Layout XL 0.5 μ m (0.6 μ m drawn) technology using Spectre simulator with power supply VDD = 5 V. The gain coefficient a_1 (500fF / 1333fF = 0.375) is chosen such that the first integrator output does not saturate and is bounded within the linear range of op-amp (1 – 4 V). As with the first integrator, the gain coefficient a_2 (500fF / 1500fF = 0.333) is chosen such that the second integrator output does not saturate. The noise shaping coefficients b_1 and b_2 are determined by the derivation in section 3.7 such that b_1/b_2 (166fF / 250fF) = 0.66. The gain coefficient a_3 (500fF / 500fF = 1) of third integrator in the first order modulator is unity. The reference voltage V_{ref} for the second order single bit modulator is 5 V for high dynamic output range of the integrators. The reference voltages V_{refp} and V_{refn} for the multi-bit first order

modulator are 4 and 1, respectively. Figures 8.12 and 8.13 show the time domain output of the second order and the first order modulators, respectively.

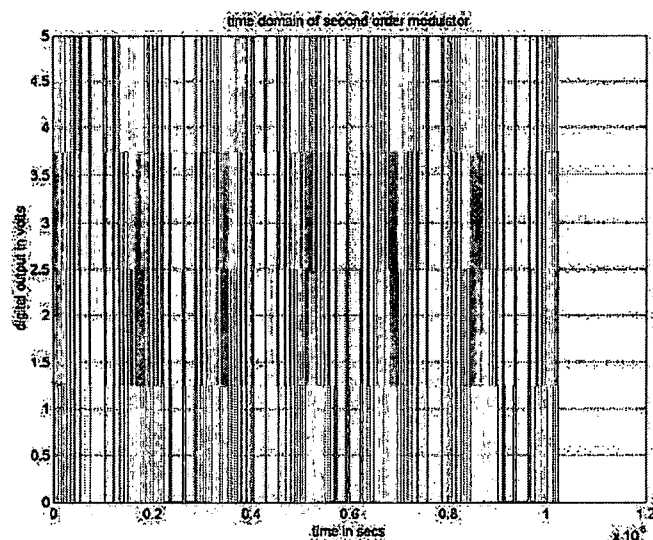


Figure 8.12 Time domain output of the implemented second order modulator.

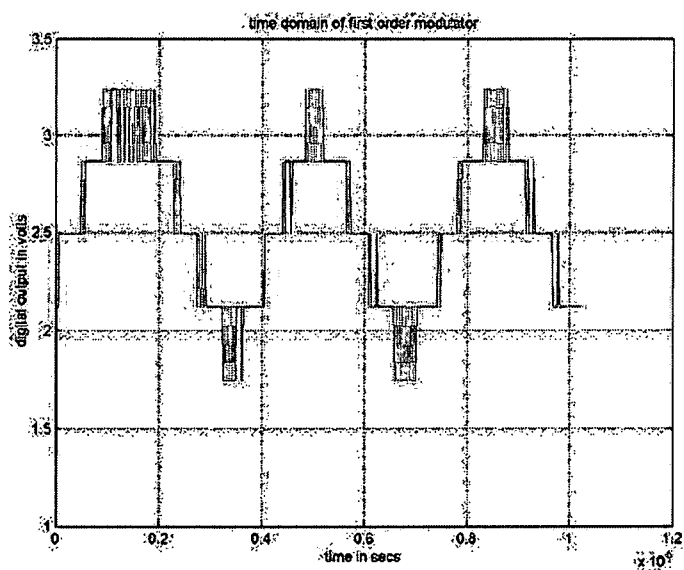


Figure 8.13 Time domain output of the implemented first order modulator.

Various essential techniques [64] were employed to realize the physical layout of the cascaded feed-forward (2-1) delta sigma modulator. An overview of these techniques will be presented in this section.

1. For designing digital circuits, standard cells having fixed height and variable width are recommended. This technique can also be used in custom analog circuits because it makes cell placement and wiring easier.
2. It is essential to measure the current density of each wire or metal in the circuit and make sure that the widths of the metal have a current handling capacity of 0.5mA per micron.
3. For high frequency signals, the lowest parasitic metal should be used. In general, it is advisable to use the wide metal wires than wires with minimum width and vias for lowering resistance and faster distribution of input or clock signals.
4. Special attention should be paid to the orientation and matching of transistors wherever required. A consistent horizontal or vertical orientation of CMOS transistors should be practiced to avoid problems during fabrication. In analog circuits, many components need to match a given device called the defining component. Placing the defining or the root component in the center and wrapping the other components around it is called interdigitation. This technique will keep the property of matched transistors as close to each other as possible yielding better performance. Figure 8.14 shows the interdigitation procedure. For proper matching and higher precision of circuit elements, dummy elements must be placed for identical etching of components. Figure 8.15 shows how matching and interdigitation of transistors are performed by placing the transistors as close to each other as possible with the same orientation.

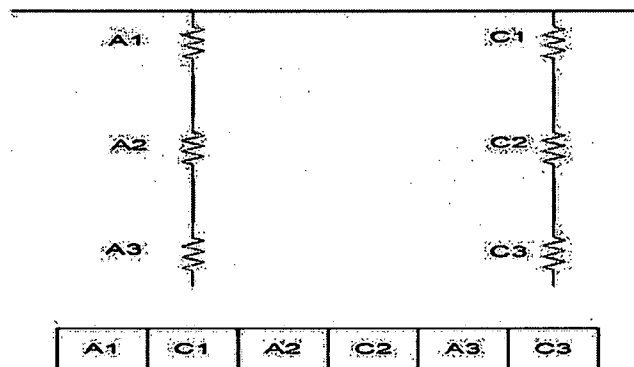


Figure 8.14 Interdigitation.

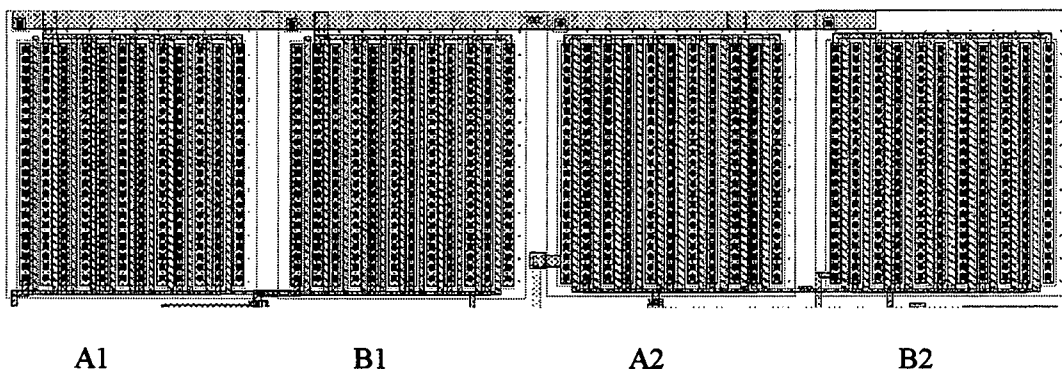


Figure 8.15 Matching and interdigitation of transistors.

5. The common centroid arrangement is ideal because it not only reduces the effect of thermal gradients but also solves problem arising from process gradients. In this arrangement, all the devices are placed around a common central point. This arrangement distributes any non-linearity due to thermal and process gradients evenly among all devices. Figure 8.16 shows the centroid arrangement of the seven 3-bit pass-gates and comparators implemented to design 3-bit ADC.

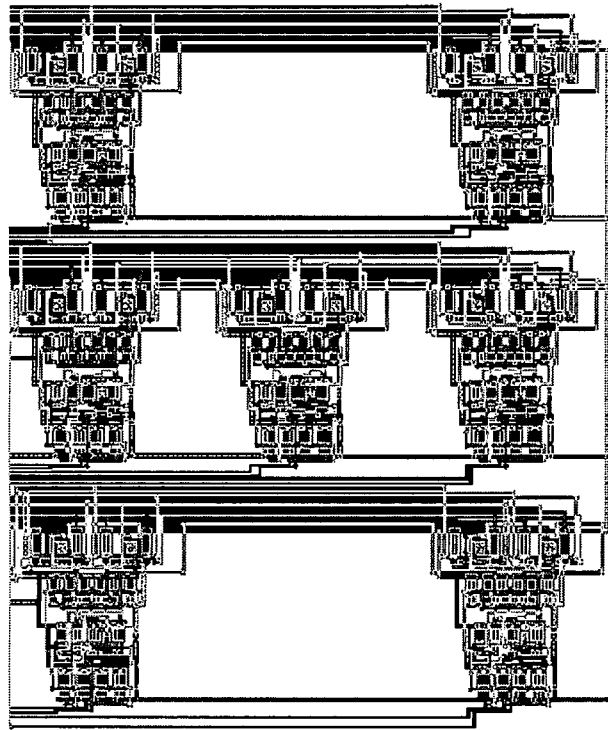


Figure 8.16 Centroid arrangement of seven pass-gates and comparators.

6. In high frequency analog circuits and particularly differential circuits, symmetry among matching devices should be preserved. This means all the component blocks, signals, elements within the component blocks should be symmetrical.

7. Floor planning is an essential key to designing integrated chips. In analog design, a frequent reshaping and resizing of circuits is required to meet the system specifications. This suggests that instead of cramming and laying out smaller chips it is advisable to leave enough room among blocks.

8. The power supply rails should be made 10% of the cell height. Also wires running over capacitors, resistors and other circuits should be avoided. Many substrate contacts should be placed around noisy devices to isolate them from neighboring circuits.

The sampling frequency used for physical layout of the delta sigma modulator is 50 MHz and the desired signal bandwidth is 1.25 MHz. An input signal of -5 dB full scale at a frequency of 292.96875 KHz was provided to the delta sigma modulator. The SNR of the implemented delta sigma modulator is 64 dB for a 1024-point FFT. A lesser sampling frequency of 50 MHz was chosen because of the speed and power limitations imposed by the higher 0.5 μ m (0.6 μ m drawn) sub-micron technology. The final chip layout of the cascaded feed-forward third order modulator is shown in Figure 8.17. The components used in the physical layout of this final modulator can be found in Appendix D. The power spectral density (PSD) of the modulator is shown in Figure 8.18. The power consumption of the implemented modulator without the digital noise cancellation is 63.44mW and the resolution is 10.33 bits. The total area occupied by this modulator without the digital noise cancellation is $1800\mu\text{m} \times 800\mu\text{m} = 1.44 \text{ mm}^2$.

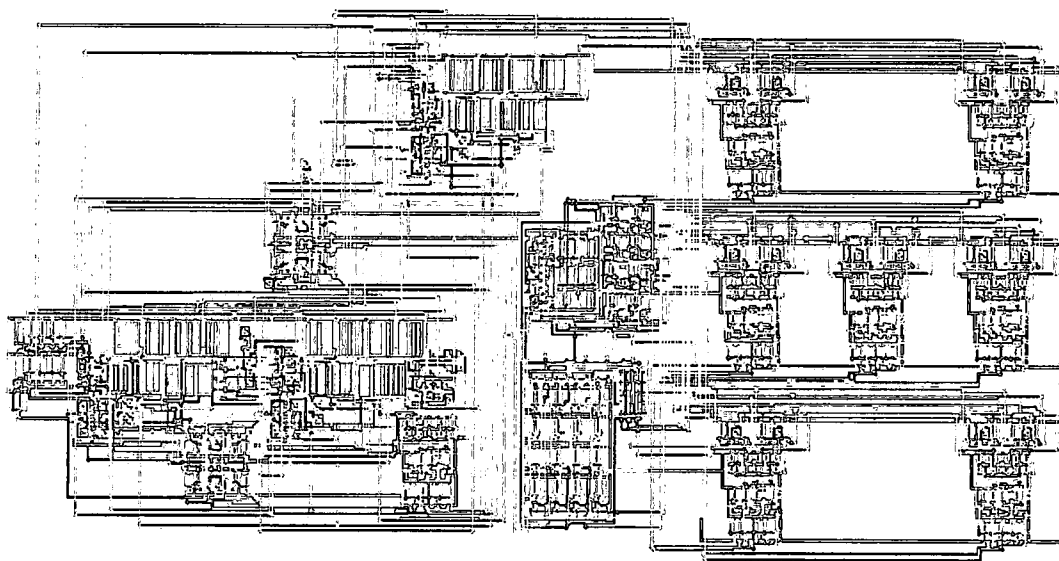


Figure 8.17 Physical layout of cascaded feed-forward third order modulator.

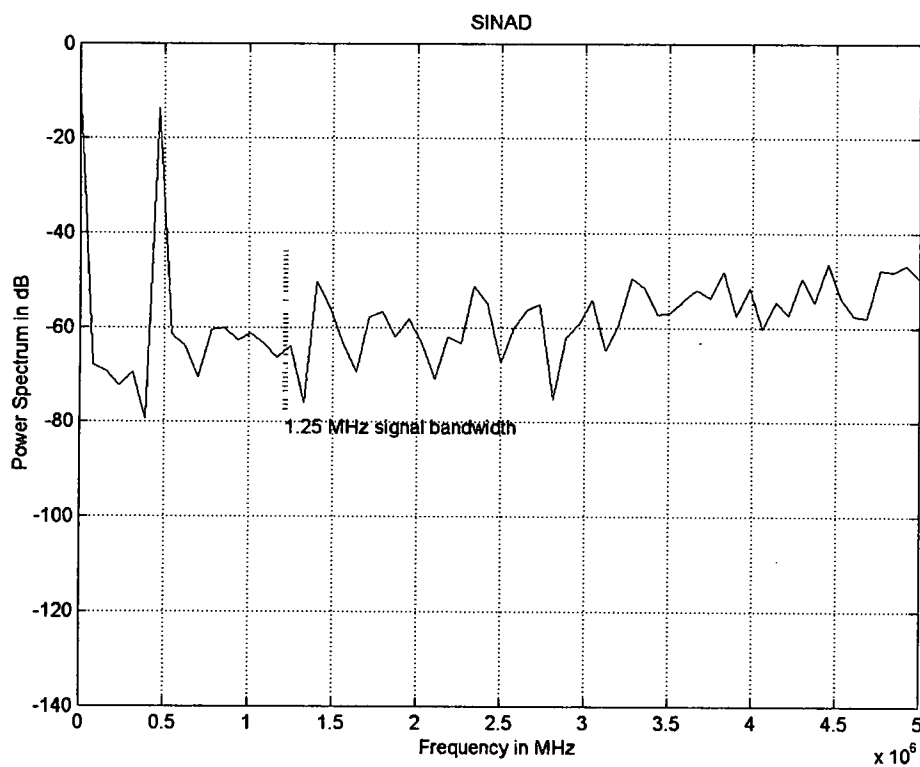


Figure 8.18 PSD of the implemented cascaded feed-forward delta sigma modulator.

8.4 Figure of Merit (FOM)

A Figure of Merit (FOM) is a parameter for comparison of the performance of delta sigma modulators. This formula was first proposed by [59] and is presented in equation (8.1).

$$\text{FOM(J)} = \frac{\text{Power(W)}}{2^{\text{Resolution (bits)}} \times \text{DOR(S/s)}} \times 10^{12} \quad (8.1)$$

Power represents the power consumption of the modulator. The digital part of the mixed signal modulator is designed using software algorithms like Matlab or C/C++. The resolution is the number of bits or the conversion performance of the data converters. DOR is the digital output rate that is obtained after digital filtering is employed to remove the out-of-band noise. The FOM for the designed delta sigma modulator is 1.11 pJ. The FOM for the chip layout of delta sigma modulator is 19.71 pJ. The FOM of the implemented modulator is quite large but the area occupied is considerably small compared to the state-of-art delta sigma modulators. Table 8.1 provides a summary of the designed and the implemented 2-1 cascaded feed-forward delta sigma modulator.

Table 8.1 Summary of the cascaded feed-forward 2-1 delta sigma modulator.

Features	Designed 2-1 Modulator	Implemented 2-1 Modulator
Sampling Frequency	80 MHz	50 MHz
Signal bandwidth (DOR)	1.25 MHz (2.5 MS/s)	1.25 MHz (2.5 Ms/s)
SNR	75 dB	64 dB
Power Consumption (VDD)	12.74mW (2.5 V)	63.44mW (5V)
Resolution	12.16 bits	10.33 bits
FOM	1.11 pJ	19.7 pJ

Table 8.2 gives the comparison of the designed delta sigma modulator with contemporary low-pass delta sigma modulators.

Table 8.2 Comparison of low-pass delta sigma modulators in terms of FOM.

Ref. (no.)	Res. (Bits)	DOR (kS/s)	Power (mW)	Process(μ m) /Supply(V)	Architecture	F _s (MHz)	FOM (pJ)
Gaggl [46]	13	2200	8 ^a	0.13/1.5	2(3b),DEM	105	0.44
Reutemann [60]	14	2500	33	0.25/2.5	5 FF(tri-level)	80	0.59
Fujimori [61]	16	2500	105	0.5/5-3	2(4b)-1(4b)- 1(4b),DWA	20	0.64
This work	12.16	2500	12.74	0.18/2.5	2-1(3b)	80	1.11
Vleugels [22]	15.0	4000	90	0.5/2.5	2(5b)-1(3b)- 1(3b),DWA	64	1.14
Harb[48]	12.6	2000	18.8	0.18/1.8	2-1-1	50	1.51
Balmelli [62]	14	2000	50	0.25/2.5	5-FF(tri-level)	80	1.53
Gupta [63]	14.3	2200	92	0.18/3.3	2-2-2(tri-level)	64	2.04
Geerts[66]	15.0	2500	295	0.65/5	3-FB(6b)-DWA	60	2.07
Rio[67]	13.8	2200	65.8	0.25/2.5	2-1-1(3b)	70.4	2.25
Geerts[21]	15	2200	200	0.5/3.3	2-1-1(FF)	52.8	2.77
Miller[18]	12.83	1250	30	0.18/2.7	2-(FB)(6b)	23	3.29
Miller[18]	11.67	3840	50	0.18/2.7	2-(FB)(6b)	46	4.00
Marques [68]	14.80	2000	230	1.00/5	2-1-1	48	4.03
Morizio [69]	12	2200	99	0.35/3.3	2-2	52.5	4.16
Morizio [69]	13	2200	150	0.35/3.3	2-2-2	52.5	5.49
Kuo[70]	13	2000	105	0.25/2.5	4-(4b)-DWA	48	6.41
Feldman [52]	13	1400	81	0.7/3.3	2-2-2	22.4	7.06
Brooks[71]	14	2500	435	0.6/5	2(5b)-0(12b)	20	9.49

FF : Feedforward

FB : Feedback

DWA : Data Weighted Averaging

There is a trade-off between power consumption and resolution among these delta sigma modulators. Although the delta sigma modulators designed in [46, 60, and 61] have better resolution; they have higher power consumption compared to the designed modulator. The modulator designed in [46] has an over-sampling ratio (48) that is much greater than the designed modulator (32); hence resolution is better because resolution is proportional to the over-sampling ratio. The FOM of this modulator is lowest among all other modulators because of its high over-sampling ratio. The modulator implemented in [60] has better resolution than the designed modulator at the expense of higher power consumption. In [61], a modulator with even better resolution is presented but at the expense of much higher power consumption of 105mW and larger area of 24 mm². All other modulators have high resolution but high power consumption. The modulator designed in this dissertation has the lowest power consumption among the recent modulators. It can also be observed from Table 8.2 that the modulators are designed using different architectures. Most of these modulators are very complex to design compared to the designed modulator. The simple architecture, low power and compact design of the proposed modulator is traded off for a little less resolution. FOM is a parameter typically used to determine the performance of the modulator in terms of DOR, power consumption and resolution. It does not take into account the area occupied by the modulator. Table 8.2 clearly shows that the proposed modulator has quite a low FOM compared to several modulators in its class; hence, advances the state-of-art technology.

The area occupied by any integrated circuit depends upon the process and the sigma delta architecture used to obtain a desired resolution at a particular sampling frequency. The area and resolution are generally inversely proportional to each other. A higher resolution demands a much larger area at a particular process technology. Table 8.3 compares the proposed delta sigma modulator with other delta-sigma in terms of their area.

Table 8.3 Comparison of low-pass delta sigma modulators in terms of area.

Ref. (no.)	Res. (Bits)	DOR (kS/s)	Area (mm ²)	Process(μ m) /Supply(V)	Architecture
Yu[72]	8.16	2200	0.4	0.09/1.3	2-FB(4b)
This work	10.33	2500	1.44	0.6/5	2-1(3b)
Miller[18]	11.67	3840	1.44	0.18/1.8	2-(FB)(6b)
Reutemann [61]	14	2500	1.5	0.25/2.5	5-FF(trilevel)
Morizio[69]	12	2200	1.7	0.35/3.3	2-2
Rio[67]	15.8	2200	2.78	0.25/2.5	2-1-1(3b)
Feldman [52]	13	1400	3.6	0.7/3.3	2-2-2
Geerts[21]	15	2200	5	0.5/3.3	2-1-1(FF)
Marques[68]	15	2000	5.27	1.00/5	2-1-1
Geerts[66]	15.0	2500	5.3	0.65/5	3-FB(6b)-DWA
Vleugels [22]	15	4000	10	0.5/2.5	2(5b)-1(3b)- 1(3b),DWA
Fujimori [61]	16	2500	24.8	0.5/5	2(4b)-1(4b)- 1(4b),DWA
Brooks[71]	14	2500	35.3	0.6/5	2(5b)-0(12b)
Chang[73]	12	1540	65	0.7/5	2-1-1

Table 8.3 shows that the proposed delta sigma modulator with second order feed-forward modulator and a multi-bit modulator has the smallest area compared to several architectures. The proposed ADC has not only low FOM but also small area, which makes it an enticing alternative to other delta-sigma architectures for commercial RF wireless applications.

9 CONCLUSION AND FUTURE WORK

A design and implementation of a new cascaded modulator was successfully completed for wireless applications requiring high data output rate. The specifications obtained for the designed modulator are met in terms of FOM compared to recent designs with similar technology and comparable data output rates. The layout of the delta sigma modulator has a comparatively poorer FOM than the delta sigma modulators in its class. The high power consumption and one bit below-par resolution is traded off for a considerably less area. The novel systems contributing to the state of art technology are as follows:

1. A cascaded third order model along with feed-forward elements and multi-bit quantizer is a novel approach in this dissertation. There is considerable reduction in noise due to cascade of first order modulator and second order feed-forward ADC; in addition, the simple feed-forward elements with just one feedback path, makes this ADC architecture attractive for high performance ADCs in wireless applications.
2. Use of differential flash ADC with a novel thermometer-to-binary encoder. The modulator was implemented using fully-differential architecture for obtaining high performance. The second and higher order feed-forward modulators have advantages like lower complexity and smaller area over the feed-back modulators because feed-forward modulators have a single digital-to-analog converter (DAC) whereas its counterpart have multiple DACs. A novel *NMOS-PMOS* thermometer-to-binary encoder, which was incorporated in the design of the multi-bit analog-to-digital converter (ADC), has a

smaller area, low power consumption, and high speed than many conventional encoders. The designed modulator has a 12.16-bit resolution at a data output rate of 2.5 MS/s for an over-sampling ratio of 32. The implemented modulator has 10.33-bit resolution at the same data rate for an over-sampling ratio of 20. The power dissipation of the designed and implemented modulators is 12.74 and 63.44mW, respectively.

The chip layout of this modulator was carried out in 0.5 μ m (0.6 μ m drawn length) technology (VDD = 5V). The design constraints like high resolution, low power consumption, and high speed become much more stringent to achieve in deep sub-micron technologies such as 0.18 μ m and 0.13 μ m because of low power supply voltages of 2.5 V and less. The analog circuits require good dynamic range at their outputs in order to have substantially high resolution. An optimum balance of power consumption and speed is difficult to accomplish. The low voltage and low power challenges serve as a good motivation for implementing circuits in deep-submicron technologies. It will be interesting to implement the proposed modulator in 0.18 μ m or 0.13 μ m CMOS technology and compare its performance with the desired performance of the designed delta sigma modulator.

The state-of-the-art mixed-signal data converters need to be implemented along with the digital circuits on a single chip. This system-on-chip (SOC) requirement facilitates the use of high density and low power CMOS technology. Bottlenecks like signal mismatch, sensitivity, accuracy and stability introduced by analog components in the receiver front-end decrease the performance of the overall receiver. These bottlenecks can be overcome by high precision digital circuits. The ADC can be moved towards the antenna in receiver architectures and number of analog front end (AFE) stages should be minimized

as much as possible. This requires designing high resolution ADCs at very high sampling frequencies and signal bandwidths. The minimum length specification of CMOS technologies complicates the design of high speed, high resolution ADCs. Thus, alternative technologies of implementing data converters should be explored. More time should be invested in designing delta sigma modulators and its performance in very high speed technologies such as GaAs or SiGe should be investigated. This serves as my topic of future interest. In future work, I recommend improvements in the implementation of the modulator and further efforts be made towards reducing the power consumption and increasing the resolution of the modulator.

Appendix A Basic ADC and DAC Designs

A. 1 Analog-to-digital converter (ADC)

An analog-digital-converter (ADC) can be designed in several ways. Different types of ADC include [26].

A.1.1 Flash ADC

For an N -bit Flash ADC in Figure A.1, the reference voltage is divided into 2^N values using resistors, each of which is fed into a comparator through voltage division. The comparator compares this value with the input signal voltage and outputs logic 1 or 0 appropriately. The output is decoded using thermometer-code logic to produce a binary output code. The Flash ADCs are generally used for high speed (GHz range) and low resolution applications. The input analog signal is converted into digital signal in one clock cycle.

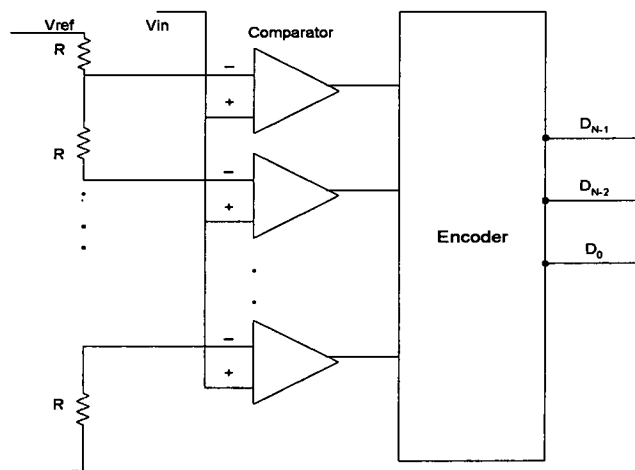


Figure A.1 Flash ADC. [26]

A.1.2. Two-step Flash ADC

Figure A.2 shows the Two-step Flash ADC architecture. The first ADC does a coarse estimate of the input signal to process the MSBs (MSB of digital signal). This estimate is converted back to analog domain by a DAC and subtracted from the original signal. The residue is amplified and then processed by the second stage which performs a fine analog-to digital conversion to obtain the LSBs (LSB of digital signal). Two step Flash ADC have higher resolution than Flash ADCs but run at lower speeds.

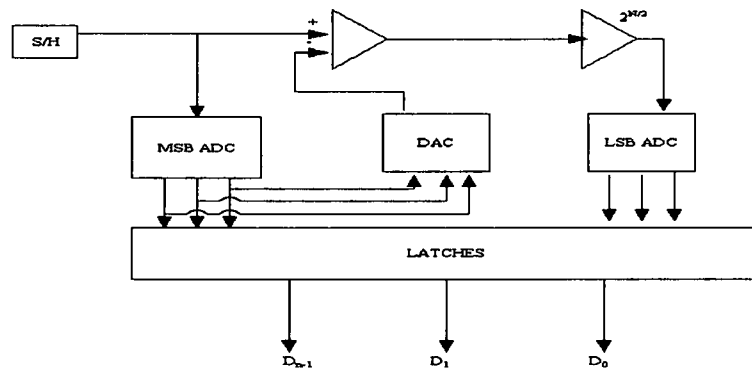


Figure A.2 Two-step flash ADC.

A.1.3. Pipeline ADC

An N -stage pipeline ADC consists of N first order stages connected in series. Each stage, shown in Figure A.3, contains a 1 bit ADC (a comparator), a sample and hold, a 1 bit DAC (switch), and an amplifier. After the input is sampled by sample-and-hold, it is compared to half the reference voltage. The output of each comparator is the digital output for that stage. If input signal is greater than half the reference voltage then, the comparator output is high; one-half of the reference voltage is subtracted from original

input and passed to the amplifier. If input signal is lesser than half the reference voltage then, output is logic 0, the original signal is passed to the amplifier and to the sample-hold of the next stage. The first output requires N clock cycles, but each subsequent output is generated every clock cycle. Pipeline ADC have high resolution and high speeds of operation, but very less noise shaping.

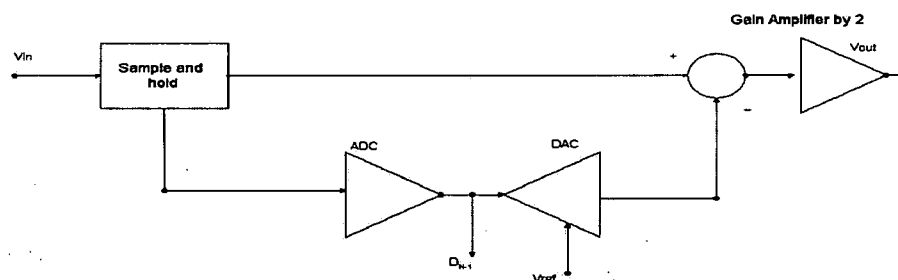


Figure A.3 Pipeline ADC [26].

A.1.4. Successive Approximation (SAR) ADC

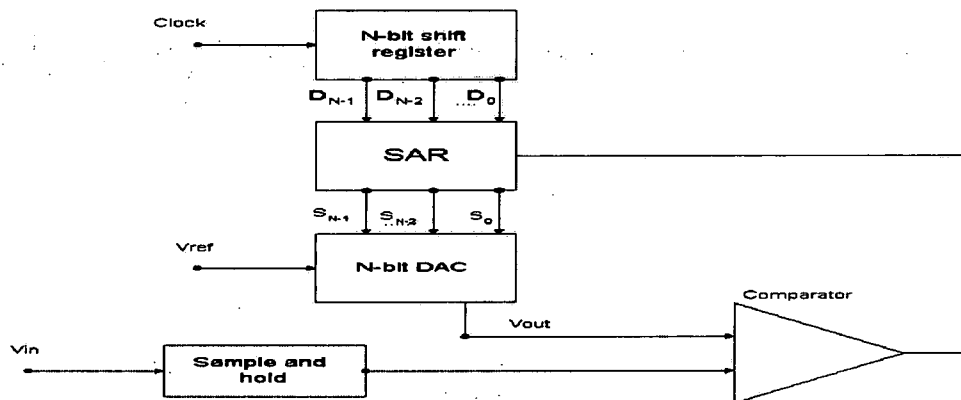


Figure A.4 Successive approximation (SAR) ADC.

A successive approximation ADC is presented in Figure A.4 [65]. A successive approximation ADC includes an N -bit shift register, a comparator, a sample and hold, an N -bit DAC converter, and an N -bit successive approximation register (SAR), where N is the resolution. Before applying the original signal, an initial set-up is performed. A "1" is applied to the shift register and the MSB of both shift register and SAR are set to 1. All other bits of both the registers are 0. Whenever a bit conversion is affected, the 1 applied to shift register is shifted by one position with all other bits 0. The SAR operates in relation with the comparator. If the comparator output is 1 the corresponding bit in the SAR for that bit conversion is set to 0. If the comparator output is 0 then the corresponding digital output of SAR is 1 with other digital bits 0. The SAR output controls the DAC. The original input is sampled and compared with the DAC output, which is initially half the reference voltage because the MSB of SAR is 1, while other bits are 0. If the DAC output is greater than the input signal, then comparator resets the corresponding output of SAR to 0. The output of the SAR is the final digital output. A SAR ADC needs n cycles for n -bit resolution, while a flash ADC requires only one clock cycle. SAR ADC is used for low power and medium rate conversion rates.

A.2 Digital-to-analog converter (DAC)

A digital-to-analog converter (DAC) transforms signals from digital to analog domain. A DAC should provide good linearity and correct quantized analog output for corresponding digital output. There are several types of digital to analog converters [26]:

A.2.1. R-2R DAC

An R-2R DAC shown in Figure A.5 is a network of binary weighted resistors alternating in R and 2R resistor values. Each node voltage is the reference voltage caused by the voltage division of ladder network. D_0 , D_1 , and D_2 are the digital inputs to the system and V_{out} is the analog output of the R-2R DAC. V_{ref} is the reference voltage which is divided to obtain appropriate analog values. According to the presence of digital one or zero, the resistor is connected to the op-amp or ground. For example if $D_0 = 1$ and $D_1 = D_2 = 0$; then $V_{out} = V_{ref}/8$. The current through the feedback resistor R_f determines the corresponding analog voltage.

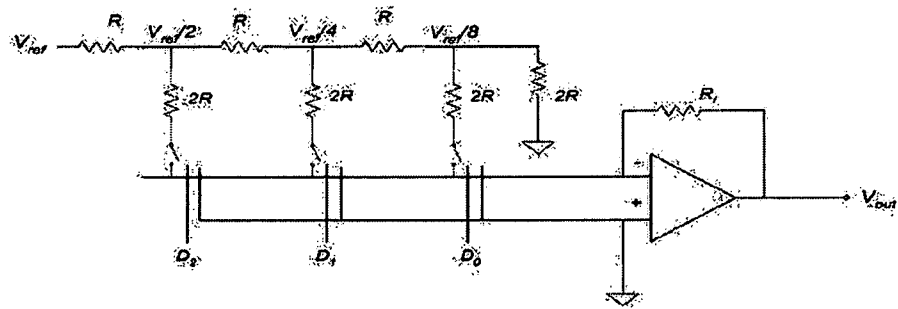


Figure A.5 R-2R DAC.

A.2.2 Charge Scaling DAC

A charge scaling DAC can be seen in Figure A.6. The parallel array of binary-weighted capacitors, totaling $2NC$, is connected to an op-amp. In *Reset* mode, all capacitors are connected to ground. After initially being discharged, each capacitor is switched to either ground or the reference voltage depending on the input digital bit, as in the case of the R-2R network. The analog output voltage V_{out} is the function of voltage division between the capacitors.

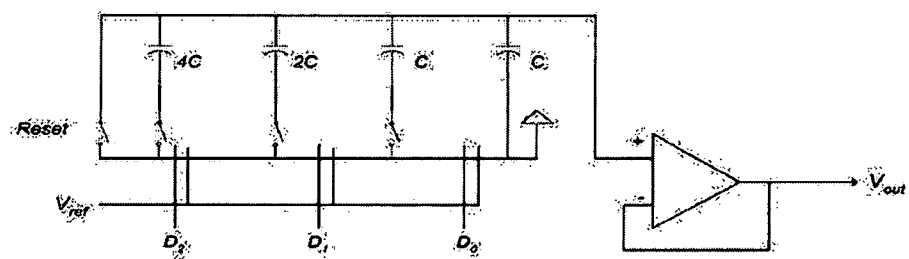


Figure A.6 Charge scaling DAC.

Appendix B Static and Dynamic Parameters

In this appendix, static and dynamic parameters of a DAC are mentioned. The static and dynamic parameters of an ADC can be found in [26]. Static parameters such as integral non linearity, differential non linearity, offset error, gain error do not vary with time. Static parameters of DAC such as integral non linearity, differential non linearity have a profound effect on the linearity of the entire system; therefore, should be highly optimized. Dynamic parameters are very important in high-speed applications such as digital communications, ultrasonic imaging, instrumentation and IF digitization.

B.1 Offset Error

The difference between the first code transition and the ideal value of $\frac{1}{2}$ LSB is the offset error as shown in Figure B.1. Offset error may be expressed in terms of percent or full scale voltage.

$$E \text{ (offset)} = (V' \text{ min} - V \text{ min}) / V_{LSB}$$

Here, $V \text{ min}$ is the smallest ideal reference voltage.

$V' \text{ min}$ is the smallest actual reference voltage.

$V \text{ max}$ is the largest ideal reference voltage.

$$V_{LSB} \text{ (least significant bit)} = V_{fsr} / 2^n - 2$$

V_{fsr} is the full scale range of the reference voltage given by $V_{max} - V_{min}$

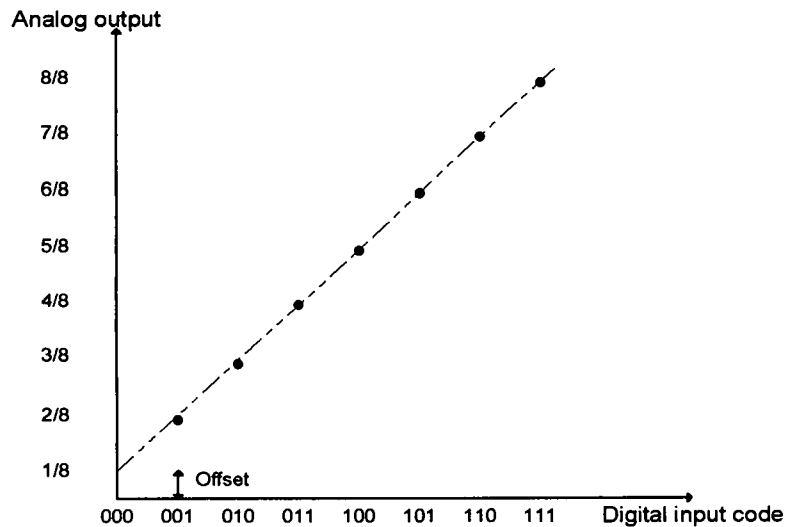


Figure B.1 Offset error of a 3-bit DAC.

B.2 Gain Error

Gain error is the difference in the slope of a straight line drawn through the transfer characteristics and the slope of 1 obtained from an ideal ADC.

B.3 Differential Non Linearity (DNL)

In an ideal converter, the code to code transitions or step-size are exactly 1 LSB apart. Differential non linearity in Figure B.2 is the difference between actual increments in the code transition to the ideal height of the code transitions, which corresponds to 1 LSB [26].

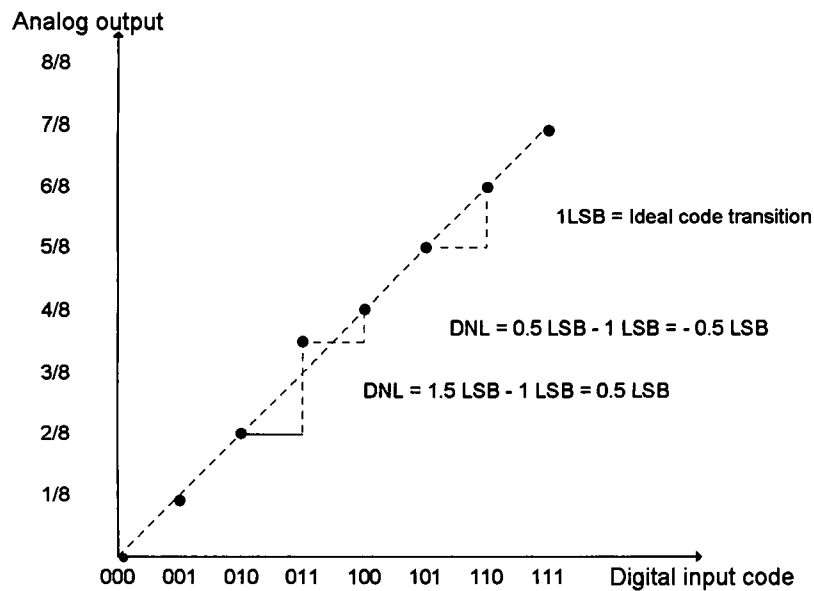


Figure B.2 DNL for a 3-bit DAC.

B.4 Integral Non Linearity (INL)

Figure B.3 describes the departure from the ideal linear transfer curve of the DAC (or an ADC). It is a measure of the straightness of the transfer function at all transition points. It can also be stated as the difference between the actual output value for the input code and the ideal output value of the transfer curve at that input code [26].

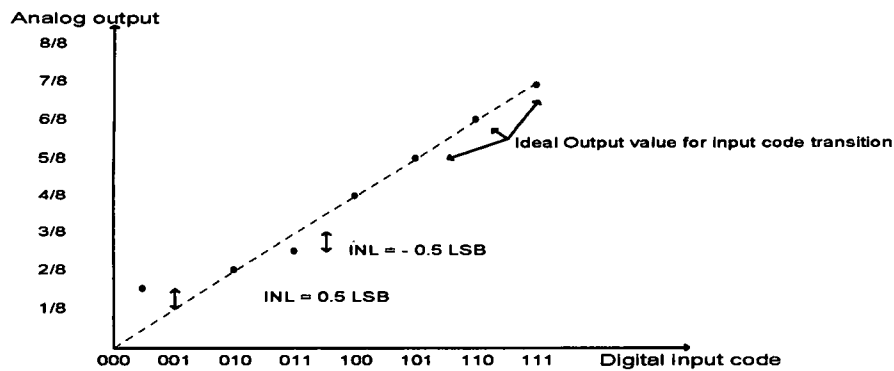


Figure B.3 INL for a 3-bit DAC.

B.5 Signal-to-noise Ratio (SNR)

It is the ratio of the fundamental signal amplitude to the root mean square (RMS) noise spectrum. The noise spectrum includes spectral components within the signal bandwidth without the dc component, the fundamental signal and the harmonics.

B.6 Signal-to-noise and Distortion (SINAD)/ (SNDR)

It is a combination of the SNR and THD specifications. It is defined as the fundamental value of the output signal to the RMS value of all the spectral components within the signal bandwidth, including harmonics excluding dc and fundamental.

B.7 Effective Number of Bits (ENOB)

ENOB shows the ADCs performance at a particular input frequency. ENOB is a function of the input frequency. As input frequency increases ENOB decreases as all the noises are increased.

$$\text{ENOB} = (\text{SNR} - 1.76) / 6.02$$

Appendix C Matlab Algorithms and Output Spectra

C.1 Data or Input Signal

```
len = 4096;  
A = 0.9; % amplitude  
% initialization;  
h = 1:len;  
fs = 80e6;  
t = (h-1)/fs;  
f = 156.25e3; % signal frequency  
w1 = (2*pi*f);  
x = A*sin(w1*t);
```

C.2 Second Order Feed-forward Modulator

```
function [y1,e] = second_order_modulator(x);
```

```
% Parameter initialization  
a1 = 0.67; a2 = 0.17;  
b1 = 1;  
c1 = 0.375;  
c2 = 0.333;  
c4 = 0.28;  
c5 = 1;
```

```
len = length(x);  
% allocate space for arrays  
y1 = zeros (size(x));  
o1 = y1;  
o2 = y1;  
q = y1;  
e = y1;
```

```
%Initialization of the first sample
```

```
y1(1) = 0;  
o1(1) = 0;  
o2(1) = 0;  
q(1) = 0;  
e(1) = 0;
```

```
%Second order modulator
```

```
for i = 2:len,
```

```
    o1(i) = o1(i-1) + c1*( x(i-1) - y1(i-1));  
    o2(i) = o2(i-1) + c2* o1(i);  
    q(i) = a1*o1(i) + a2*o2(i);
```

```
    % 1-bit quantizer
```

```
    if q(i) >= 0
```

```
        y1(i) = 1.25;
```

```
    else
```

```
        y1(i) = -1.25;
```

```
    end
```

```
    % quantized error
```

```
    e(i) = c5*o2(i) - c4*y1(i);
```

```
end
```

C.3 First Order Multi-bit Modulator

```
function [y2] = first_order_modulator(e);
```

```
b2 = 1;
```

```
c3 = 1;
```

```
len = length(e);
```

```
%Initialization of first sample;
```

```
o3(1) = 0;
```

```
y2(1) = 0;
```

```
e(1) = 0;
```

```
%First order modulator
```

```
for i = 2:len,
```

```

o3(i) = c3 *o3(i-1) + b2*( e(i-1) - y2(i-1));

if ( o3(i) > 0.8928)
    y2(i) = 1.25;

elseif (o3(i) > 0.5357)
    y2(i) = 0.8928;

elseif (o3(i) > 0.1785)
    y2(i) = 0.5357;

elseif ( o3(i) > -0.1785)
    y2(i) = 0.1785;

elseif ( o3(i) > -0.5357)
    y2(i) = -0.1785;

elseif (o3(i) > -0.8928)
    y2(i) = -0.5357;

elseif ( o3(i) > -1)
    y2(i) = -0.8928;

else
    y2(i) = -1.25;

end
end

```

C.4 Digital_error_correction

```

function[y] = digital_error_correction(y2,y1);

for u = 2:length(y2),
    corr(u) = 4*y2(u) - 4*y1(u-1);
    diff1(u) = (corr(u) - corr(u-1));
    diff2(u) = diff1(u) - diff1(u-1);
    y(u) = diff2(u)+ 6*y1(u-1);
end

```

C.5 Signal processing

```
function [SINAD, SNR, ENOB, SFDR] = signalprocessing(y);
fs = 80e6;
FFF = fft(y);
len = length(y);
hertz = (1:len)*(fs/len);

%Compute the power by squaring the FFT
pwr = FFF.*conj(FFF);
%Zero out DC bin and find power for the signal bandwidth
pwr(1) = 0; % power of DC = 0
hertz(1) = 0;
FFF(1) = 0.000001; % fft of DC = 0
g = find(hertz >= 1.25e6); % Covers entire signal bandwidth
span = g(1);
bandwidthpower = abs(s(1:span));
fundamentalfreq = find(bandwidthpower >= max(bandwidthpower));

%Store power of fundamental frequency in As bin in dB
signalpower = 10*log10(pwr(fundamentalfreq));

% To find noise and distortion clear out the fundamental frequency
bandwidthpower(fundamentalfreq)= 0;

%To find signal to noise and distortion ratio we need noise power represented by all
noisy components including harmonics
totalnoise_distortion = sqrt(sum((bandwidthpower))/span);

% To find noise for SNR we clear out all the harmonics
for i = 2:1:round(span/fundamentalfreq);
freqmax(fundfreq*i - (i-1)) = 0;
end
noisepower = 10*log10(bandwidthpower(2:span)); %Computing power of noise bins

maxnoise_comp = max(noisepower); %Highest spurious component in bandwidth

totalnoise = sqrt(sum((bandwidthpower))/span); %Computing square root of the average
power of total noise generated by modulator or RMS noise

signal_to_noise = (pwr(fundamentalfreq))/(totalnoise); %Signal power to sum of noise
power

signal_to_noise_and_distortion = (pwr(fundamentalfreq))/(totalnoise_distortion); %
Signal power to sum of noise power and harmonics
```

% Dynamic performance of the proposed Delta Sigma modulator

SFDR = signalpower - maxnoise_comp;

SINAD = 10*log10(signal_to_noise_and_distortion);

SNR = 10*log10(signal_to_noise);

ENOB = (SNR-1.76)/6.02;

C.6 Output Spectra

The data spectrum is shown in Figure C.1. The FFT spectrum of second order modulator is shown in Figure C.2. The first order modulator, whose FFT spectrum is shown in Figure C.3. The power spectrum of the cascaded modulator is shown by Figure C.4.

Spectrum for second order modulator

```
F1 = fft(y1);  
F1log = (20*log10((abs(F1)/len)));  
hertz = (1:len)*(fs/len);  
figure  
plot(hertz,F1log);  
axis([0 5e6 -140 0]);  
ylabel('Magnitude in dB');  
xlabel('Frequency');  
title('Frequency Spectrum of SECOND order modulator in Hz');  
grid
```

Spectrum of First order modulator output

```
F2 = fft(y2);  
F2log = (20*log10((abs(F2)/len)));  
hertz = (1:len)*(fs/len);  
figure  
plot(hertz,F2log);  
axis([0 5e6 -140 0]);  
ylabel('Magnitude in dB');  
xlabel('Frequency');  
title('Frequency Spectrum of FIRST order modulator in Hz');
```

```
grid;
```

Spectrum for digital correction

```
FF = fft(y);  
FFlog = (20*log10((abs(FF)/len)));  
hertz = (1:len)*(fs/len);
```

```
figure
```

```
plot(hertz,FFlog);  
axis([0 2e6 -140 0]);  
ylabel('Magnitude in dB');  
xlabel('Frequency');  
title('Output Spectrum of digital error correction logic signal in Hz');  
grid;
```

Spectrum for SINAD

```
function [final] = spectrum_SINAD(y);  
FFF = fft(0.166*y); %For proper representation we scale y.  
fs = 80e6;  
pwr = FFF.*conj(FFF);  
len = length(y);  
hertz = (1:len)*(fs/len);  
%Zero out DC bin and find power for the signal bandwidth  
%Zero out DC bin and find power for the signal bandwidth  
pwr(1) = 0; % power of DC = 0  
hertz(1) = 0;  
FFF(1) = 0.000001; % fft of DC = 0  
spanfreq = find(hertz >= 1.25e6);  
span = spanfreq(1); %Covers entire signal bandwidth  
bandwidthpower = abs(pwr(1:span));  
SINAD = (10*log10((pwr)/(len * len)));  
figure  
plot(hertz,SINAD);  
axis([0 5e6 -140 5]);  
ylabel('Magnitude in dB');  
xlabel('Frequency');  
title('Frequency Spectrum of Signal to noise plus distortion');  
grid;
```

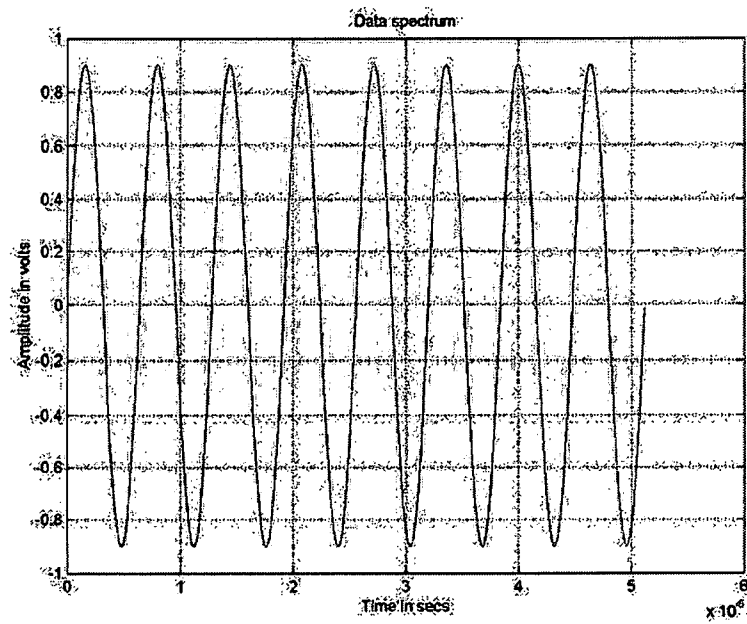


Figure C.1 Data spectrum.

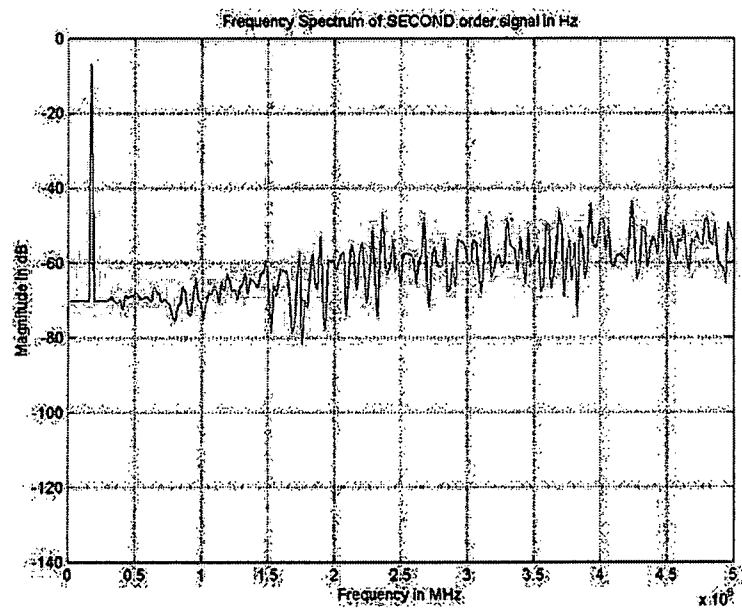


Figure C.2 FFT spectrum of second order modulator.

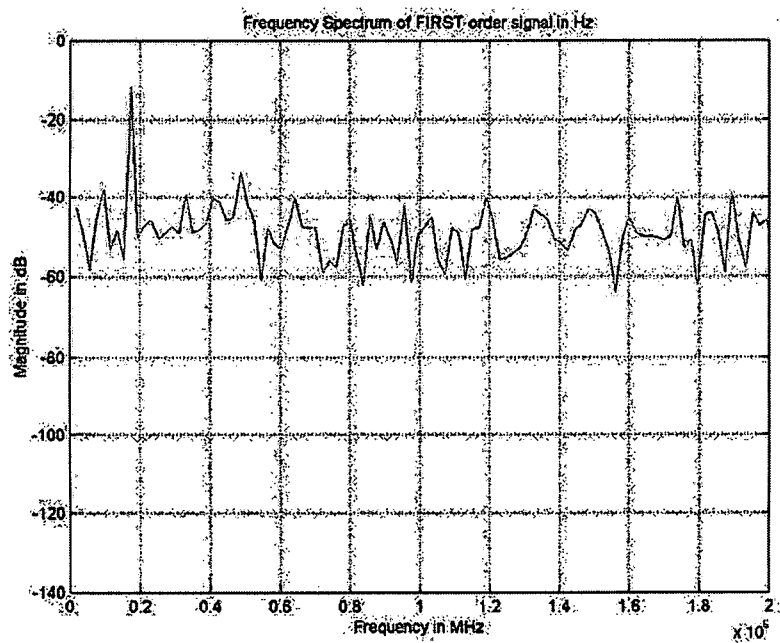


Figure C.3 FFT spectrum of first order modulator.

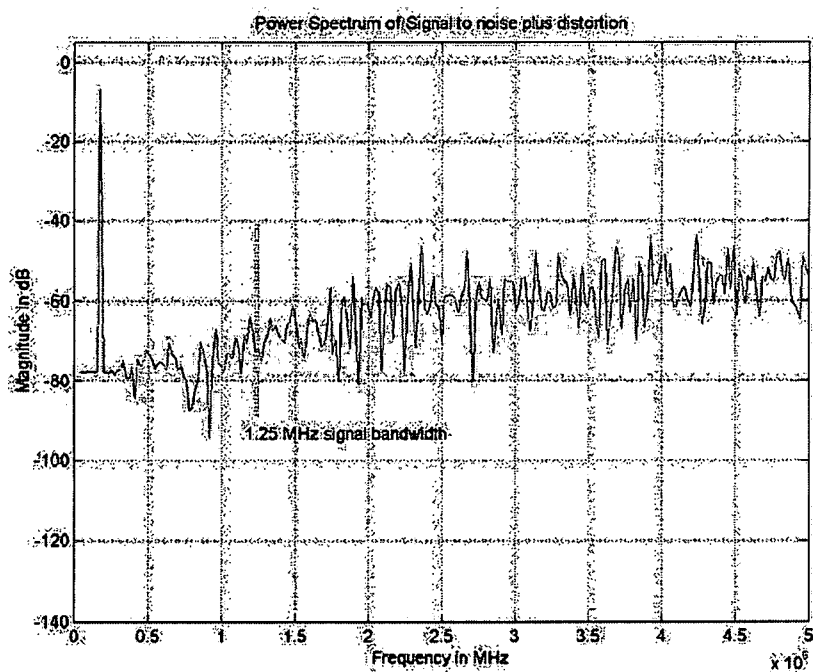


Figure C.4 Power spectrum of signal to noise plus distortion.

Appendix D Layouts

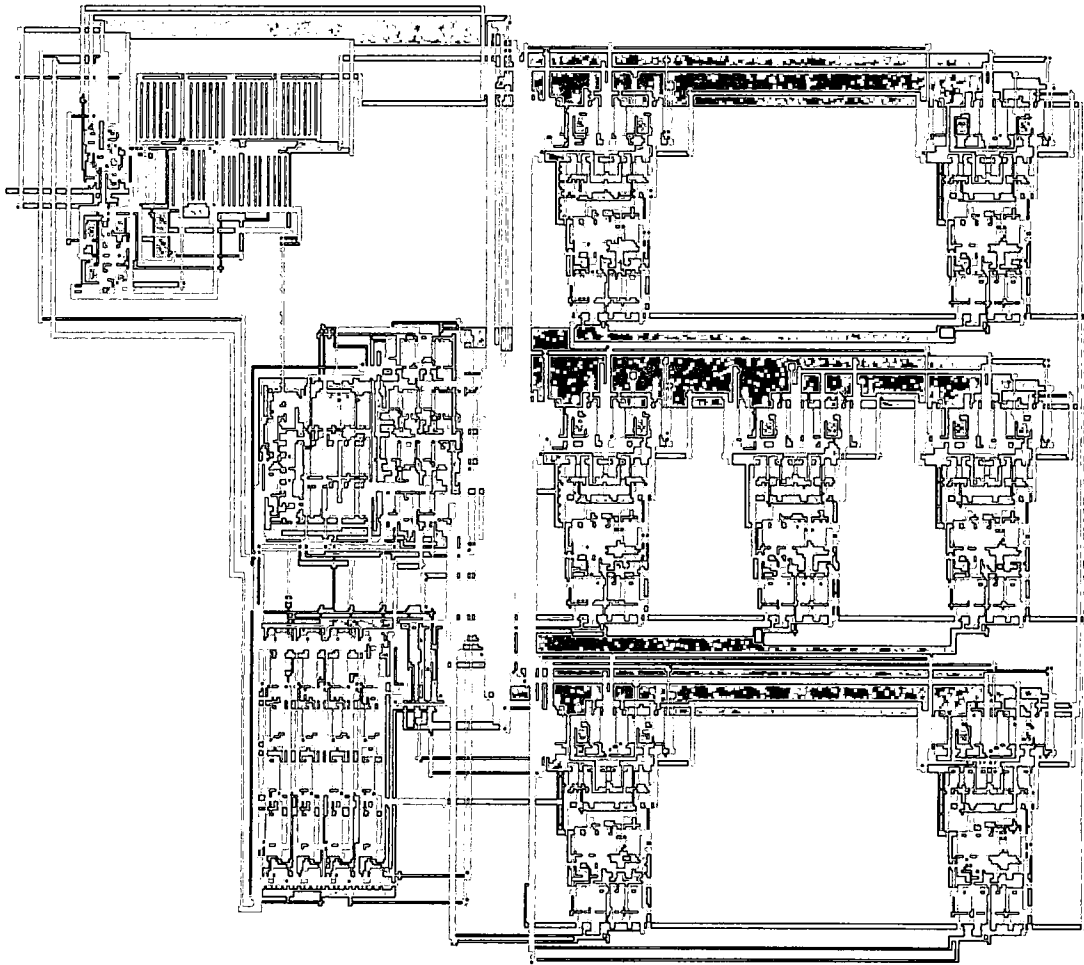


Figure D.1 Multi-bit first order delta sigma modulator.

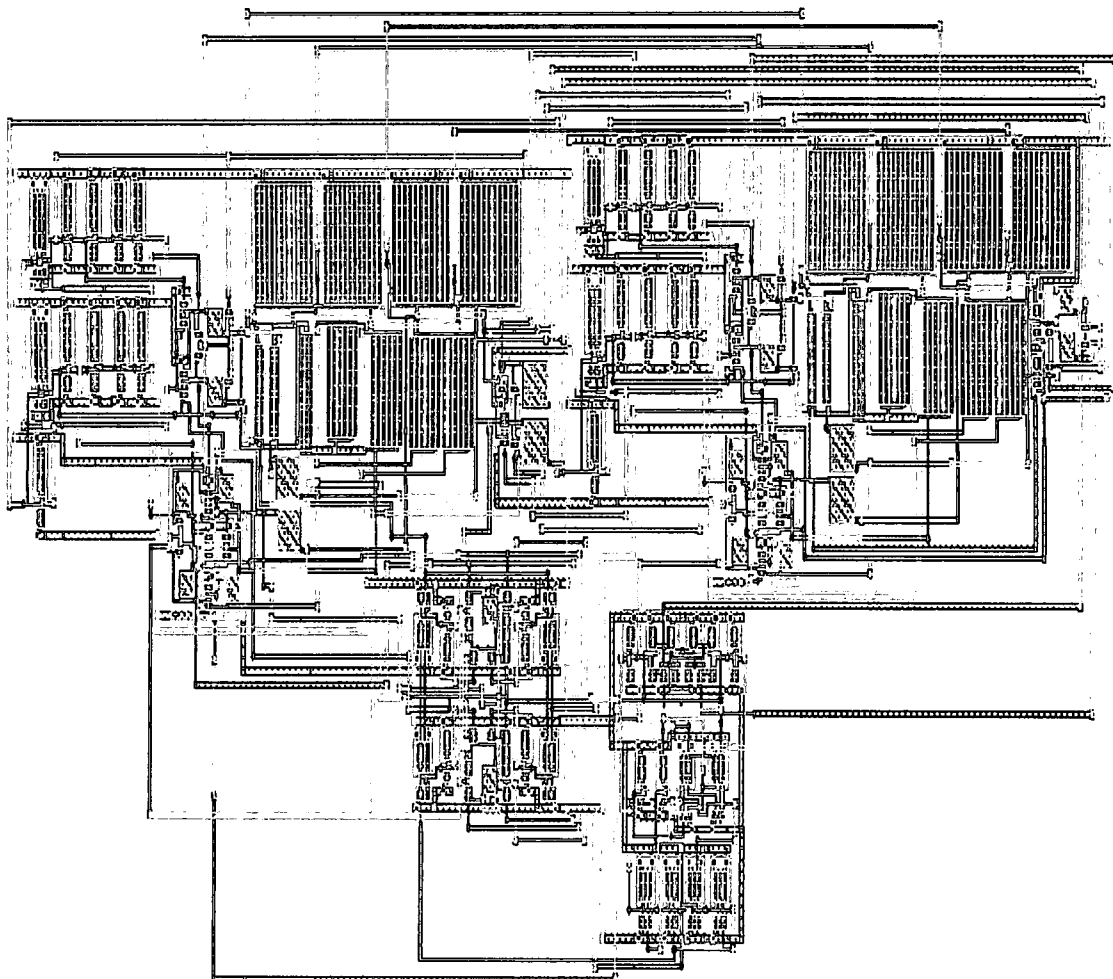


Figure D.2 Feed-forward second order modulator.

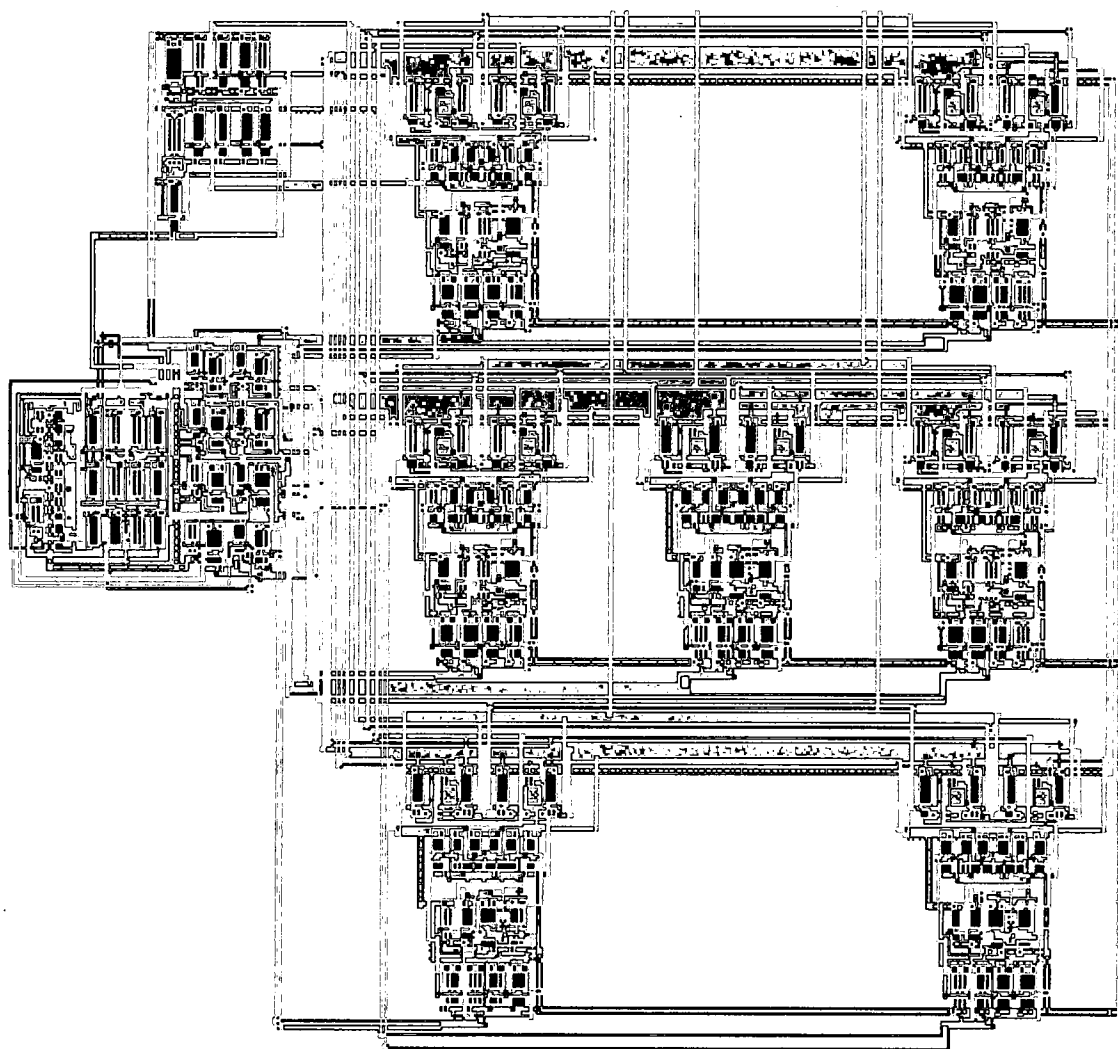


Figure D.3 A 3-bit ADC and thermometer-to-binary encoder.

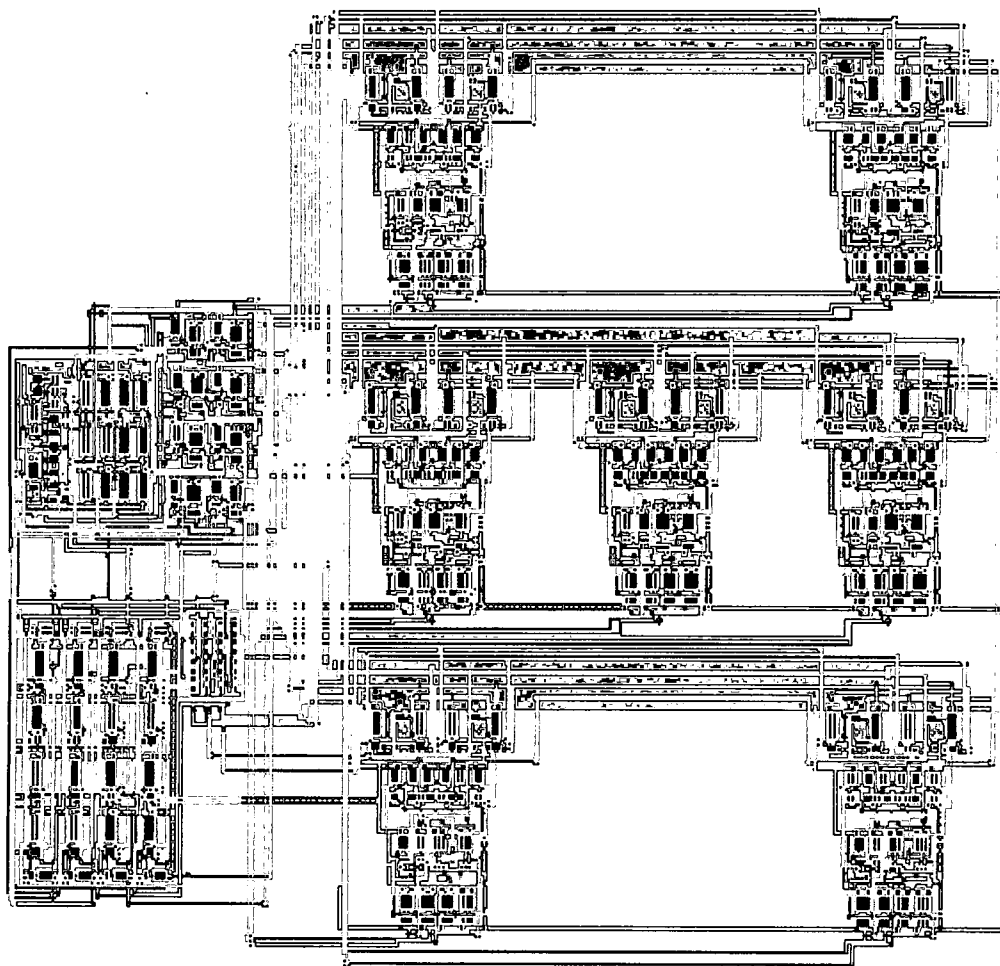


Figure D.4 A 3-bit ADC, thermometer-to-binary encoder and DAC.

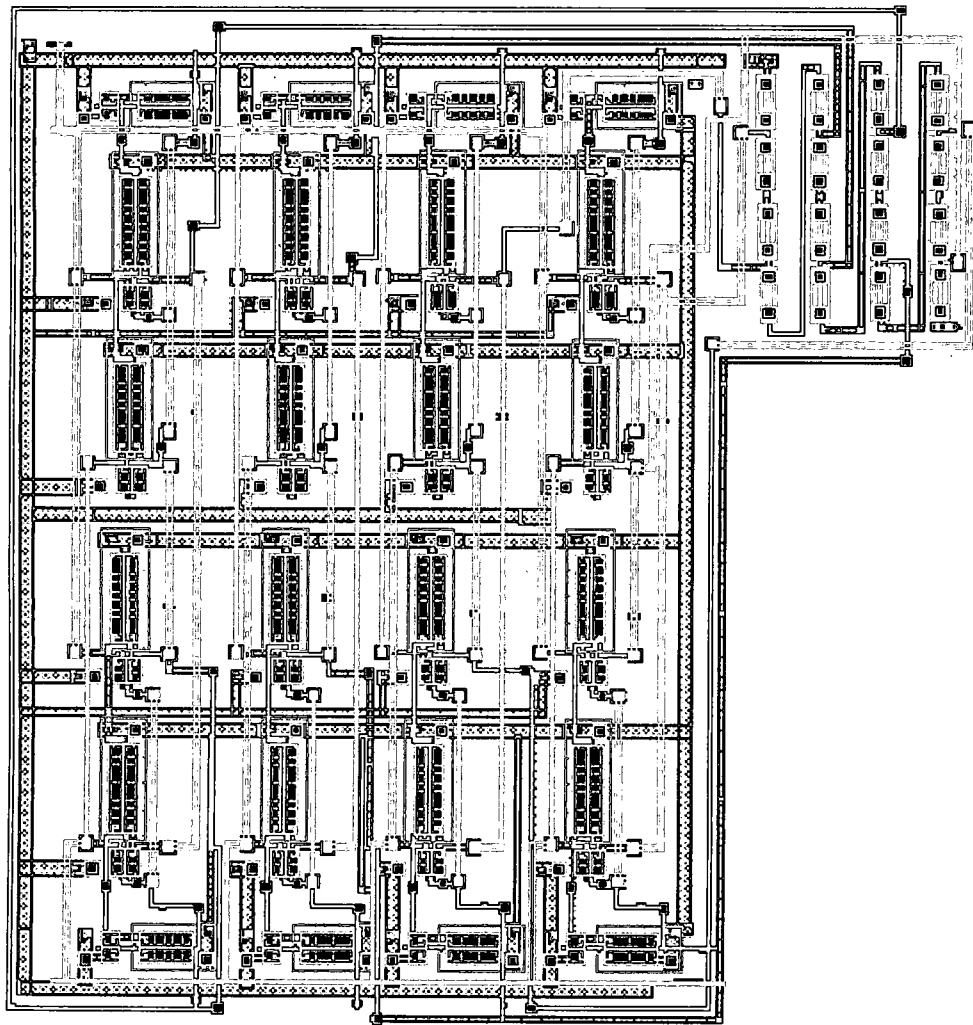


Figure D.5 A 3bit DAC.

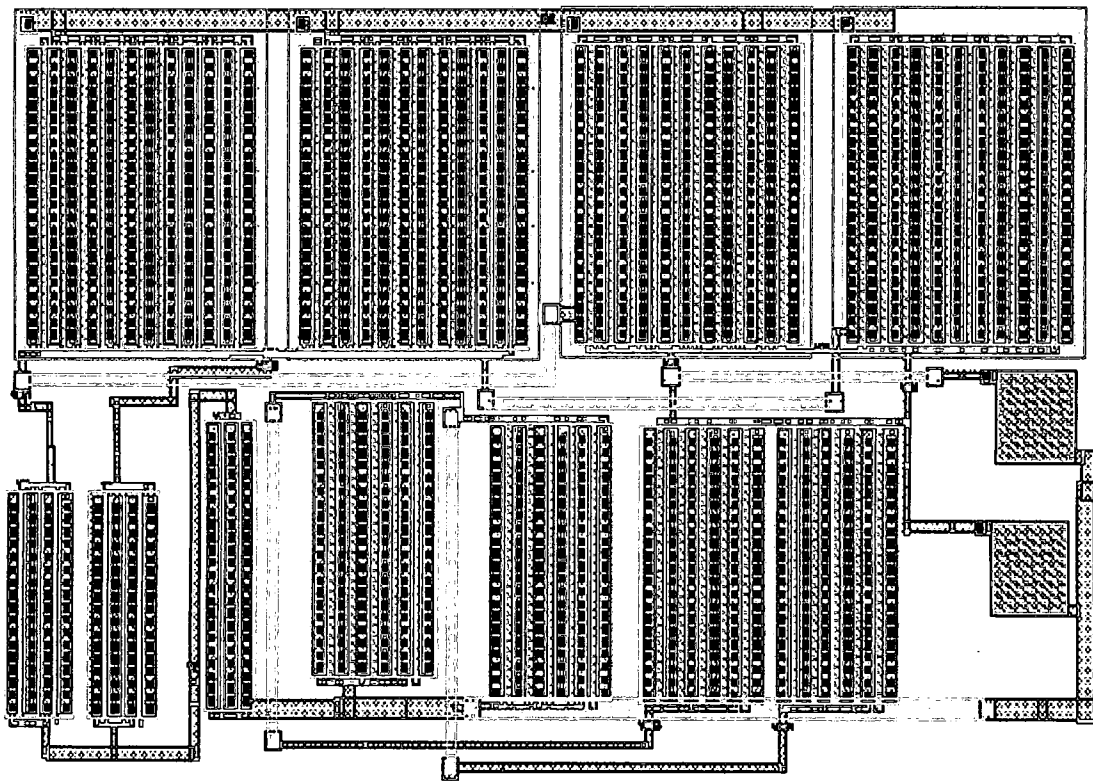


Figure D.6 First stage op-amp.

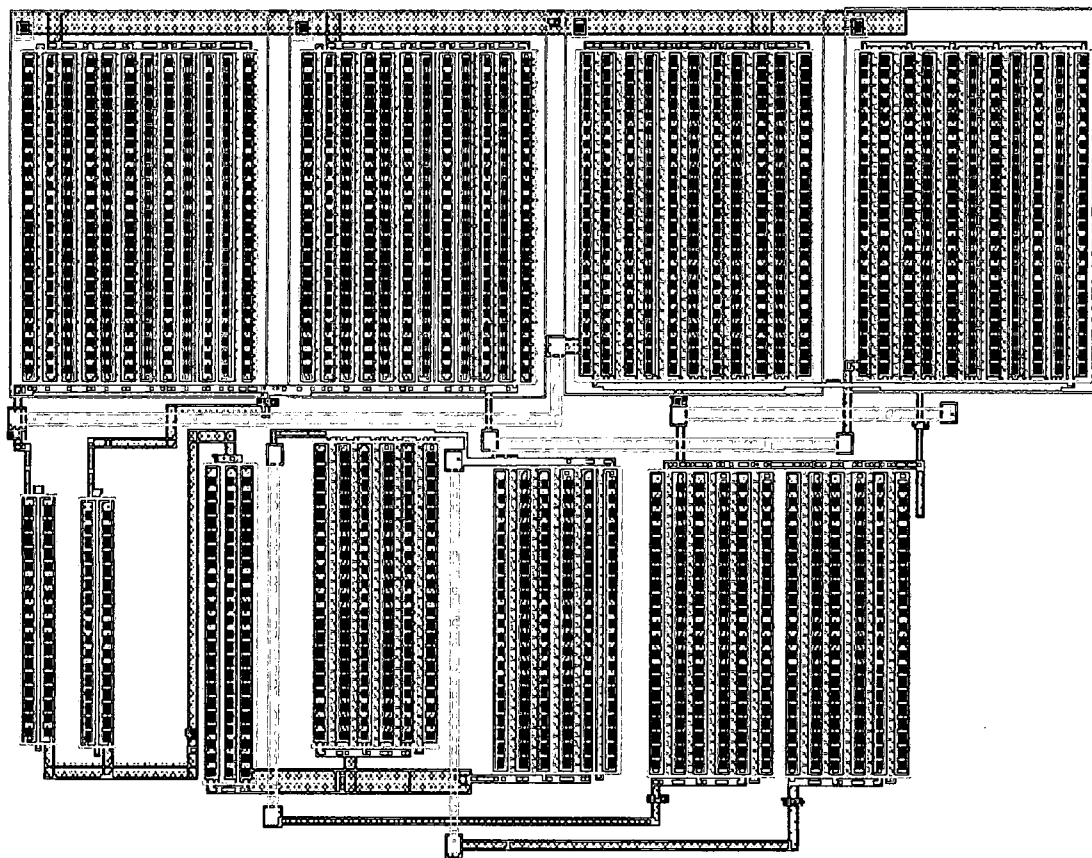


Figure D.7 Second and third stage op-amp.

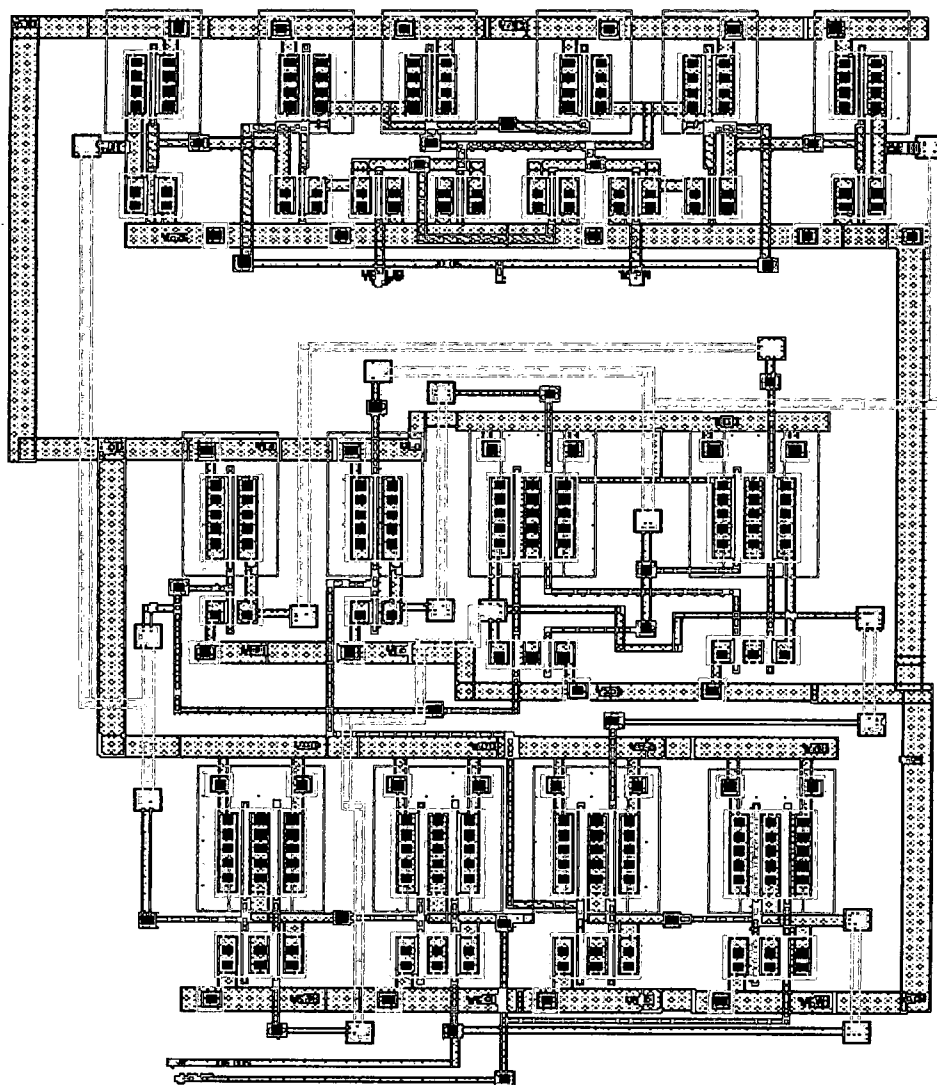


Figure D.8 Comparator.

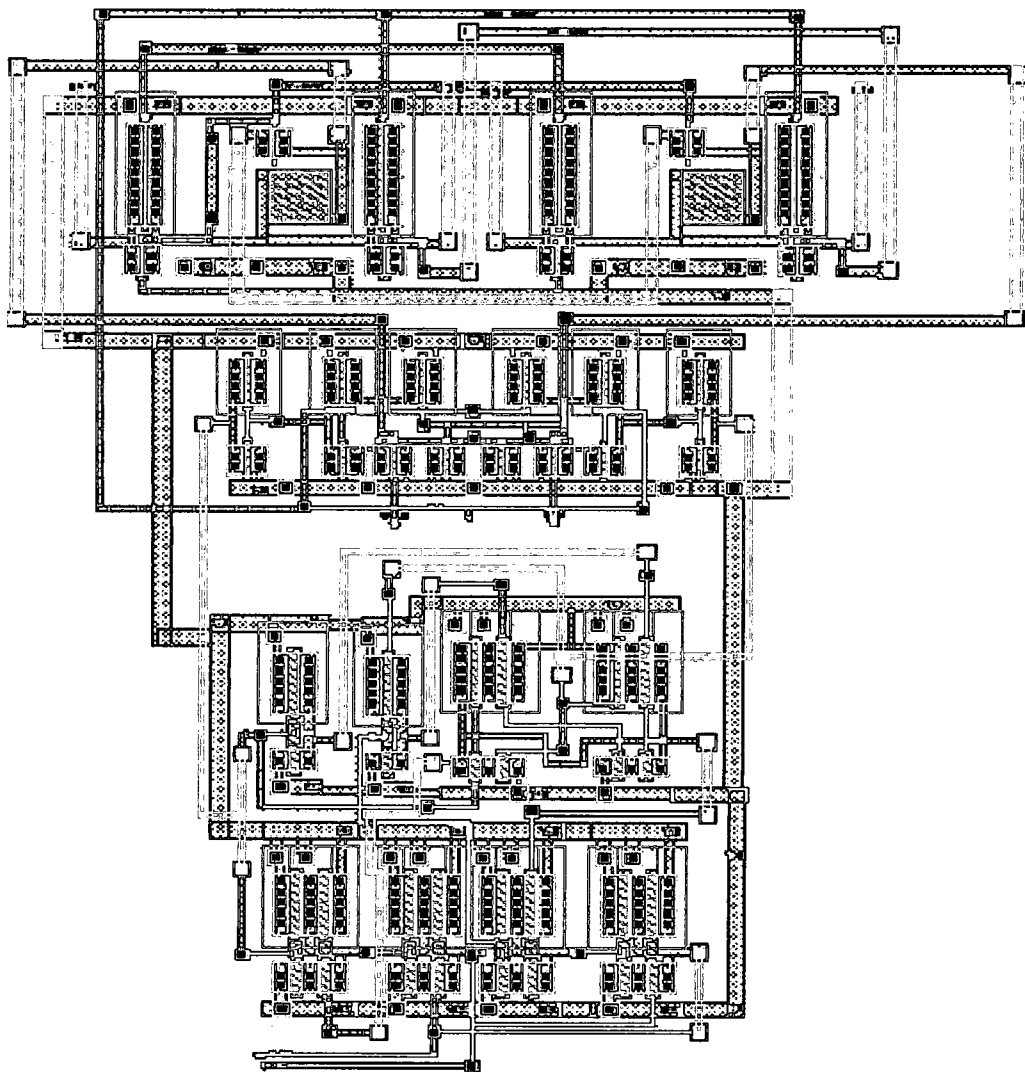


Figure D.9 Comparator with pass-gates.

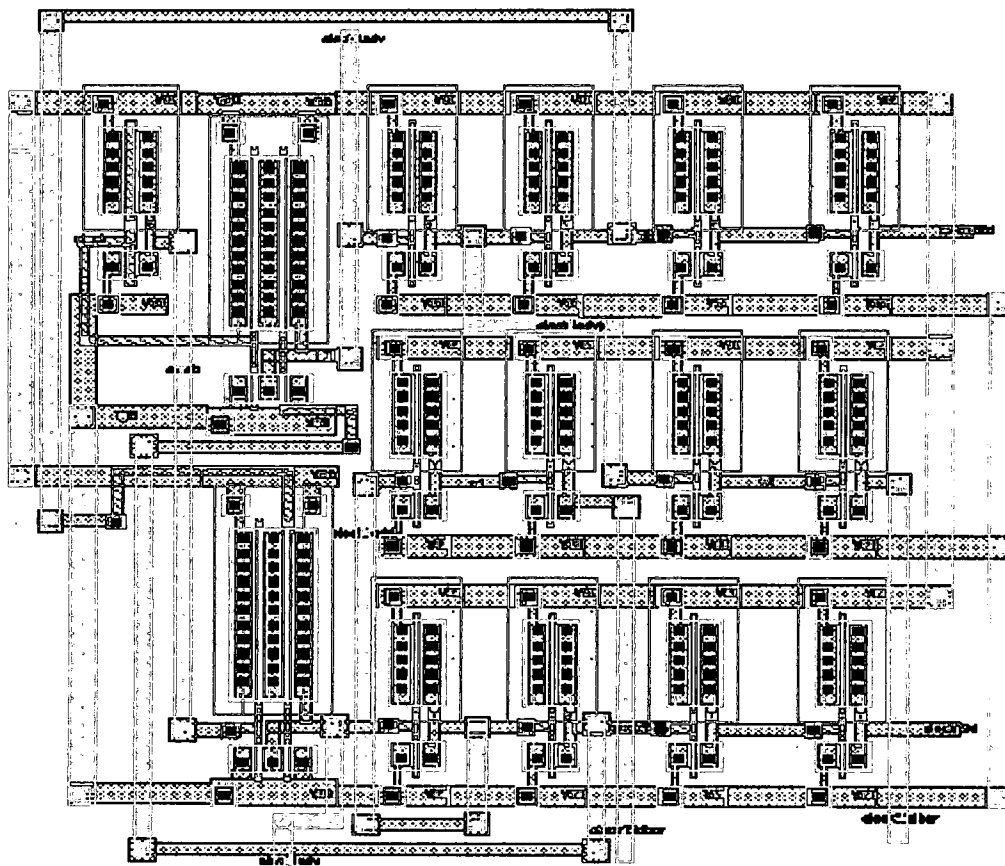


Figure D.10 Non-overlapping clocks.

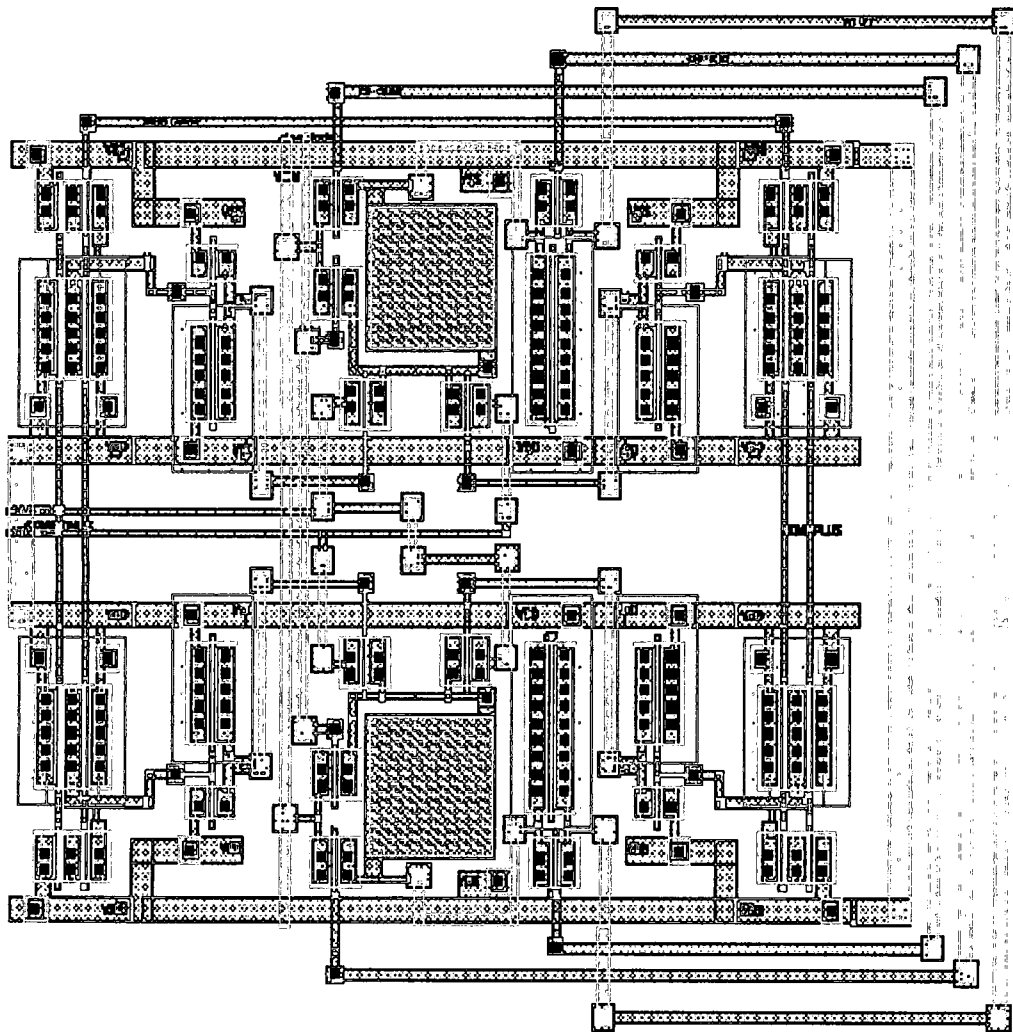


Figure D.11 Commercially implemented 1-bit DAC.

Appendix E Matlab Functions

E.1 Matlab Code for Finite DC Gain, Finite Slew-rate and Finite Gain bandwidth

```
len = 4096;
A = 0.9; %Amplitude
% Initialization;
h = 1:len;
fs = 80e6;
t = (h-1)/fs;
f = 156.25e3; %Signal frequency
w1 = (2*pi*f);
inp2 = zeros(1,4096);
inp1 = A*sin(w1*t) + 1.25;
A0 = 750;
inp = inp1(1:128); % for testing slew-rate
figure;
plot(inp);

% Actual parasitic and input/output capacitances
Cs = 75e-15;
Cpi = 2e-15;
Ci = 200e-15;
Cl = 200e-15;
Ceq = 500e-15; % output capacitance and load capacitance

% The transconductance of the input transistors of the op-amp

k = 132e-06; %NMOS input transistors
WLratio = (16e-06)/(0.18e-06);
Vgs = 0.56;
Vt = 0.36;
Id = 250e-06;
gm = k*WLratio*(Vgs - Vt);
gml = sqrt(2*Id*k*WLratio);
```

```

%Finite OTA gain due to close loop pole and gain errors

%Sampling phase
% Capacitive feedback factors
fdc1 = 1;
fdc1 = Ci/(Ci+Cpi); %When parasitics included
p1 = (A0*fdc1)/(1+A0*fdc1); % Pole and gain errors

% During integration
% Capacitive feedback factors
fdc2 = Ci/(Ci+Cs);
fdc2 = Ci/(Ci+Cpi+Cl); % When parasitics included
p2 = (A0*fdc2)/(1+A0*fdc2); % Pole and gain errors

% Finite Slew rate and finite gain-bandwidth

alpha = max(p1,p2); %gain error
srate = Id/Ceq; % Slew rate
GBW = gm/(Ceq*2*pi); % gain bandwidth
Ts = 12.5e-09;
tau=1/(2*pi*GBW);
Tmax = Ts/2;
outputslope = alpha.*abs(inp)/tau; %Actual output slope
t0 = (max(abs(inp))*alpha/srate) - tau; %Slewing time

if outputslope > srate

% Op-amp in slewing mode when output's slope exceeds the Slew-rate and the op-
amp first enters linear region and then saturation region

if t0 >= Tmax % if the time required to settle is greater than tmax = ts/2 then slewing

error = abs(inp) - srate*Tmax;

else
% first part is linear with slope SR = slewrate and hence v = dvo/dt*dt

texp = Tmax - t0; % Partial slew
error = abs(inp)*(1-alpha) + (alpha.*abs(inp) - srate*t0) * exp(-texp/tau);
end
else
% Op-amp in linear region and the output settles in an exponential fashion - no
slewing perfect output
texp = Tmax;
error = abs(inp)*(1-alpha) + alpha*abs(inp) * exp(-texp/tau);
end

```

```

out = inp - sign(inp).*error;

% Modeling settling time error during integration phase
Ceq = Cs + Cpi + (Cs + Cpi + Ci)*Cl/(Ci); % Total capacitance at output
delta = exp((-gm * t0)/(p2 * Ceq)); % Settling time error

% Finite dc gain vs noise power[41]
M = 32; % over-sampling ratio
del = 2.5; % LSB in second order single-bit modulator
g1 = 0.375;
g2 = 0.333;
pi = 3.14159;
AvdB = [10 20 30 40 50 60 70 80 90 100];
Pa = (del^2/12)*(g1+g2)^2 *(pi)^2./(M).^3*1./(AvdB).^2; % noise power
PadB = 10*log10(Pa);
figure;
plot(AvdB,-abs(PadB));
title('Gain of op-amp vs Noise power')
xlabel('Gain in dB');
ylabel('Baseband noise power');
grid;

```

E.2 Matlab Algorithm for Finding NTF of the Second Order Feed-forward Modulator

```

[B,A] = butter(2,0.155,'high');% cut off frequency chosen to have NTF = 3 dB
B1 = B*(1/0.7077); % normalizing the numerator
h = impz(B1,A); % first coefficient as 1 or impulse response with leading 1
[z,p,k] = tf2zp(B1,A); % check for stability of NTF
[H,F] = freqz(B1,A,512,80e6);
figure
plot(F,abs(H));
grid;
figure
plot(F,20*log10(abs(H)));
grid;

```

E.3 Matlab Function for Calculating Op-amp Noise

```
function [noise, vout] = opampnoise(gm); % includes switch on resistance
k = 1.38e-23;
T= 300;
WLP = 27.77; % width to length ratio of the PMOS 5u/0.18u
WLN = 11.11; % width to length ratio of the NMOS 2u/0.18u
Kp = 50e-06;
Kn = 132e-06;
Vtp = -0.4;
Vtn = 0.36;
VDD = 2.5;
VSS = 0;
Vin = 0.7;
gsw = Kn*WLN*(VDD - Vtn - Vin) + Kp*WLP*(-VSS + Vtp + Vin);
rsw = 1/(gsw); % resistance of the switches
csamp = 75e-15;
fs = 80e6;
Ts = 1.25e-08;
Tt = 0.5*Ts;
noise = (rsw*gm*2*k*T*(Tt)^2)/(fs*csamp*(Ts^2)); % Op-amp noise
vout = Vin * (1 - exp(-Ts/(2*rsw*csamp))); % Output - error
```

Appendix F Simulation Results

F.1 Op-amp Parameters

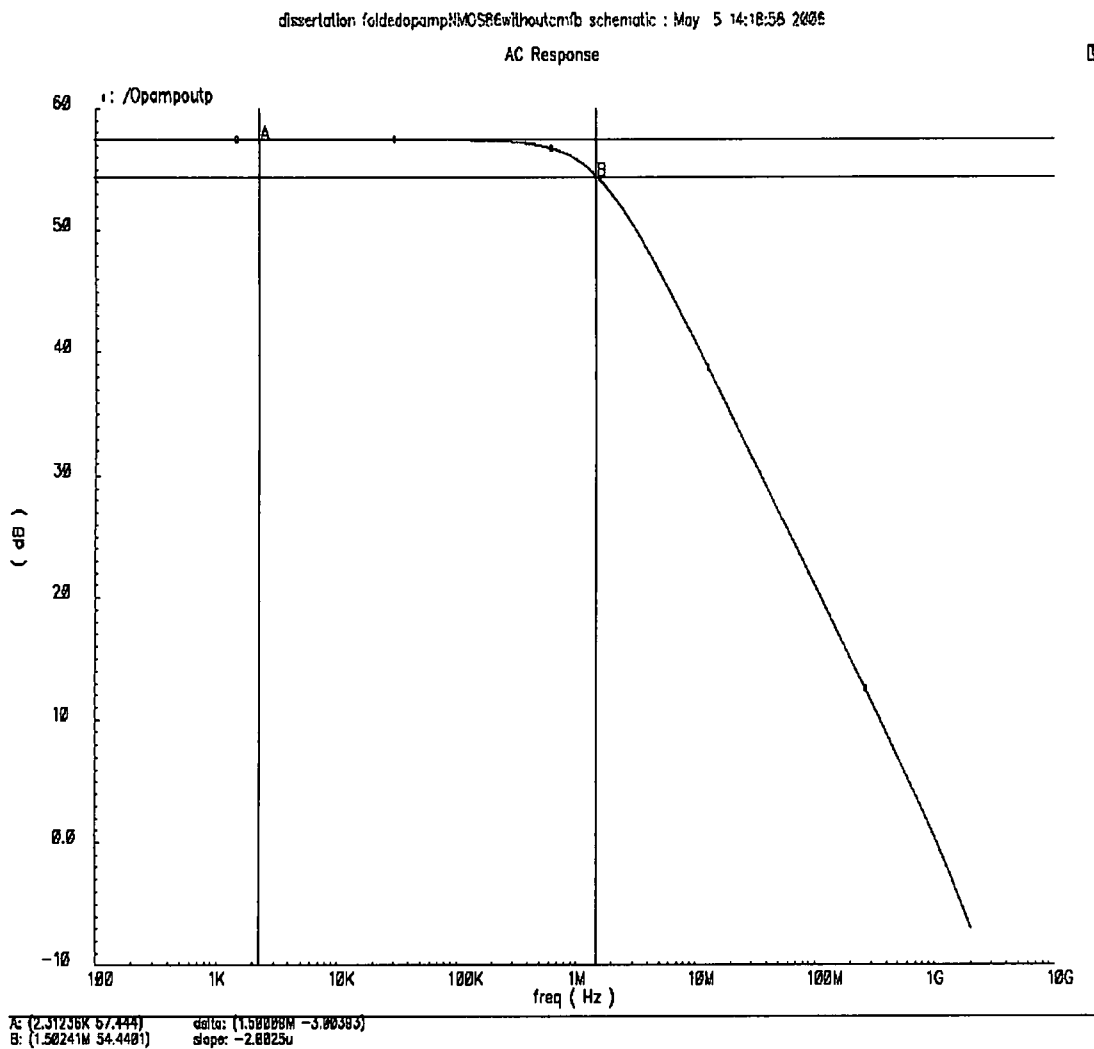


Figure F.1 Folded cascode OTA DC gain.

dissertation foldedopampNMOS6withoutcmfb schematic : SLEWRATE IN OPEN LOOP

Transient Response

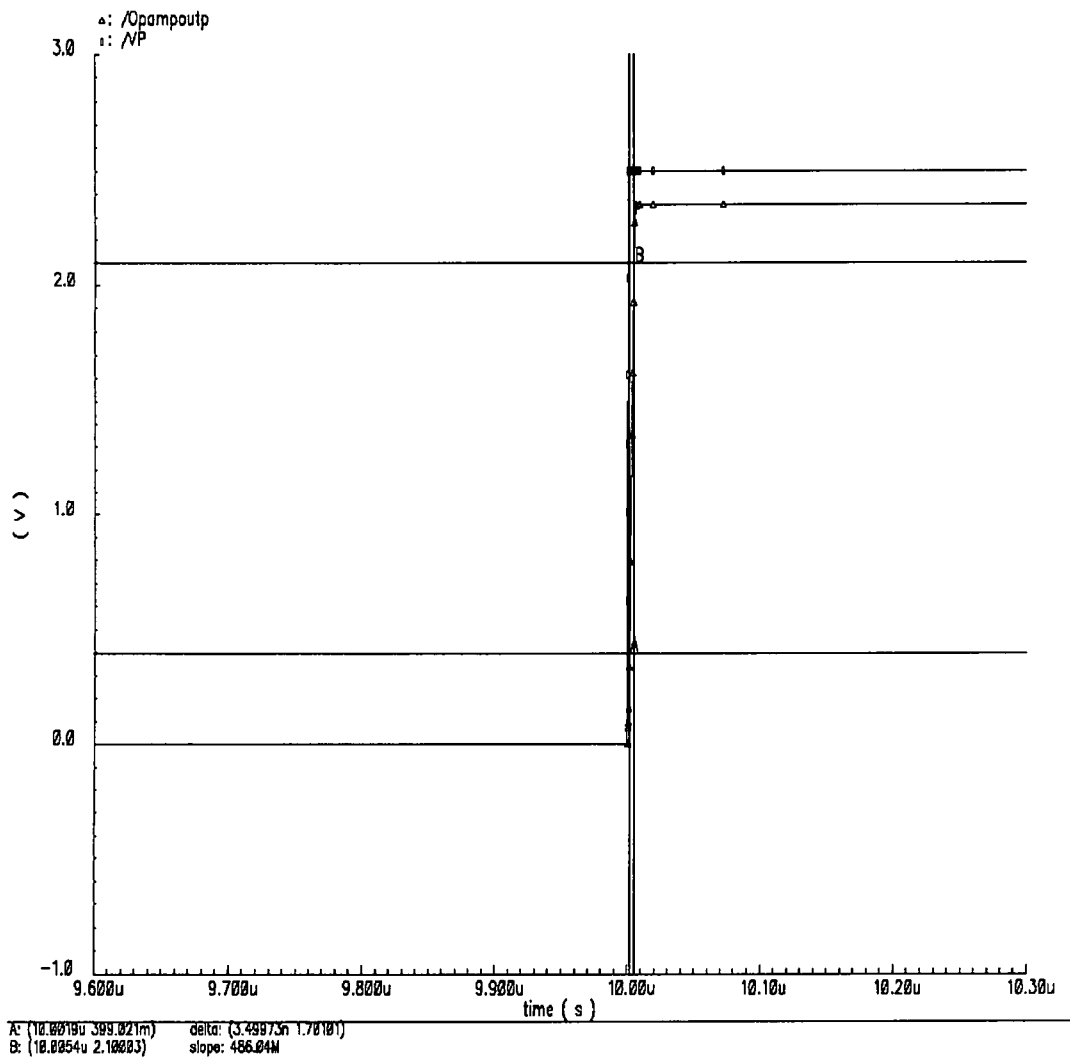


Figure F.2 Slew-rate of folded cascode OTA.

dissertation foldedopampNMOSB6withoutcmfb schematic : VB1,2,3,4 = 1.6544 1.5699 0.628 0.5569 0.55245

DC Response

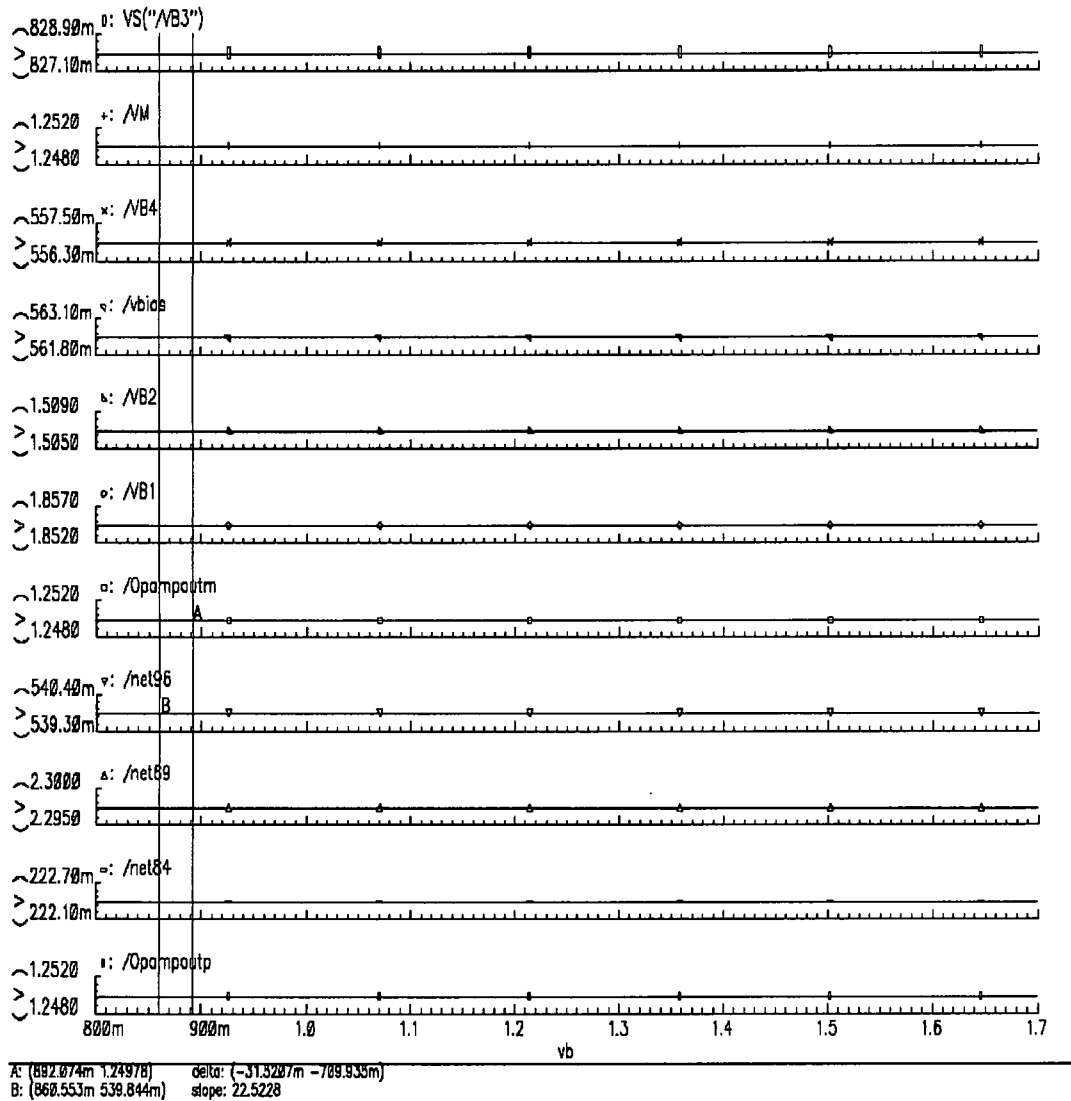


Figure F.3 DC response of the folded cascade OTA.

DC Response

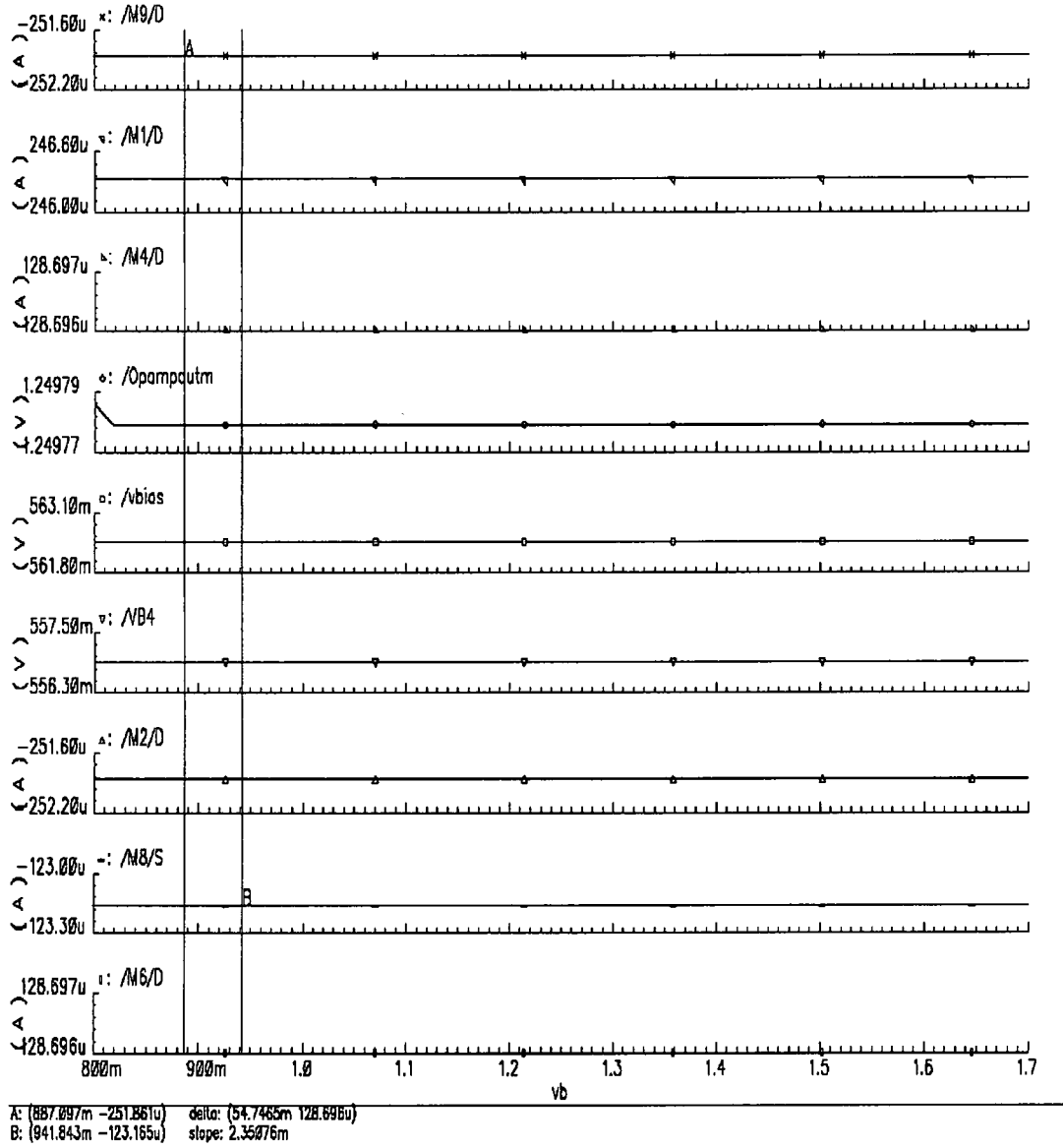


Figure F.4 DC currents in OTA.

PM = 60

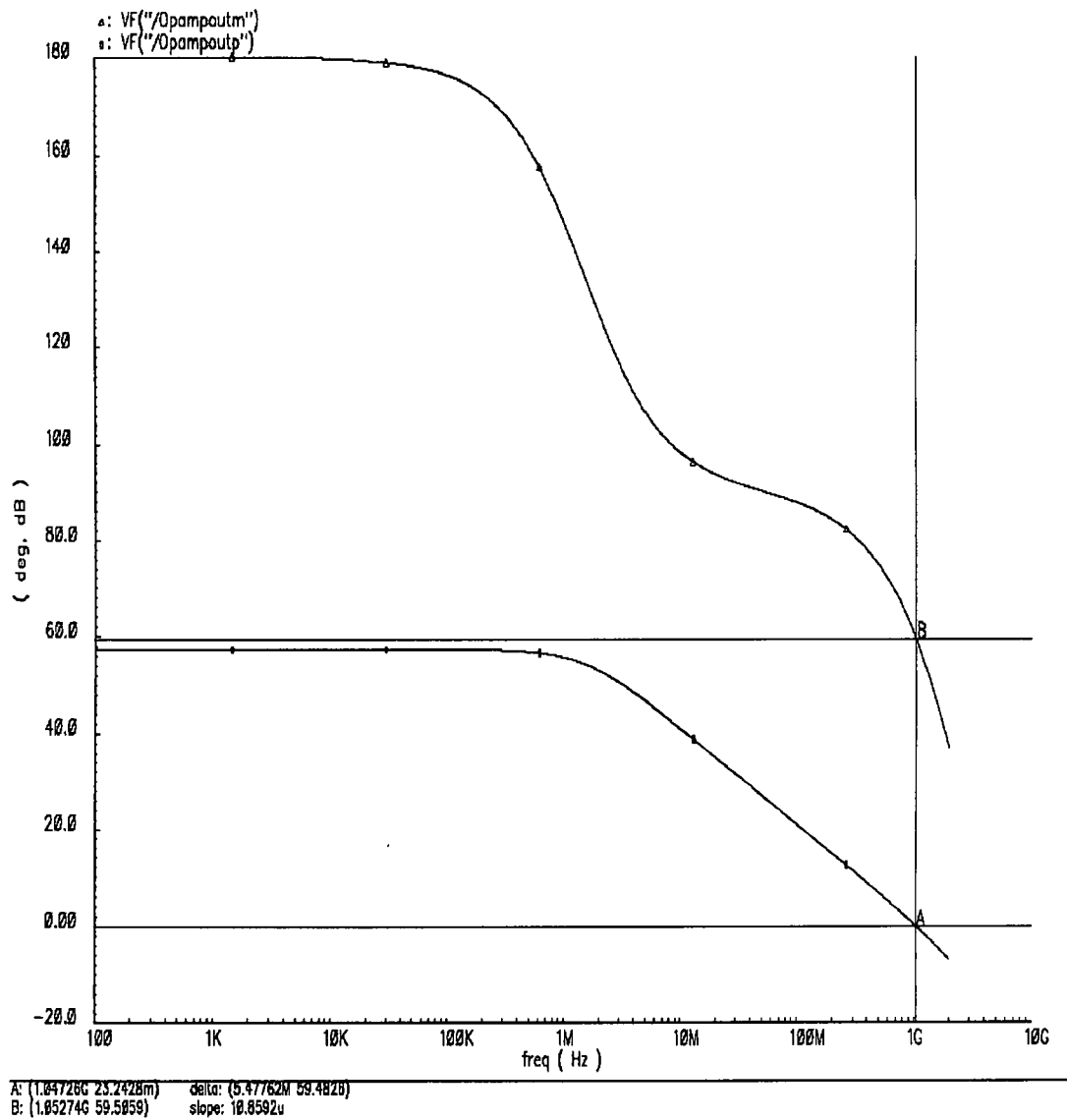


Figure F.5 Unity gain bandwidth and phase margin of the OTA.

dissertation folder\pump\NMOS60withoutcmfb schematic :settling time

Transient Response

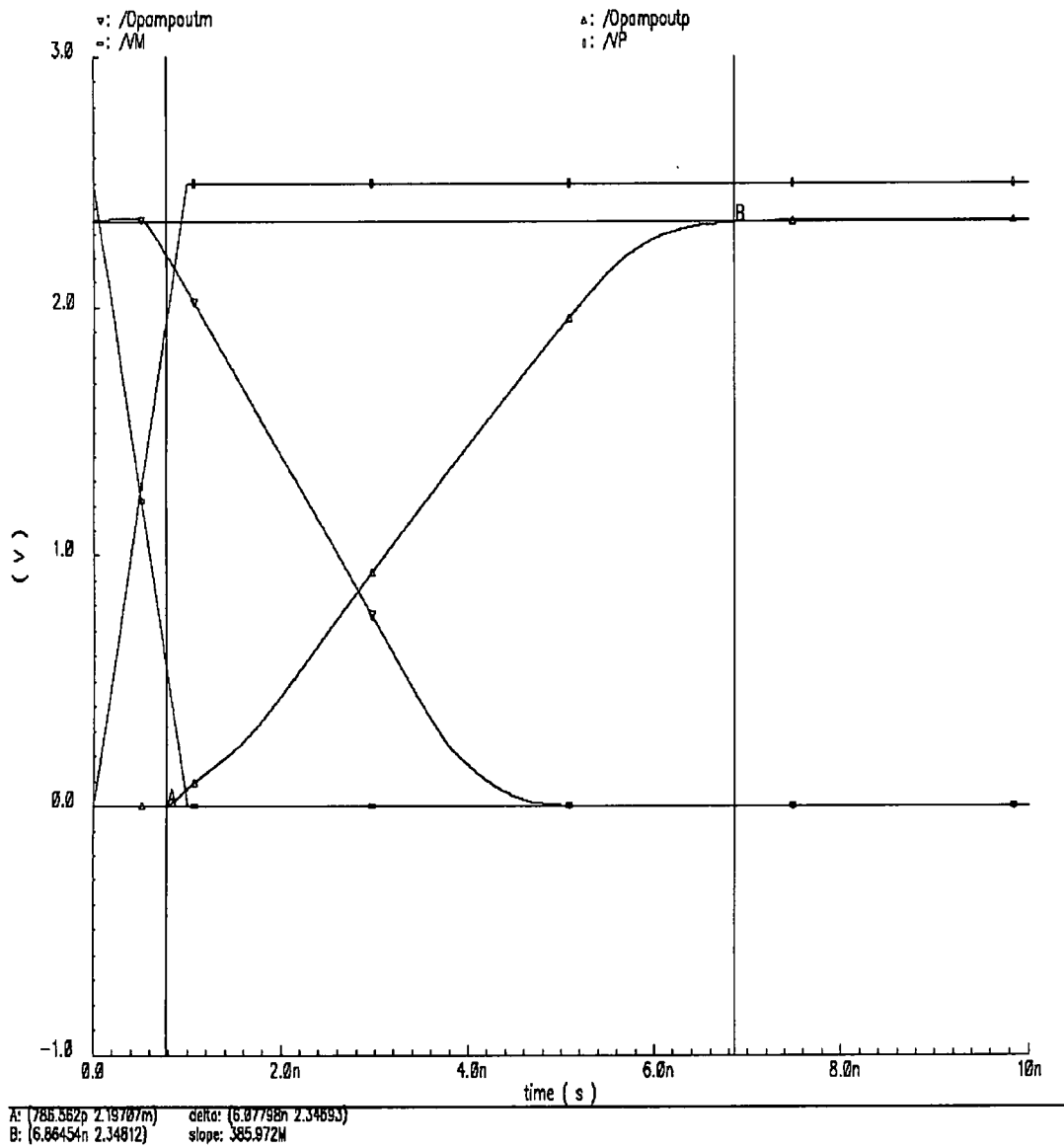


Figure F.6 Settling time (0.1 %) of OTA.

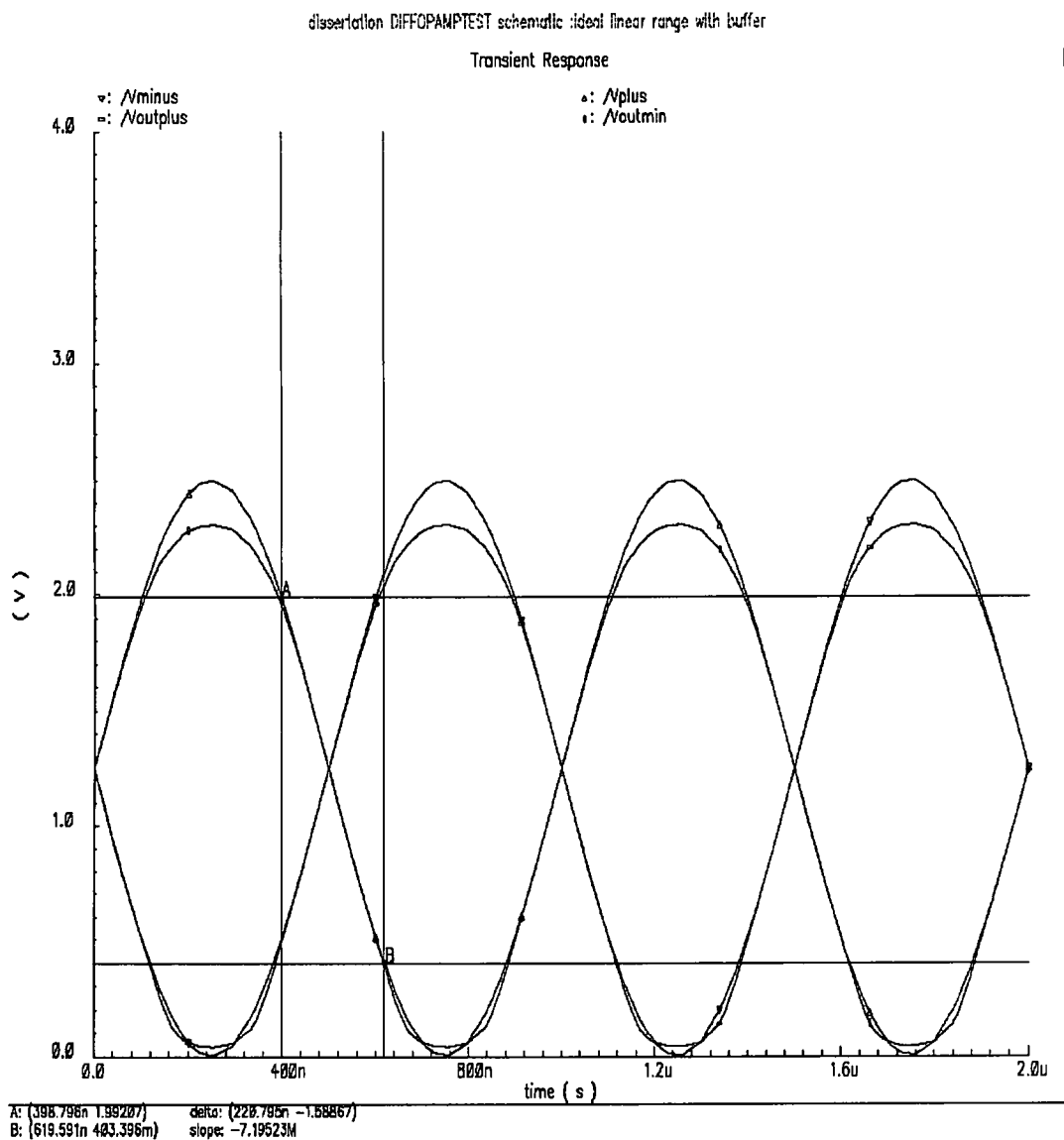


Figure F.7 Linear output swing of the folded cascode OTA.

F.2. Wide Swing Current Mirror

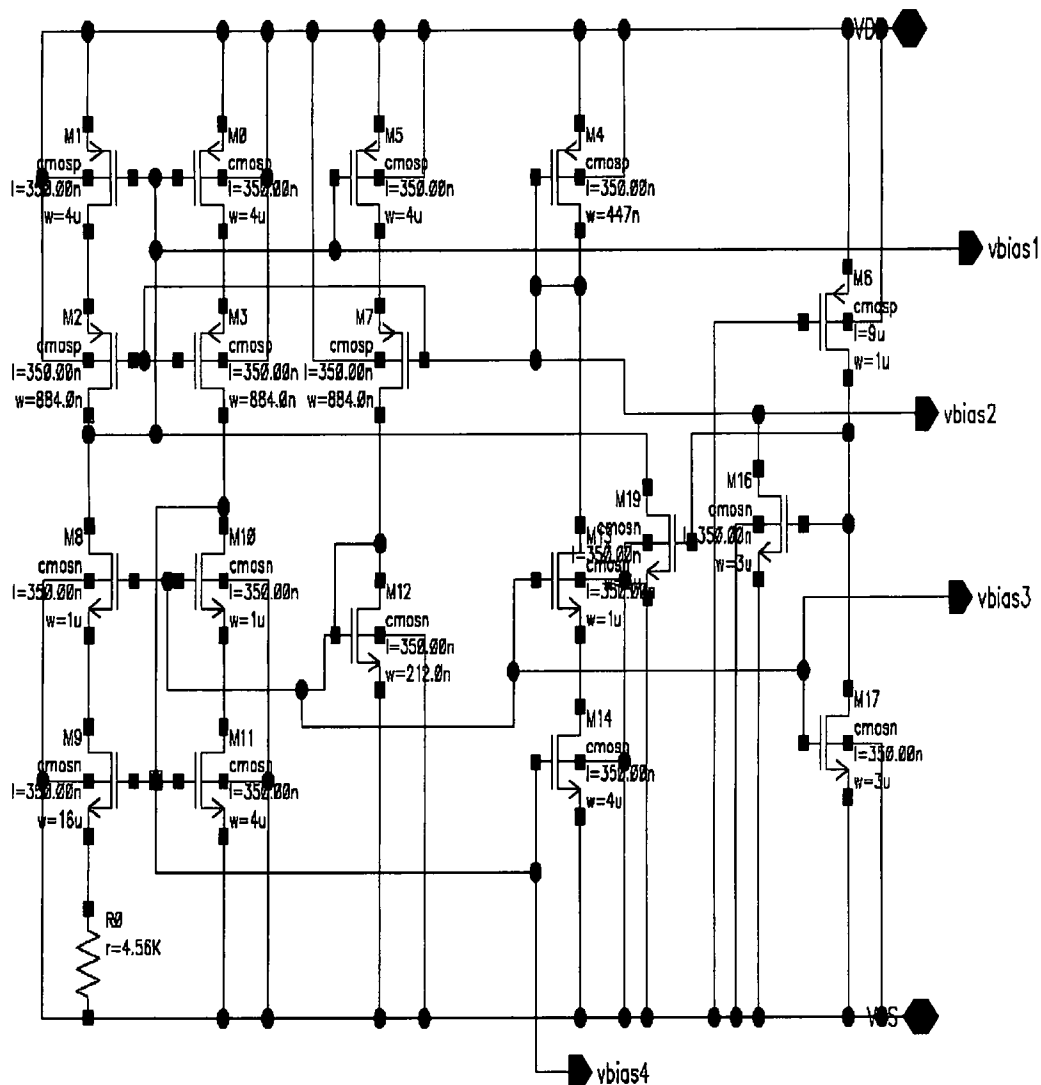


Figure F.8 Wide swing current mirror.

F.3. DNL and INL for 3-bit DAC

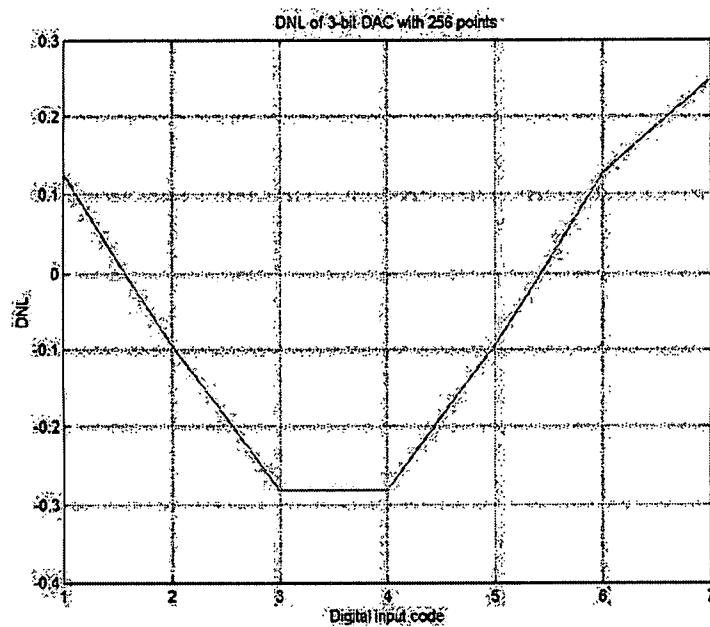


Figure F.9 DNL of the 3-bit DAC.

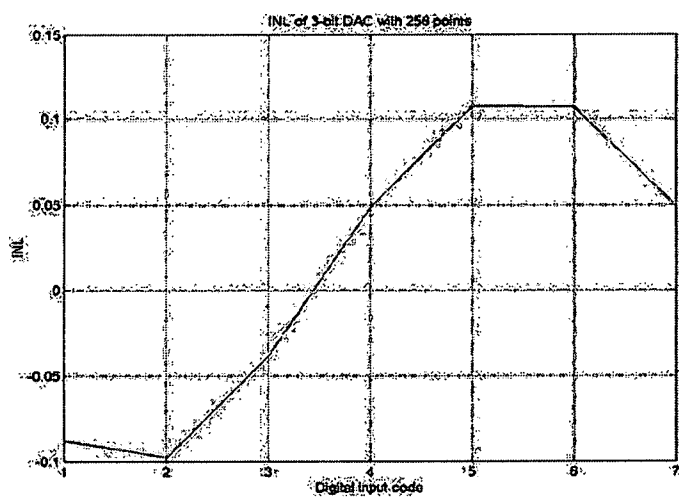


Figure F.10 INL of the 3-bit DAC.

F.4. Switched Capacitor Integrator Response

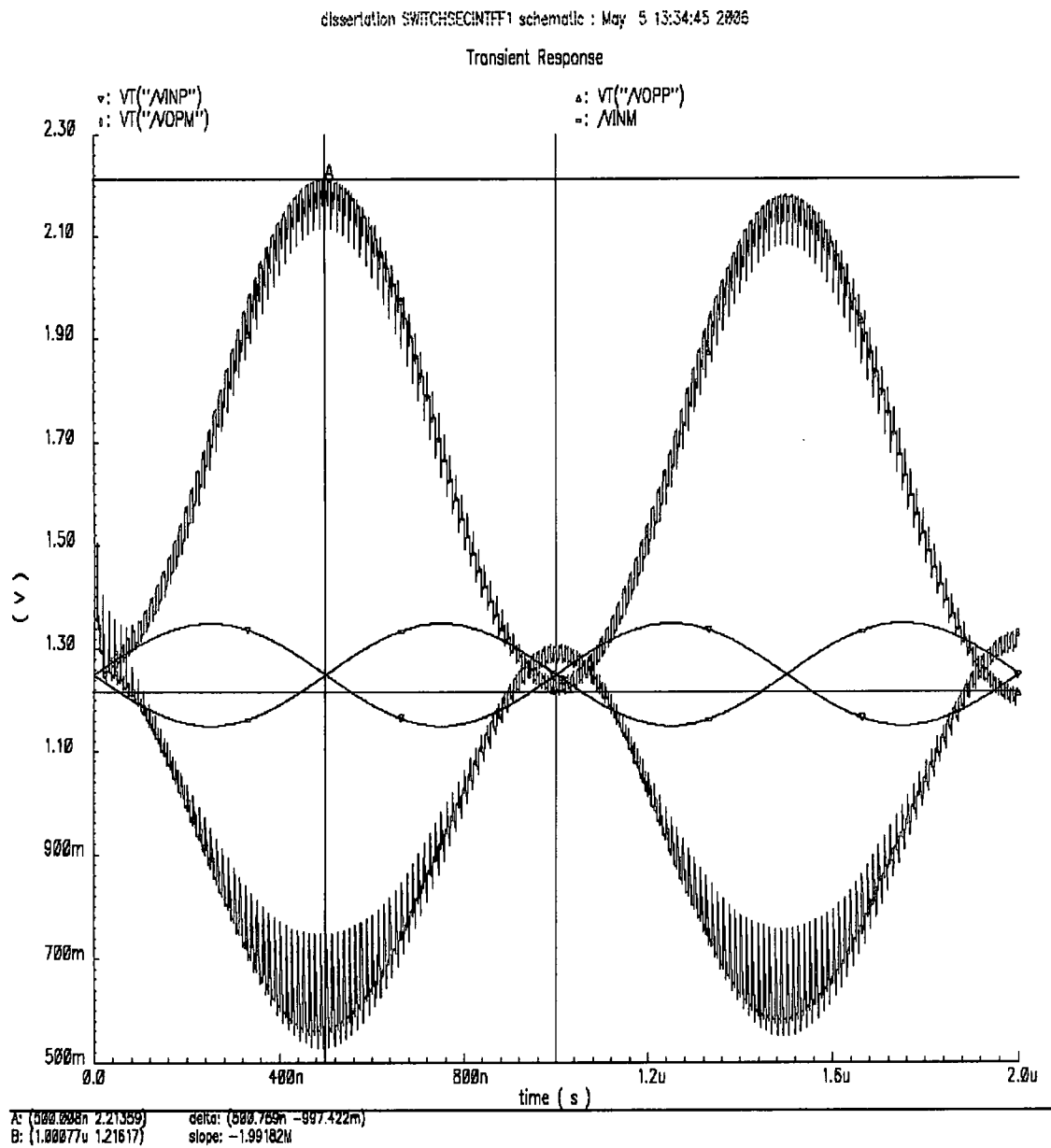


Figure F.11 Response of a switched capacitor integrator.

Appendix G Testing of Physical Layout of the ADC

The cif (CALTECH Intermediate Format) file format of the MOSIS pad frame for 0.5 μ m AMI (C5N) process was imported in Cadence. This is the top-most level in the hierarchy. The physical layout of the ADC was completed and imported into this 900 μ m \times 900 μ m pad-frame. This pad frame is a 40-pin tiny frame with several sub cells such as, PadInC, PadOut, PadVdd, PadIO, PadGnd, PadARef, PadSpace and PadNC. The function of each sub cell is given below:

1. **PadGnd:** This pad is ground pad to connect all the ground nodes.
2. **PadVdd:** This pad provides the supply voltage to the entire chip.
3. **PadOut:** This is an output pad where digital outputs will be connected (DOUT).
4. **PadNC:** This is a pad spacer and is not connected.
5. **PadIO:** This is input output pad for analog input/output signals.
6. **PadInC:** This is an input pad where digital inputs will be connected (DI).
7. **PadARef:** This pad pin is available to connect analog bias voltages.
8. **PadSpace:** This is provided at the corners to route the Vdd and Gnd along the chip

The arrangement of the input-output, bias voltages, supply voltages for the chip layout of second order feed-forward, switched capacitor integrator and operational amplifier are provided along with their functions in Table G.1. The bias voltages of the operational amplifier are given in Table G.2.

Table G.1 Pin arrangements of physical IC layout.

Pin Name	Pin No.	Pads	Pin Function
Vdd	1	PadVdd	Positive Supply
Gnd	22	PadGnd	Ground
Vinp	7	PadIO	+ve Sine-wave + dc(Vcm)
Vinm	9	PadIO	-ve Sinewave + dc(Vcm)
Int1p	26	PadIO	First_integrator_output
Int2p	27	PadIO	Second_integrator_output
Comparator_p	3	PadOut	Comparator_positive_out
Vbias1	2	PadARef	Bias_voltage1_opamp
Vbias2	21	PadARef	Bias_voltage2_opamp
Vbias3	24	PadARef	Bias_voltage3_opamp
Vbias4	23	PadARef	Bias_voltage4_opamp
Vbias(cmfb)	20	PadARef	Bias_voltage_cmfb
VREF	34	PadARef	Second_order_Reference
Opampinp	15	PadIO	Opamp_positive_input
Opampinm	16	PadIO	Opamp_negative_input
Opampoutp	18	PadIO	Opamp_positive_output
Opampoutm	19	PadIO	Opamp_negative_output
Common_mode_out(Vcm)	37	PadARef	Analog Ground
Second_digitalp (Y ₁)	27	PadOut	Second_order_out_positive
Clk	39	PadInC	Sampling clock
Int_switched_p	13	PadIO	Switched int. Pos. out

Table G.2 Bias voltages of the operational amplifier.

Bias voltages	Value in volts
Vbias1	3.75
Vbias2	3.33
Vbias3	1.333
Vbias4	0.8869
Vbias(cmfb)	0.98092
Vcm	2.5

Due to unavailability of high-performance testing instruments, the testing of the ADC is carried out at a lower frequency using the following steps:

1. Provide an input signal with a suitable clock frequency of 10 MHz from a function generator. This input signal should be a sine-wave with amplitude of 1.3V peak and dc offset of 2.5V. The reference voltage of 5 V for the second order modulator, the two reference voltages of 1.0 and 4.0 V for the multi-bit first order modulators, and dc bias voltages for the op-amp should be provided externally using dc supply generators.
2. The input frequency should obey the principle of coherent sampling and must have a sampling period that is an integer number of the testing time. For an input frequency 19.53 KHz, the testing should be carried out for 4096 samples.
3. The time domain digital output of the second order modulator Y_1 should be captured using data/spectrum analyzer. Similarly, the three digital time domain outputs of the first order modulator b_0 , b_1 , b_2 should be captured using

data/spectrum analyzer. Both outputs can be imported into a PC. The FFT spectrum of the output signal can be obtained using Matlab or C/C++ algorithm. The SNR, resolution, SDNR, and other dynamic performance parameters are determined by signal processing algorithm. Figure G.1 shows a die of the physical layout of the proposed delta sigma ADC. This chip consists of the second order modulator, comparator, op-amp, and switched capacitor integrator.

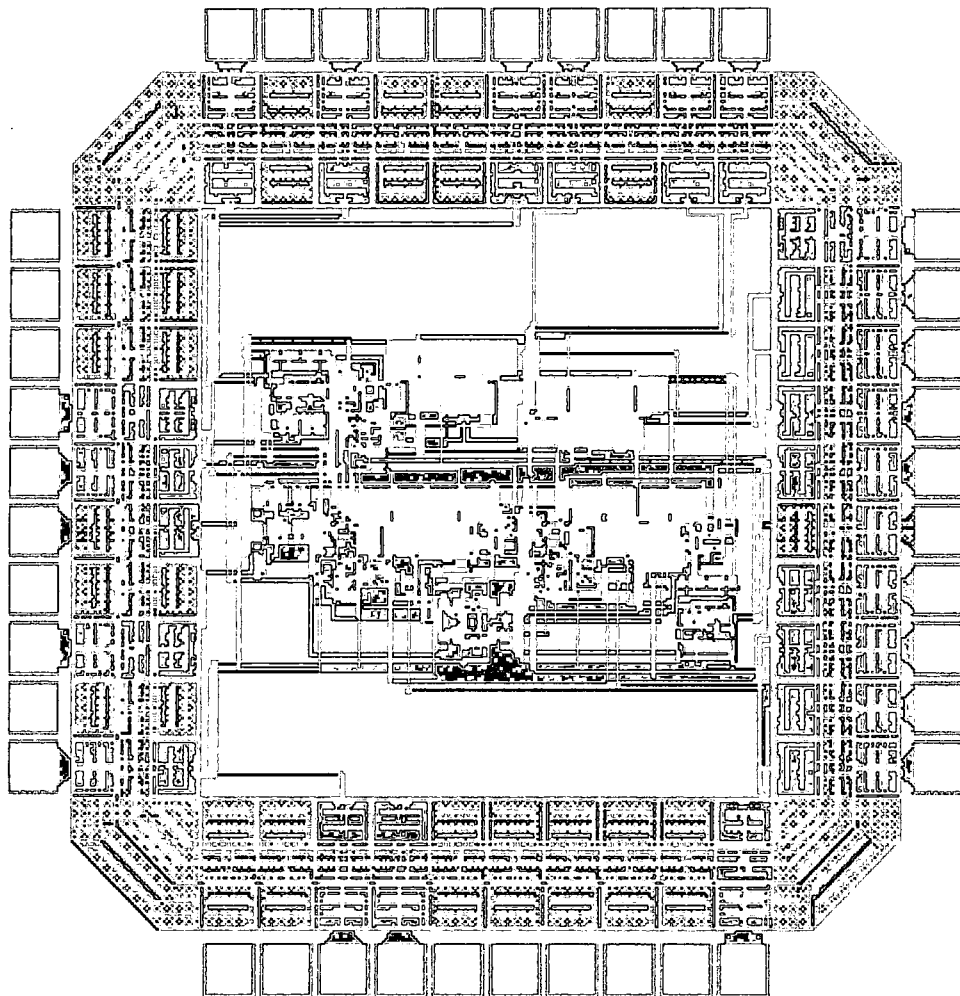


Figure G.1 Die Layout of second-order modulator, integrator, op-amp.

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