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DIGITALLY CONTROLLABLE VARIABLE GAIN AND VARIABLE SLOPE
HIGH PERFORMANCE X-BAND AMPLIFIER

Thesis

Submitted to

The School of Engineering of the
UNIVERSITY OF DAYTON

in Partial Fulfillment of the Requirements for
The Degree
Master of Science in Electrical Engineering

by

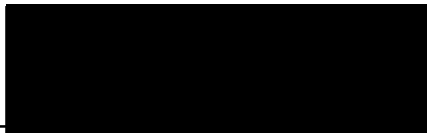
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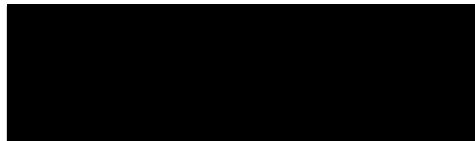
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Digitally Controllable Variable Gain and Variable Slope High Performance X-
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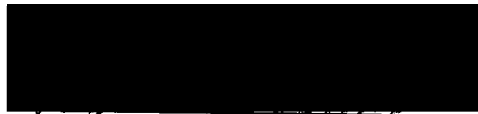
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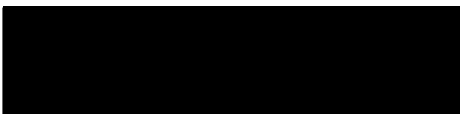
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ABSTRACT

DIGITALLY CONTROLLABLE VARIABLE GAIN AND VARIABLE SLOPE HIGH PERFORMANCE X-BAND AMPLIFIER

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As the performance of silicon-based technologies increases the ability to integrate digital, analog, and RF components onto a single substrate, the development of mixed signal integrated chips becomes possible. Hence, the next generation radar / communication systems would have the ability to adapt or reconfigure for environmental changes based on real time needs. Furthermore, next generation RF components would be able to compensate for process variation and device mismatches. This thesis reports on the development of a digitally controllable variable gain and variable slope X-Band amplifier (VGSA) using 0.13 μm Silicon Germanium (SiGe) Bipolar CMOS (BiCMOS) technology. The VGSA consists of an X-Band amplifier, current steering digital-to-analog converter (DAC), and commercial voltage DAC, which are integrated into a single module on a low loss FR4 substrate. The measurements of the VGSA yielded a

maximum gain of 8.38 dB with 2.30 dB of amplitude tuning and 0.000 to -0.125 dB/GHz slope adjustment. These results show that the current 0.13 μm SiGe design node is capable of supporting an adaptive X-band RF component. This VGSA increases circuit yield by reducing the impact of process variation and device mismatch while maintaining adaptive RF functionality.

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INTRODUCTION

The goal of this research effort is to develop an X-Band Radio Frequency (RF) variable gain and variable slope amplifier (VGSA) with integration to a digital-to-analog converter (DAC). A silicon-germanium (SiGe) 0.13 μm bipolar complimentary metal-oxide-semiconductor (BiCMOS) technology was chosen for the amplifier and the current steering DAC components. The 0.13 μm SiGe BiCMOS technology combines heterojunction bipolar transistors (HBT) with complimentary metal-oxide-semiconductor (CMOS) field effect transistors (FET) having a cutoff frequency (f_T) and maximum frequency of oscillation (f_{max}) in the 200 GHz regime. This thesis work develops a mixed-signal based amplifier to address the need for an adaptive circuit suitable for future receiver/exciter (RX/EX) architectures. For example, in a highly integrated, RF front-end chipset that contains multiple amplifiers, mixers, filters and oscillators, it becomes very difficult to maintain gain flatness and gain performance due to environmental and fabrication variations. As the chipset increases in complexity, the ability to rework or tune the chip decreases proportionately. In order to meet system operation requirements, individual RF components would require fine tuning to meet system needs. These include manual or electronic adjustments to variable gain amplifiers, attenuators, and tunable filters. In general, system engineers would perform manual adjustments and calibration of RF components to ensure a

balance between various channels so the entire receiver / exciter (RX/EX) system would perform in a coherent manner. The calibrated data set for various environmental temperature and other system requirements are generated. Based on the data set, a look up table is produced and stored in memory. The final system's operating condition is based on the calibrated data set. The development of the VGSA would alleviate a large part of the system pre-qualification. The insertion of the VGSA component in a complex RF system would increase the likelihood the system would meet performance requirements and hence achieving first pass design success. This thesis demonstrates that in an integrated RX/EX architecture, the VGSA has the capability to increase system performance and improve yield by adjusting amplifier gain performance. The amplifier development will play a critical role in any RX/EX chain due to its ability to compensate for process variation, received power levels and gain slope; while mitigating the associated cost of re-design resulting in 1st pass success.

CHAPTER I

Project Definition

1.1 The Goal/Objectives of the Study

The goal of this research effort is to develop a tunable RF amplifier consisting of circuit design, fabrication, and characterization of a monolithic X-Band variable gain and variable slope amplifier (VGSA) with an integrated digital analog converter (DAC). This amplifier combines two functional characteristics that enable amplifier gain and slope adjustments. The first characteristic is the ability to attenuate the gain without degrading the bandwidth of the amplifier as shown in Fig.1.1. The second functionality, illustrated in Fig, 1.2, is to tune the gain slope without affecting the overall bandwidth. These characteristics make the VGSA ideal for integration into a highly integrated RX/EX chains.

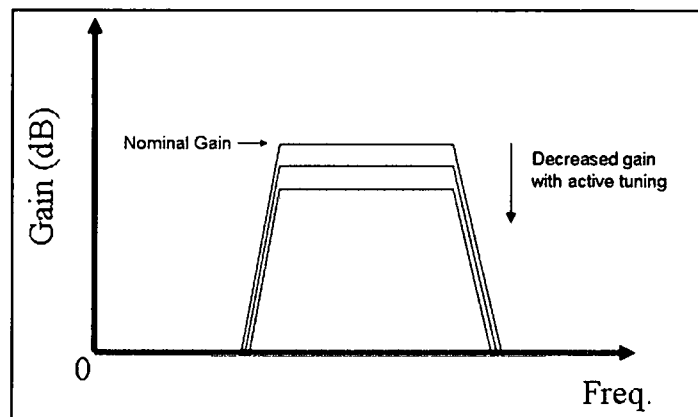


Figure 1.1: Ideal variable gain attenuation

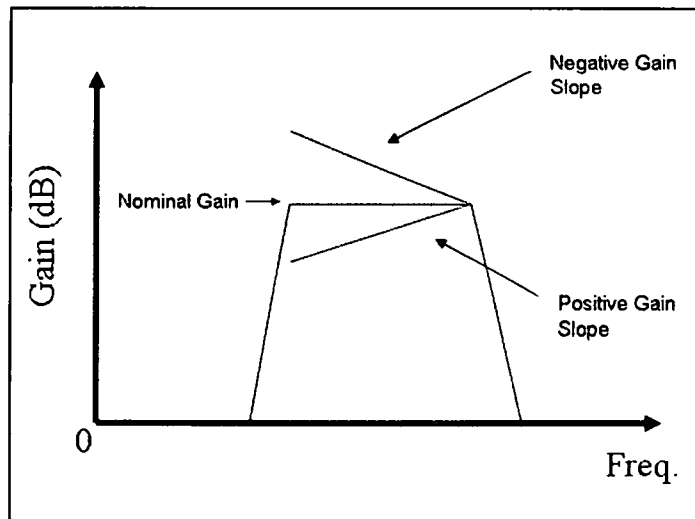


Figure 1.2: Ideal variable slope tuning

1.2 SiGe Technology

A SiGe 0.13 μm BiCMOS technology is chosen for the amplifier demonstration. SiGe BiCMOS technologies combine HBTs and FETs having f_T and f_{max} in the 200GHz regime on a single silicon reticle. This technology also supports high quality passive elements such as; inductors, capacitors, and resistors.

1.3 The Purpose/Significance of the Study

The purpose of this circuit is to address the need for adaptive RF functionality in silicon receiver exciter modules. As silicon-based technologies continue to advance in performance, the capability to support integrated RF circuitry becomes more realizable [1-8]. This makes silicon technologies ideal for

next generation wireless receivers where high density digital circuits are required to mate with high performance RF circuitry. However, the cost of entry into the silicon market is extremely high. Figure 1.3 shows that the predicted mask costs for the 0.090, 0.065, and 0.032 μm design nodes are expected to exceed one million dollars per design iteration [9]. Real estate cost on these chips is extremely expensive for large RF amplifiers requiring passive elements for input and output matching networks. Additionally, RF amplifiers are sensitive to process variations across the wafer. This amplifier mitigates the need for redesign due to it's capability to compensate for process variations, temperature, received power levels and gain slope.

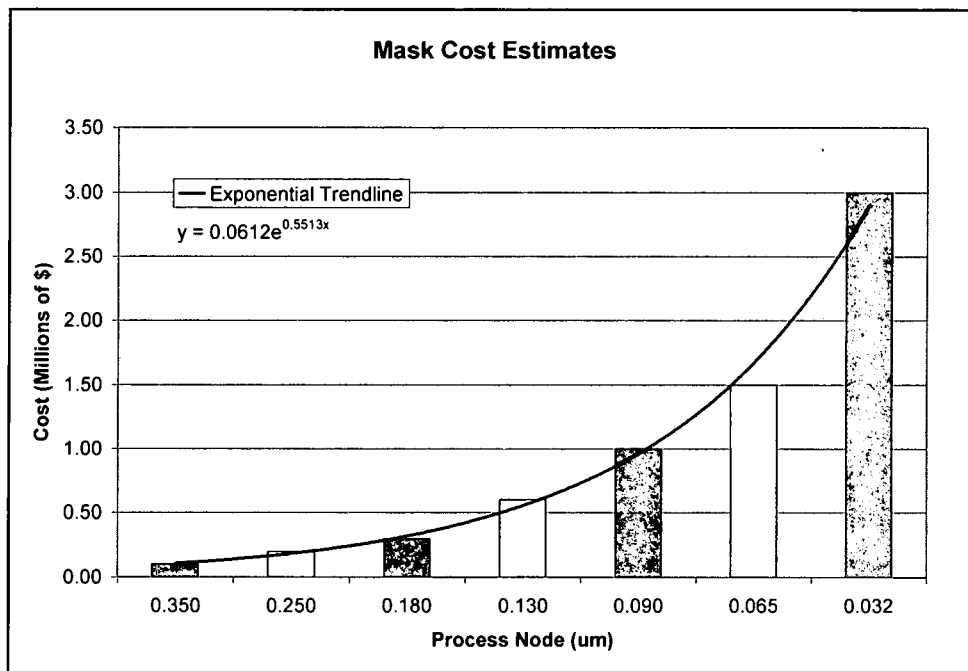


Figure 1.3: Associated Mask Costs from 0.35 μm to 0.032 μm [9]

1.4 VGSA Comparison

A literature search was done as a comparison of the current state of the

art in variable gain and/or variable slope amplifiers. The results of the search are summarized in Table 1.1. Based on the results, previous variable gain amplifier development has been focused at low frequencies (100's MHz) with the ability to tune for large gain attenuation. Variable gain amplifiers operating in X-Band and beyond are typically implemented in GaAs technology. Low frequency VGAs then tends to be implemented in silicon. This thesis work combines high frequency operation with the ability to digitally adjust for gain amplitude and gain slope.

Table 1.1: Technology Comparison

Work	Technology	Frequency of Operation	Gain Variance	Slope Variance (per GHz)
[10]	DGFET	14-17GHz	30dB	-
[11]	GaAs	85MHz	85dB	-
[12]	GaAs	DC-18GHz	-	0.22dB to -0.67dB
[13]	Si CMOS	70MHz	80dB	-
[14]	Si CMOS	150MHz	75dB	-
This work	SiGe CMOS	8-12GHz	2.3dB	0.00dB to -0.125 dB

1.5 Introduction to the Chapters

Chapter 2 provides background information on receiver architectures. Chapter 3 provides detailed information on the process and the devices. Chapter 4 describes the amplifier and supporting digital hardware design. Chapter 5 addresses the test plan development, procedure and results. Finally, Chapter 6 provides the summary and conclusions.

CHAPTER II

Receiver Architectures and Component Metrics

Radio Frequency (RF) receivers are increasing in function and popularity. This is mainly driven by the emergence of the cellular phone, Ultra Wideband, and Bluetooth markets and the need for fully integrated receiver solutions [1-8]. The RF receiver's primary purpose is to condition the signal through amplification, filtering and up/down-conversion without distortion. Once the signal has been appropriately conditioned it is fed into the analog-to-digital converter (ADC) and then input to a DSP for digital post-processing. The net result of this process provides information on what type of signal (CW, pulsed, PSK, etc...), frequency of operation, and angle of arrival. The ADC component is the system limiter and dictates the frequency plan of the receiver architecture based on the ADC's operation and the associated Nyquist zones [15]. In general, there are two primary RF receiver architectures that are used in today's wireless receivers, homodyne and heterodyne. For simplicity, direct conversion and quadrature architectures will be a subset of the homodyne receiver architecture. This will permit a general discussion of the advantages and disadvantages of these architectures and how they relate to this thesis work.

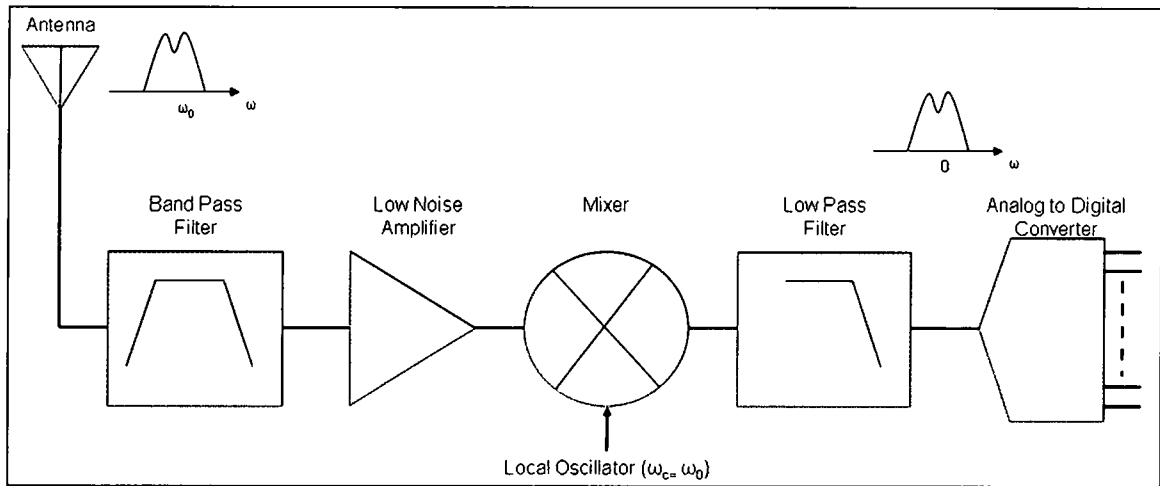


Figure 2.1: Simple Homodyne receiver with ADC

2.1 Homodyne Receiver Architecture

Homodyne receiver architectures have a single down conversion in which the incoming RF frequency is mixed with the local oscillator (LO) and down converted to the baseband frequency. Fig. 2.1 illustrates a simple block diagram of the homodyne receiver. The baseband frequency is established by the ADC component and the bandwidth is determined by the rate in which the ADC can convert the incoming RF signal to a digital stream. Typically in homodyne receivers, the center of the band of interest is directly translated to zero frequency [16]. A subset of the homodyne receiver architecture is a quadrature down conversion configuration which provides phase and amplitude information of the incoming RF signal as shown in Fig. 2.2. The quadrature architecture requires the incoming LO signal to be supplied in both sine and cosine form and fed into two parallel homodyne systems [17-18]. The resultant parallel paths provide in-phase (I) and out of phase (Q) information about the incoming RF signal. This is usually referred to as I and Q.

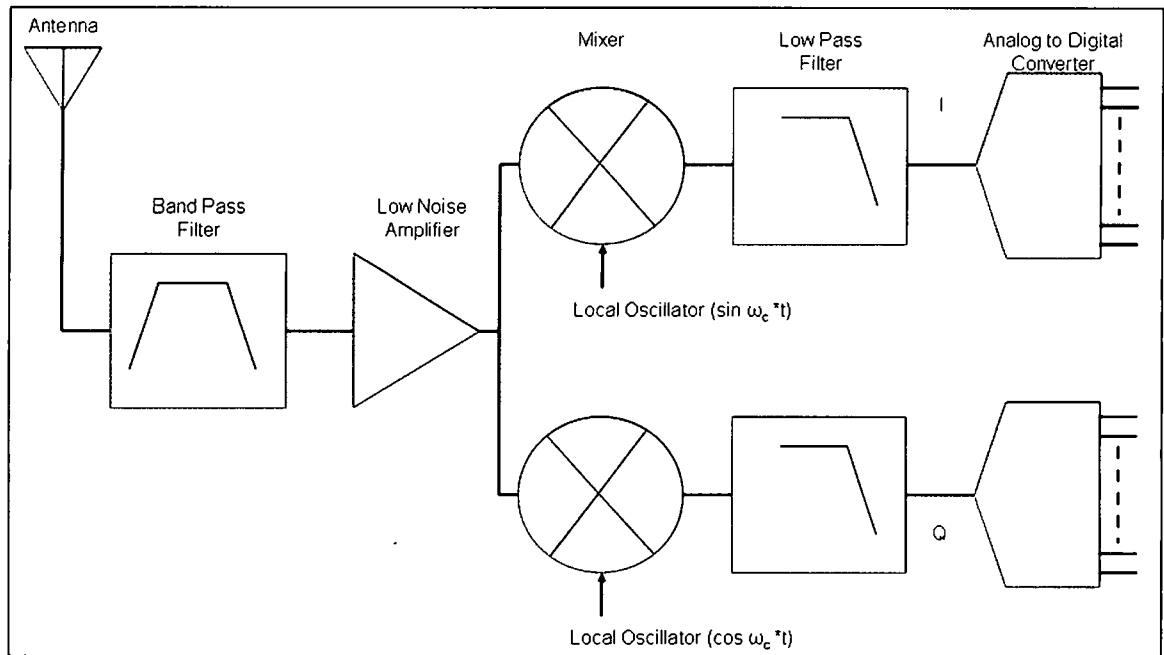


Figure 2.2: Homodyne receiver with quadrature down conversion and ADC's.

The main disadvantage of the homodyne receiver architectures is that the DC components may corrupt the converted RF frequency which now resides at or near DC [19]. Another disadvantage of this type of receiver is self-mixing. This occurs when the LO leakage is amplified through the receiver which then distorts the incoming RF frequency. Most of the disadvantages associated with self-mixing can be compensated using sophisticated offset-cancellation techniques in the digital domain. Another disadvantage with homodyne receivers is that they are susceptible to higher-order distortion. This occurs when two interferers are close to the band of interest and experience a nonlinearity. This nonlinearity causes them to be translated to a lower in-band frequency before the mixer. The mixer down-converts these signals to the baseband with finite attenuation, therefore corrupting the baseband signal. Quadrature receivers are

sensitive to I and Q mismatch. This occurs when the I and Q outputs are not equal or their phase difference deviates from 90 degrees in turn causing the error rate of detecting the baseband signal to rise. Amplitude and Phase mismatches occur when the two mixers, in each leg, are not identical. This is due to process variation across the wafer and additional parasitics in the design.

2.2 Heterodyne Receiver Architectures

The heterodyne receiver architecture was developed to address many of the disadvantages of the homodyne receivers outlined above. This architecture employs multiple conversions to enhance the ability of the receiver to identify weak signals in the presence of strong interferers [15]. Figure 2.3 outlines a double down conversion architecture. Typically a band pass filter is inserted between the first intermediate frequency (IF) and the second IF to remove any DC offsets from corrupting the signal [19].

Heterodyne receivers are susceptible to the images generated by the LO-RF mixing products. Two general forms of the mixing operation are:

$$RF - LO = IF \quad (2.1)$$

$$LO - RF = IF \quad (2.2)$$

where:

- LO: Local Oscillator Frequency (GHz)
- RF: Incoming RF (GHz)
- IF: Outgoing Down-converted Frequency (GHz)

From these equations two distinct values of the LO can be chosen to achieve the

desired IF value. For instance, if the incoming RF signal, is 10 GHz and the final IF signal is 4 GHz, then a high side LO of 14 GHz or a low side LO of 6 GHz may be chosen. In this case, the mixer will translate both high side and low side LO's to the same IF frequency. If the mixing products of each mixer are not filtered out correctly they will corrupt the final RF signal. Therefore, this architecture requires a bandpass filter to reside between the two mixers and prevent the signals of interest from being corrupted.

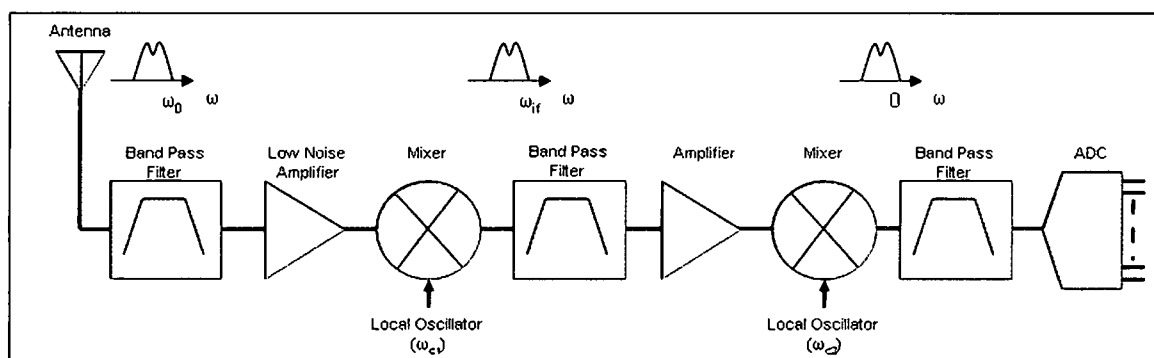


Figure 2.3: Heterodyne receiver with ADC.

Ideally the baseband gain amplitude across the receiver band would be flat minimizing the gain variation before entering the ADC. If the gain is not flat either the baseband signal could potentially be clipped or it is not fully utilizing the ADC. However, due to active device roll-off as a function of frequency coupled with low Q passive components, and mixer translation, it is difficult to obtain a flat gain across the receiver band for the RF front-end. The cascaded gain equation, Equation 2.3, highlights that the additive sum of each gain term through the receiver system is dependent on each receiver component's gain product. This means that any particular receiver component could compensate for a gain slope

produced by another component in the chain.

$$\sum_{i=1}^N \text{gain}_i(f) \Rightarrow \text{gain}_N(f) = \text{gain}_1(f) + \text{gain}_2(f) + \dots + \text{gain}_{N-1}(f) \quad (2.3)$$

where:

- N: the number of stages
- f : frequency

The noise figure of the receiver is another critical specification and determines the sensitivity of the receiver. The cascaded noise figure equation, Eqn. 2.4, shows that the noise figure of the system is primarily dependent on the first component, mainly the low noise amplifier (LNA). This amplifier, having a significant amount of gain, will set the noise figure of the entire system. This is due to the gain of the first stage being the divisor for the subsequent stages and the noise figure of the first stage adding to the subsequent stages.

$$nf_1 + \sum_{i=2}^N \frac{nf_i - 1}{\prod_{j=1}^{i-1} \text{gain}_j} \Rightarrow nf_N = nf_1 + \frac{nf_2 - 1}{\text{gain}_1} + \frac{nf_3 - 1}{\text{gain}_1 \text{gain}_2} + \dots + \frac{nf_N - 1}{\text{gain}_1 \text{gain}_2 \dots \text{gain}_{N-1}} \quad (2.4)$$

where:

- N: the number of stages
- nf : noise figure

CHAPTER III

Fabrication Process

SiGe technology allows RF and digital logic to be integrated on a single substrate. As the technology continues to scale to smaller feature sizes, the capability to support high frequency circuit components becomes realizable. The ability to support digital and RF integration makes SiGe technology appealing for compact miniature RX/EX that requires tight integration to the digital backend. This, in turn, reduces packaging costs, component size, and weight. The cumulative effect is a dramatic cost reduction. The fabrication process chosen for this thesis is a 0.13 μm BiCMOS SiGe technology. This SiGe process node was the highest performing available at the time of development and fabrication. Figure 3.1 plots two important figures of merit, f_T and f_{max} , for microwave transistors at each technology node. To the first order effect, f_T and f_{max} are related to device transit time which corresponds to emitter width and parasitic capacitances for HBTs per the following equations [6]:

$$f_t = \frac{1}{2\pi \tau_F} \quad (3.1)$$

where:

$$\bullet \quad \tau_F = (C_{be} + C_{bc}) \left(R_e + \frac{kT}{qI_c} \right) + \frac{W_b^2}{2D_b} + \frac{W_c}{2v_s} + R_c C_{bc} \quad (3.2)$$

- τ_F : Forward transit time
- Cbe: Emitter-base capacitance
- Cbc: Base-collector capacitance
- Re: Emitter series resistance
- k: Boltzmann's constant
- T: Temperature [K]
- q: Elementary charge
- Ic: Collector current
- Wb: Vertical base width
- Db: Electron diffusivity in the base
- v_s : Electron saturation velocity
- Wc: Collector-base vertical depletion width
- Rc: Collector resistance

$$f_{max} = \sqrt{\frac{f_t}{8\pi R_b C_{bc}}} \quad [6] \quad (3.3)$$

where:

- Rb: Base Resistance

Fig. 3.1 shows the trend of both f_T and f_{max} versus lithographic feature size for BiCMOS and CMOS technologies. The 0.13 μm process node supports a f_T of 200 to 300 GHz for the high-speed npn HBT devices depending on the particular vendor. Also, Fig. 3.1 shows that the comparable CMOS f_T is two to three times lower than SiGe HBT's for any given technology node. Thus, in order to achieve

similar f_T performance from CMOS FET vs. BiCMOS HBT one would have to choose the 0.065 μm process node to yield greater than 200 GHz performance. However, this would incur a significant increase to the mask costs as shown in Fig. 1.1.

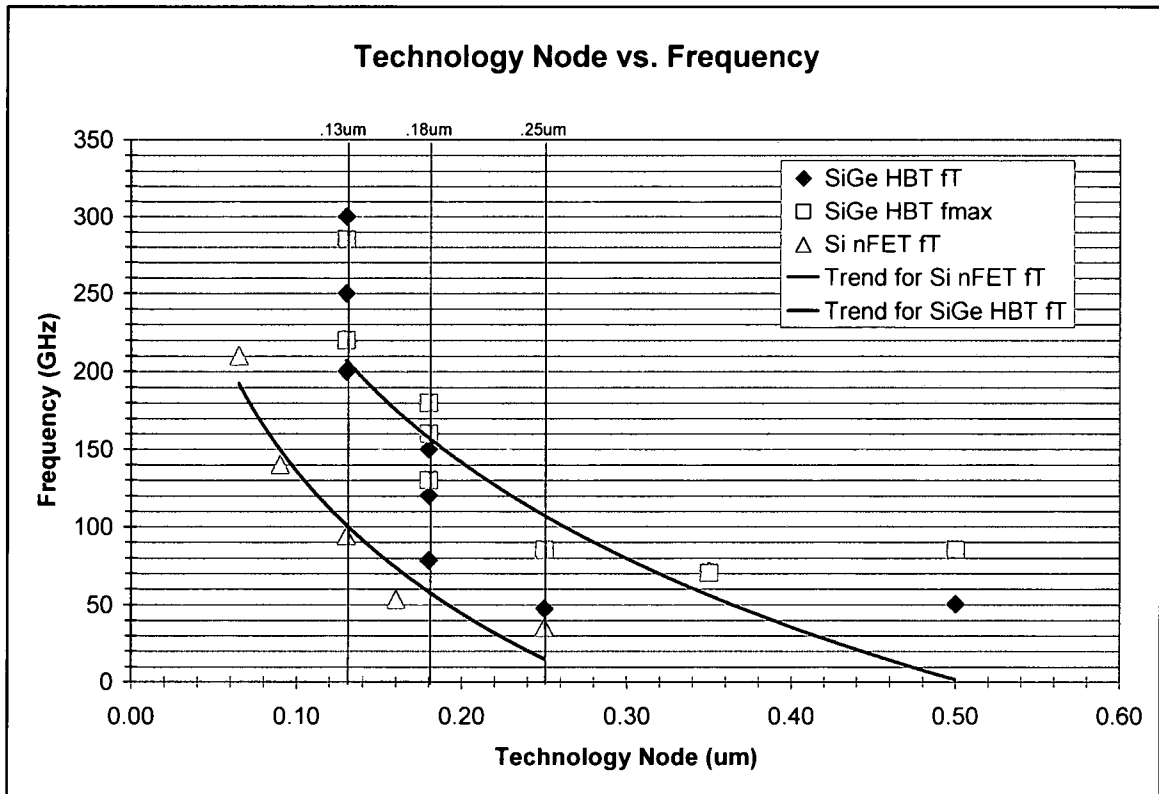


Figure 3.1: SiGe HBT vs. CMOS f_T for each technology node [5,7]

Another important metric when choosing a RF device is the collector-emitter breakdown voltage (BV_{ceo}). The BV_{ceo} of reported SiGe devices and their CMOS counterpart are shown in Fig. 3.2. As device feature size decreases, the associated BV_{ceo} also decreases proportionally. The device breakdown voltage limits the amount of available headroom for amplification.

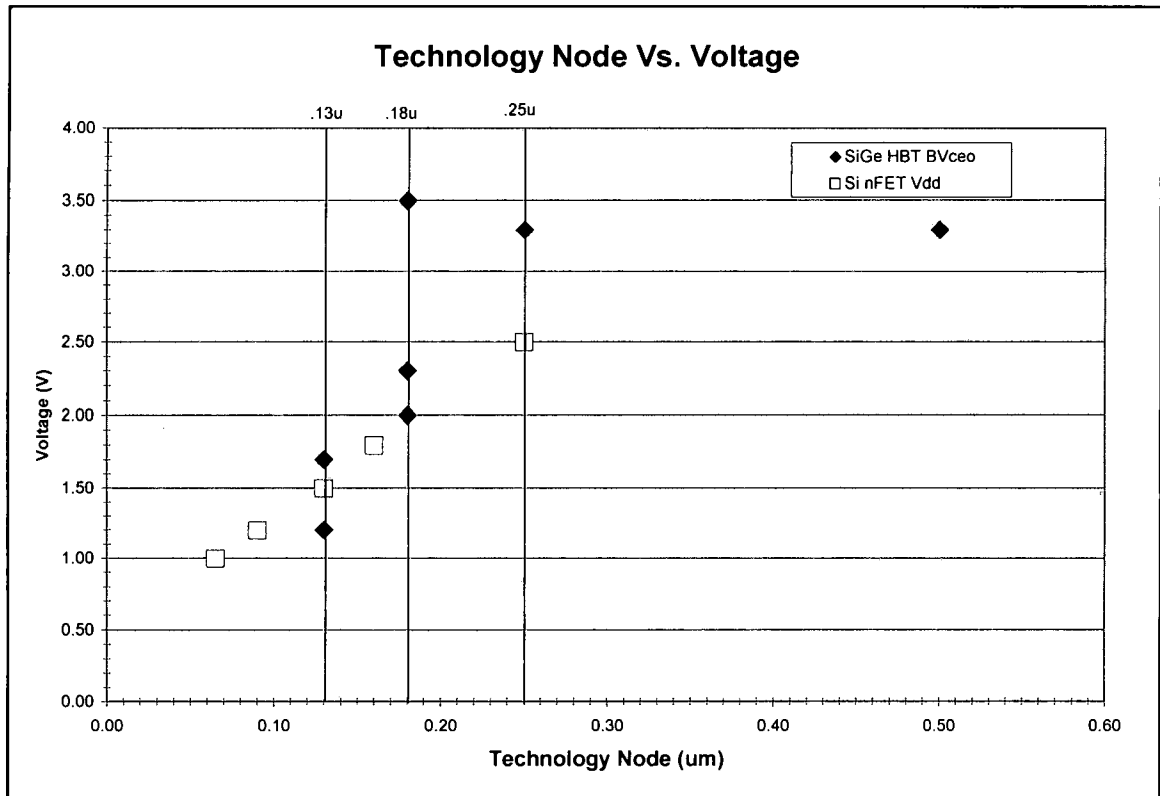


Figure 3.2: Relative operating voltage for each technology node [5,7]

The associated CMOS lithography parameters for the nodes in Fig. 3.2 are shown in Table 3.1. CMOS device scaling is accomplished by thinning the gate oxide (T_{ox}) for each subsequent node this increases the f_T and decreases V_{dd} of the device. Additionally, SiGe technology process nodes support high-quality passive devices such as precision resistors, metal-oxide-silicon (MOS) and metal-insulator-metal (MIM) capacitors, and high Q spiral inductors.

Table 3.1: CMOS Lithography Parameters [5]

Parameter	Units	CMOS Lithography Generation				
Node	um	0.25	0.18	0.13	0.09	0.065
T_{ox} (inv)	A	62.0	44.5	31.2	22.0	18.0
V_{dd}	V	2.5	1.8	1.5	1.2	1.0
f_T	GHz	35	53	94	140	210
pPoly Res	$\Omega/sq.$	210	260, 1600	340, 1700	260, 1700	310, 1600

3.1 SiGe Active Devices

The selected process node, for this project, is the SiGe 0.13 μm BiCMOS Technology. This technology has a minimum device feature size of 0.13 μm and supports both HBTs and FETs. The HBTs are a conventional vertical bipolar transistor illustrated in Fig. 3.3 showing the emitter, base, and collector for an NPN device. The HBT base has a graded germanium doping profile enhancing the carrier mobility from the collector to the emitter, shown in Fig. 3.4. The introduction of 10% Ge into the base region of the SiGe HBT changes the bandgap by 75 meV thus enhancing the collector current and the dc current gain (beta) [20]. The change in the bandgap across the device causes a built in drift field which reduces the base transit time and increases the f_T , Eqn. 3.1. The implantation of the Ge is done using an ultrahigh-vacuum/chemical vapor deposition (UHV/CVD) method for depositing epitaxial silicon. Passivating the wafer surface with hydrogen and performing UHV/CVD at temperatures $< 850^\circ\text{C}$ results in an epitaxial film with $< 10^3$ defects/ cm^2 [21]. This low-temperature epitaxy (LTE) process enables abrupt, fully activated in situ boron doping and the controlled incorporation of germanium into the silicon lattice [22]. The LTE process replaces the implanted base with an in situ-grown base and graded germanium HBT [23].

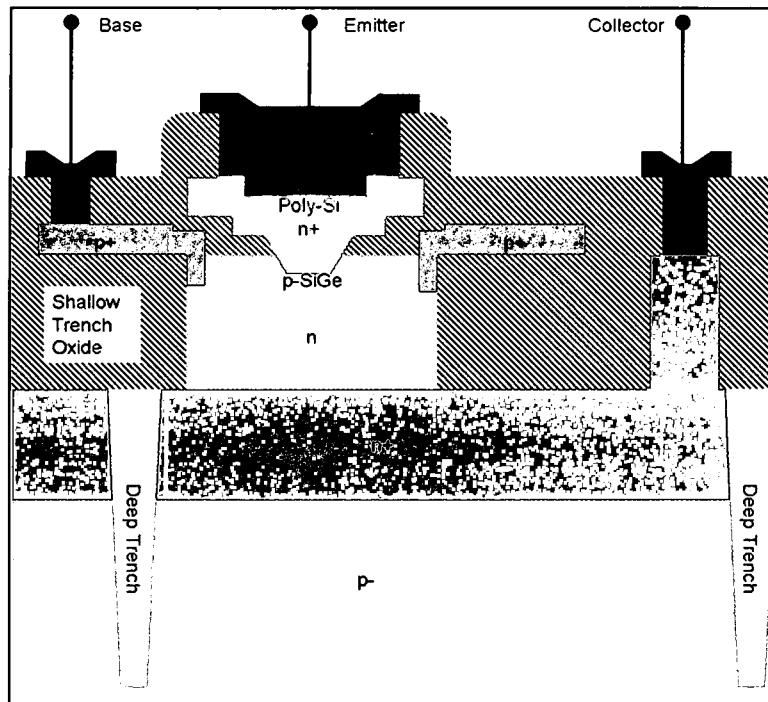


Figure 3.3: Cross section of SiGe HBT [24]

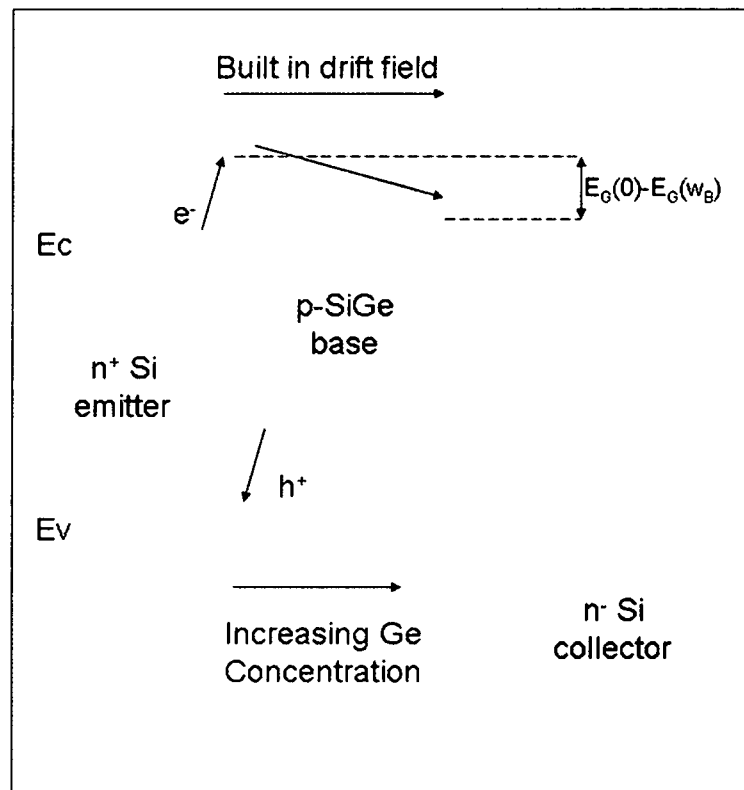


Figure 3.4: Base Germanium Doping Profile [25]

Typically, there are two ways in which the device is integrated into the CMOS portion of a process node. They are base-equal-gate and base-after-gate integration methodologies. In the base-equal-gate methodology, the growth and patterning of the NPN SiGe epitaxial base also forms the FET polysilicon gates. Minimizing the number of overall steps required to create both the NPN and FETs. In the base-after-gate process the HBT is formed after the FET is annealed; therefore minimizing the thermal cycles the SiGe base is exposed to and improving HBT device yield [26].

3.2 Metallization Layers

The selected 0.13 μm process node supports 5-7 layers of metallization, Fig. 3.5. The two topmost metal layers consist of thick aluminum metals suitable to support for many of the passive components. The sheet resistance can be calculated from the metal resistivity and thickness shown in Eqn. 3.4 and Table 3.2.

$$DC \text{ Sheet Resistance} \left(\frac{\Omega}{\square} \right) = \frac{\rho}{t} \quad (3.4)$$

where:

- ρ : bulk resistivity (Ohm-meters)
- t : metal thickness (meters)

The bottom three to five metal layers are made of thin copper and can be used for high density digital interconnects. For this thesis work the seven metal layer

option was chosen to enable the integration of digital, analog, and RF functionality. This allowed for the flexibility of using either microstrip or coplanar waveguide transmission line structures in the topmost aluminum metal. The microstrip transmission line structure is selected using the top aluminum metal as the signal line and the lowest copper metal as ground plane. This provides for a solid RF ground return for microwave propagation [27]. Essentially, the same metal stack is used for both the 5 and 7 layer options. The main difference is the number of copper layers added to compose of the number of layers fabricated. The resultant increase in dielectric height moves the topmost Al metal layer farther away from the lossy Si substrate thus minimizing the parasitic coupling with the lossy substrate and improving interconnect insertion loss at microwave frequencies.

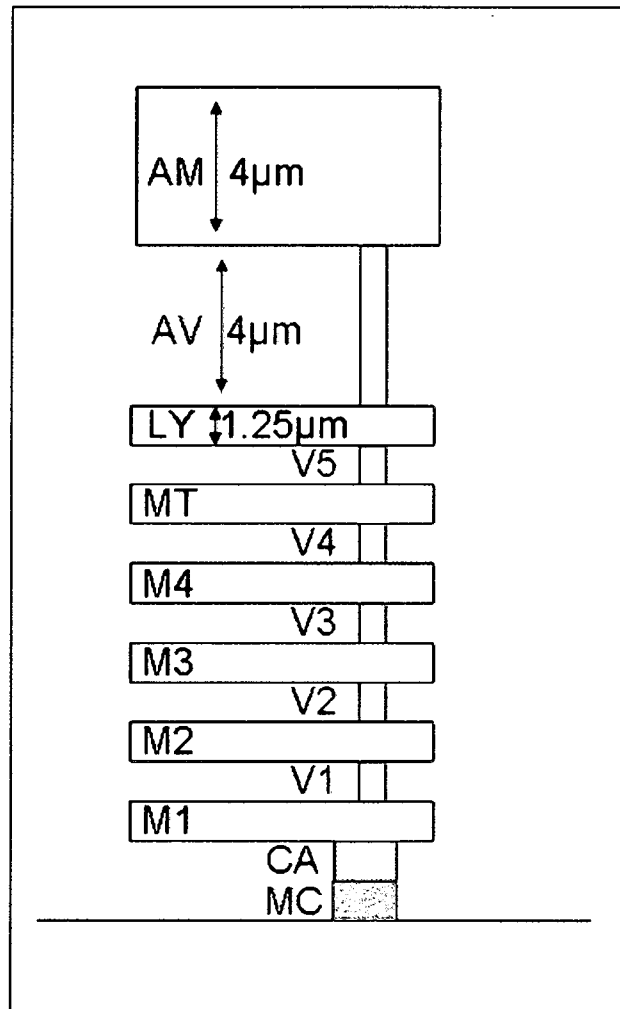


Figure 3.5: Diagram of the cross section of 7-layer metallization option

Table 3.2: Calculated DC Sheet Resistances for the 0.13 μm node

Metal Type	bulk resistivity	metal thickness	DC Sheet Resistance
Units	($\Omega\text{-cm}$)	(μm)	($\text{m}\Omega/\text{sq.}$)
Aluminum	2.65	4.00	6.625
Aluminum	2.65	1.25	21.200
Copper	1.68	0.30	56.000

3.3 Passive Components

The SiGe process offers a variety of high quality passive components necessary for RF, analog, and digital component design. These include high-

quality passive devices such as precision resistors, metal-oxide-silicon (MOS) and metal-insulator-metal (MIM) capacitors, and high Q spiral inductors. These components are critical to the success of integrating high performance RF circuitry with CMOS logic on a single silicon substrate.

The typical resistors offered in the SiGe technologies can be broken into three types: doped polysilicon, diffusion and metal. The figures of merit for resistors are sheet resistance, tolerance, parasitic capacitance, voltage, and temperature coefficients (TCR). Table 3.3 lists the resistor parameters for the SiGe technologies [26]. The offered polysilicon resistors have a low parasitic capacitance, good matching characteristics, and high value resistances for circuit area minimization. The diffusion resistors provide the designer with the ability to create low valued resistors necessary for bias networks. The thin film metal resistor can be placed on any copper layer, with dielectric layers above and below, providing a low parasitic capacitance and good tolerance.

Table 3.3: Resistor figures of merit [26]

Parameter	Units	Available resistors in SiGe Technologies				
		p+ poly	p poly	n+ diffusion	n subcollector	Thin-film metal
Resistor Type	-					
Sheet Resistance	$\Omega/\text{sq.}$	270	1600	72	8	142
Tolerance	%	10 - 15	25	10	15	10
TCR	ppm/Degree C	21	-1105	1751	1460	-728
Parasitic Capacitance	fF/ μm^2	0.11	0.09	1.00	0.12	0.03
Maximum current	mA/ μm	0.6	0.1	1.0	1.0	0.5

The supported capacitors in the 0.13 μm design node are a MOS cap and MIM cap. The MOS cap is a polysilicon gated substrate device using the silicided gate polysilicon, gate oxide and well-doped silicon. The MOS cap resides below the lowermost copper level on top of the silicon substrate. The

resulting capacitor has a large capacitance per unit area. But due to the heavily doped silicon, the resistance results in a poor quality factor. Additionally, the low voltage coefficient makes the MOS cap unsuitable for RF design as a matching network component [28]. However, the MOS cap is well suited for DC bypassing where large valued capacitances are necessary to prevent low frequency oscillation. The MIM capacitor is ideal for RF design due to its low parasitic resistance and high Q. It resides between the thick topmost Al layers and uses a high-k dielectric to achieve a capacitor having $1 \text{ fF}/\mu\text{m}^2$ unit capacitance [26], as shown in Fig. 3.6. Since, the Al layers account for the top plate and bottom plate the series resistance is dramatically reduced compared to the MOS capacitor. Additionally, the parasitic capacitance is reduced due to topmost layers being the farthest away from the lossy silicon substrate. The combination of the reduced series resistance and parasitic capacitance enhances the quality of the capacitor for RF designs, in particular matching networks and on chip filters.

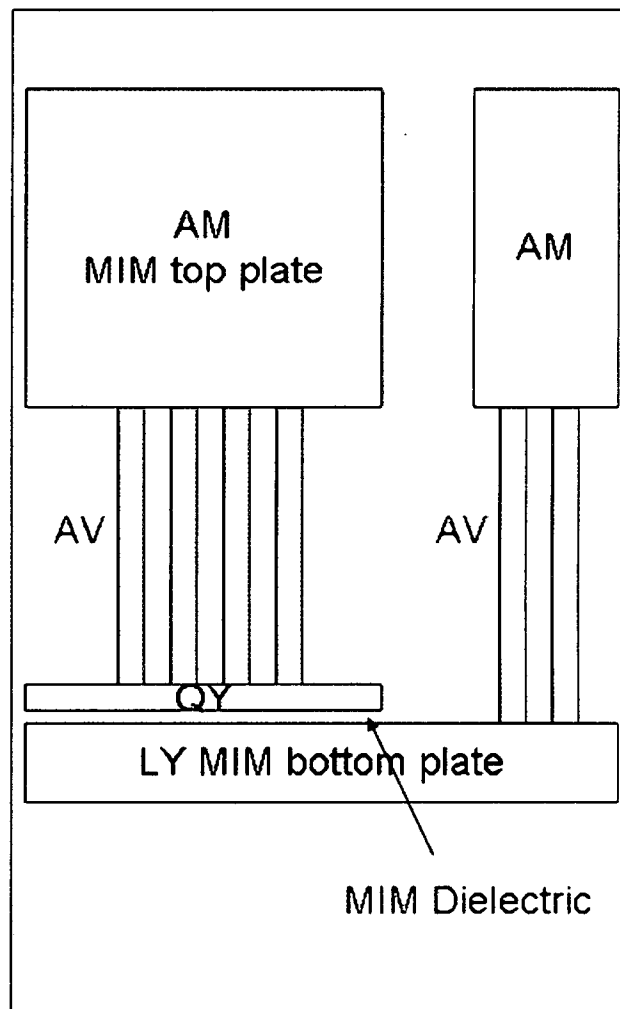


Figure 3.6: MIM capacitor

Inductors are a key component to realize high performance RF designs on silicon. The inductors offered on the 0.13 μm process utilize the thick top metal layer to reduce the series metal loss and the substrate parasitics. In Fig. 3.7, the top two Al layers can be seen with interconnects and inductor coil. This represents the interface of the inside turn to the outside of the inductor. The main draw-back to using this inductor is its current handling capability is limited to the lower Al layer and the vias that connect them to the top metal layer.

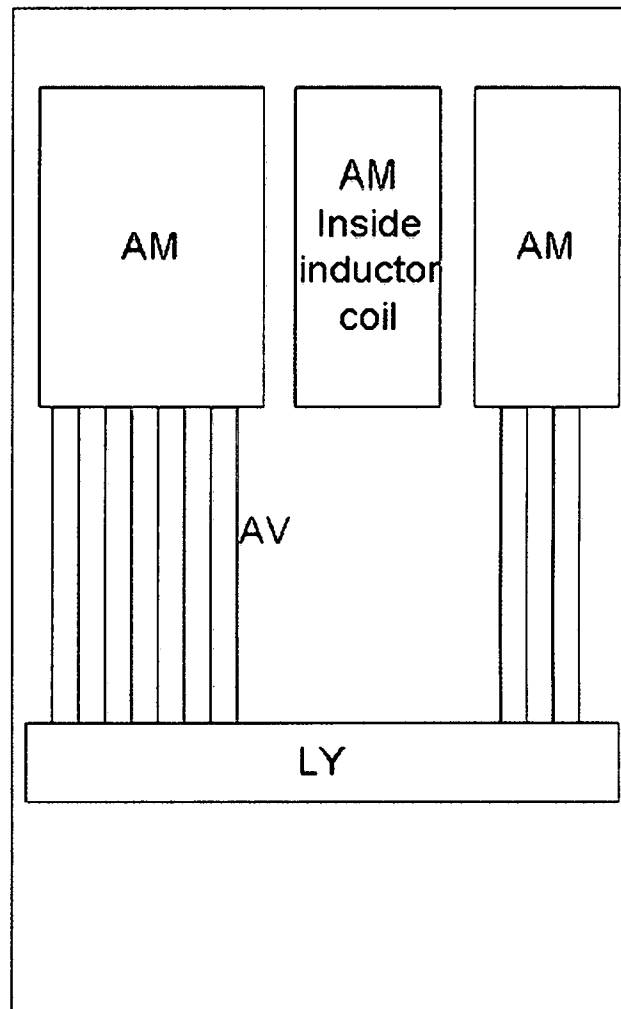


Figure 3.7: Al metal layers forming an inductor

The top-two metal layers are utilized to maximize the Q factor of the inductor.

The Q factor for an inductor is defined as:

$$Q_{factor} = \frac{\omega L_s}{r_T} \quad (3.5)$$

where:

- ω : frequency
- L_s : spiral inductance
- r_T : total series resistance

The quality factor is effectively the ratio of inductive reactance (ωL_s) to the total series resistance (r_T) [27]. For estimation purposes, the Q-factor can be approximated by the ratio of the imaginary and real components, Eqn 3.5 [29]. This estimate is good for low frequency approximation. However, at high frequency of operation, the parasitics of the inductor play a larger part. Reported Q's for SiGe technologies are in the 5-20 range depending on the inductance value [5, 6, 30-37]. Virtually any size or shape inductor can be fabricated in this process giving the designer flexibility in placement and use.

$$Q_{CONV} = -\frac{Imag\{Y_{11}\}}{Real\{Y_{11}\}} \quad (3.5)$$

Figure 3.8 illustrates many of the common problems associated with inductors implemented in the SiGe process. The left side inductor was simulated at low frequency and shows a more uniform current distribution compared to the inductor on the right. This highlights that most of the current in the inductor on the right is being carried through a thin region, highlighted in red. This thin region is determined by the metal properties and the skin depth or frequency and provides key insight into the quality of the inductor. Additionally, since the inductor has no isolation mechanism preventing eddy currents from generating below the inductor, the quality of the inductor is further decreased [27].

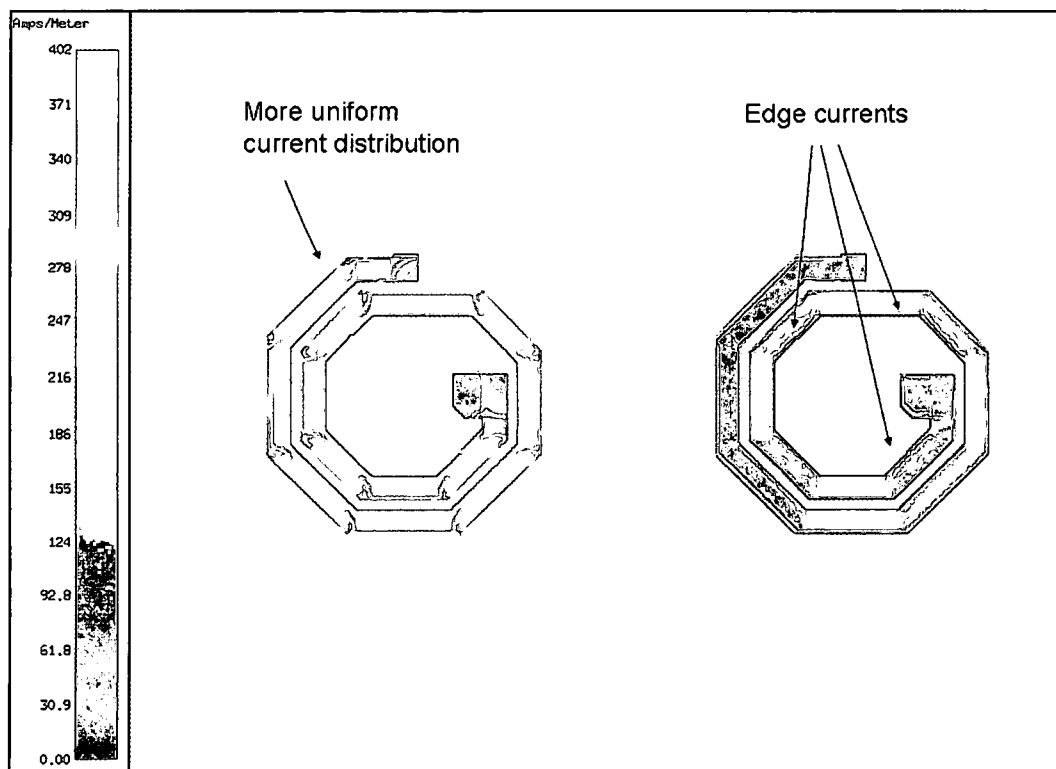


Figure 3.8: The simulated current distribution of a 1.75 turn SiGe inductor

CHAPTER IV

Design

The X-Band VGSA amplifier is critical to RF RX/EX systems due to its ability to digitally compensate for wafer to wafer process variation and gain slope in a RX/EX system. As SiGe and Si mask cost continue to increase, the importance of first pass success is critical to the development of enabling technology. The proposed VGSA would be capable of yielding more functional amplifiers across a wafer due to the amplifiers' tuning capability based on system requirements to adaptively change its performance characteristics. Also, when the VGSA is placed in an integrated RX/EX chain where it would be virtually impossible for rework or manual tuning, the VGSA could compensate for gain performance and gain variation generated by each sub-cell of the RX/EX. This is extremely useful when trying to maximize the overall system performance of an RX/EX system. The additional incorporation of digital control logic offered in the BiCMOS SiGe technology increases the overall functionality of the VGSA and the interface without compromising performance. Figure 4.1 shows the notional system block diagram for the VGSA. This illustrates the two control options available, one for gain compensation and the other for slope control.

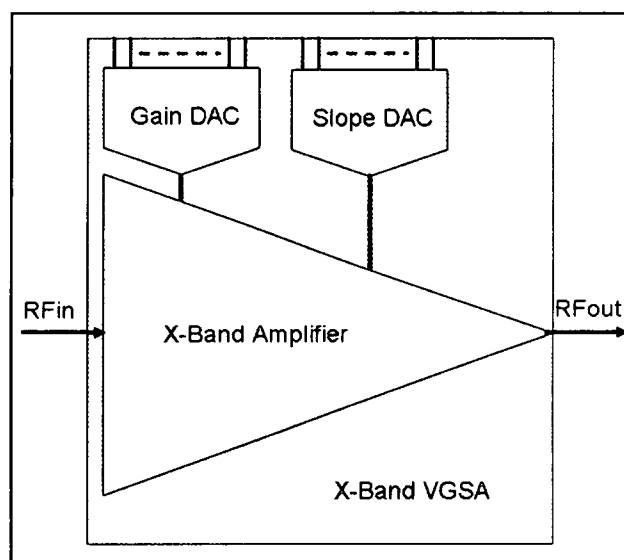


Figure 4.1: Block diagram of VGSA

4.1 X-Band Amplifier Design

The overall architecture of the X-Band Amplifier requires the use of both series and shunt feedback, as described by [38], elements in combination with a $0.13\ \mu\text{m}$ emitter width and $18\ \mu\text{m}$ emitter length device. The input and output matching networks are designed to match to $50\ \Omega$ impedance for on-wafer characterization as a sub-cell of an integrated chipset. Bias networks were also designed to provide the device with the desired base and collector currents. Additionally, this amplifier employs an active shunt feedback network used for slope adjustment.

The RF transistor selected is a $0.13\ \mu\text{m} \times 18\ \mu\text{m}$ single finger device based on the IV curves shown in Fig. 4.2, and the smith chart, Fig. 4.3. The IV curves for the HBT were generated by sweeping the collector voltage and stepping the base current and then plotting the collector current versus the collector voltage. The operating point for the device was set at $1.5\ \text{V}$ collector to

emitter voltage and a base current of 43 μA producing a collector current of 14 mA. The smith chart is generated using the 43 μA base current resulting in 14 mA collector current. Fig. 4.3 shows that as the gain circles value increases, the circles move toward the outside of the smith chart and towards the instability region. Additionally, Fig. 4.3 highlights the input and output impedance points and their conjugates. This is important to note since conjugate matching was employed to match the impedance of the transistor to 50 Ohms [38].

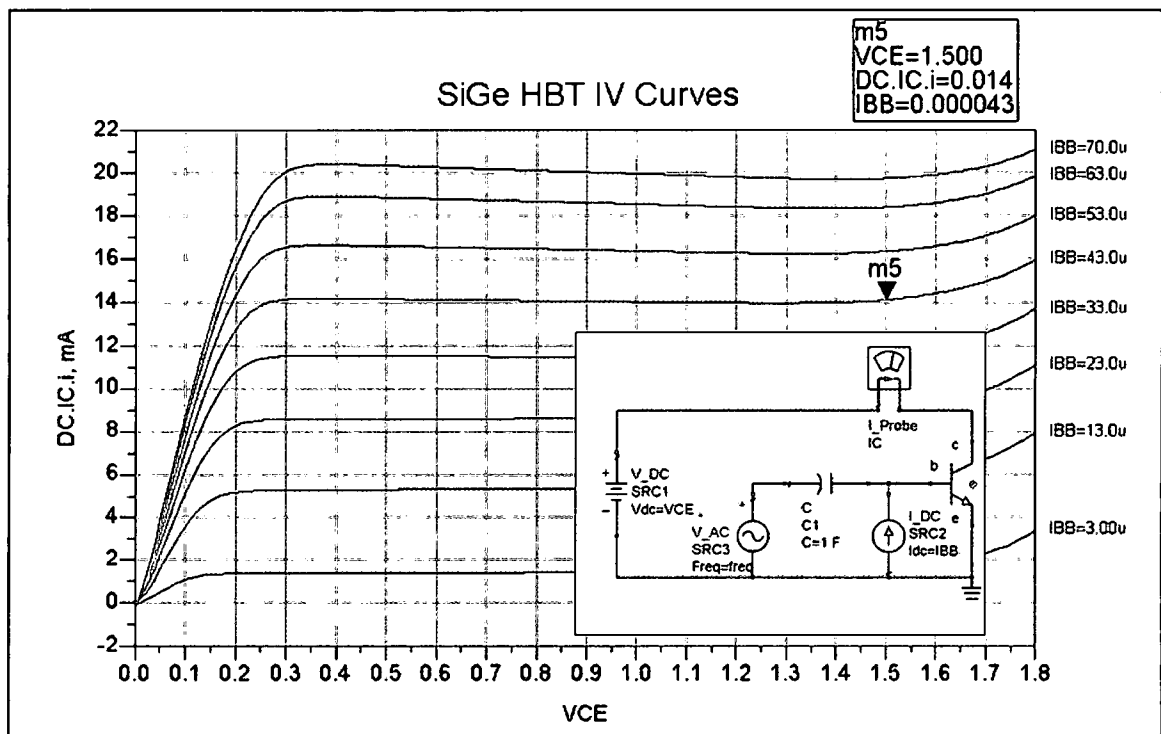


Figure 4.2: IV curves for a single finger $0.13 \mu\text{m} \times 18.0 \mu\text{m}$ device

this resistance from affecting the DC biasing of the circuit two capacitive elements are added for isolation. Now the input and output stability circles are significantly outside the smith chart. Also, both the input and output conjugates are nearly 50 Ohm making conjugate matching easily achievable. The maximum stable gain (MSG) from a potentially unstable device is plotted in Fig. 4.6. As illustrated in the plot, the amount of feedback added to the device does impact the overall gain performance of the amplifier, but improves circuit stability.

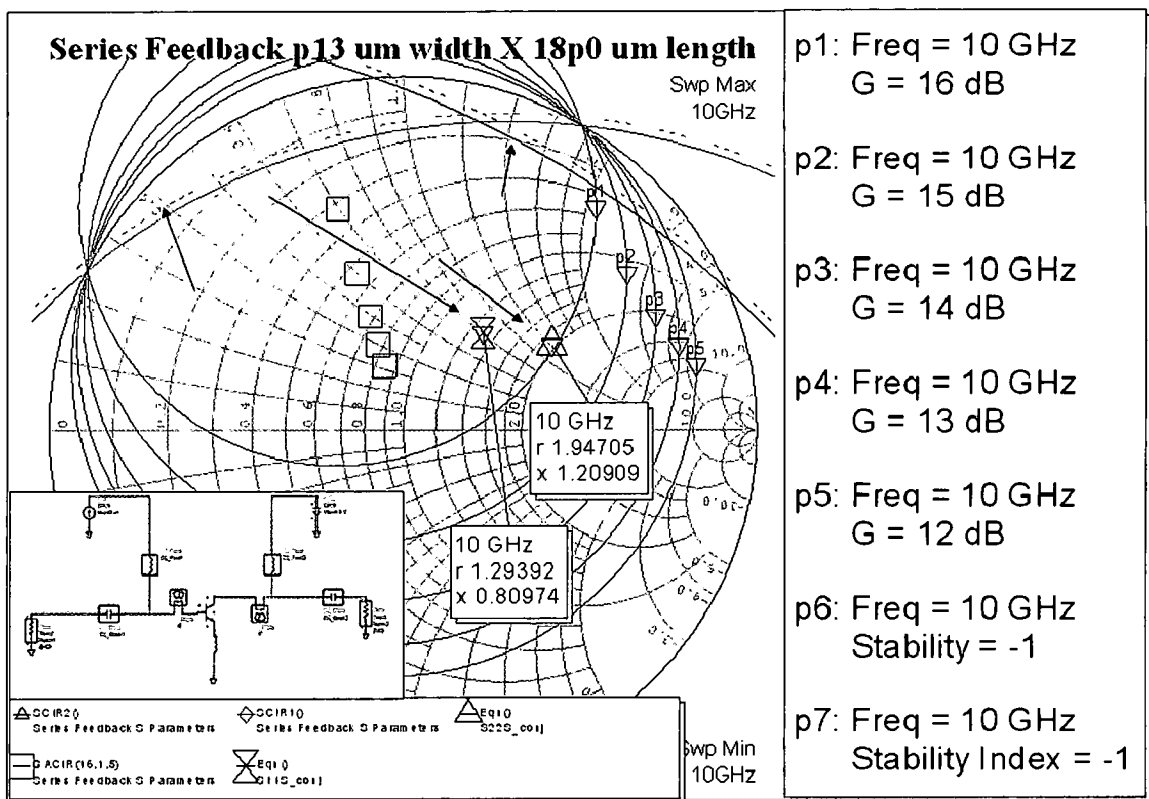


Figure 4.4: Smith chart of the series feedback for a 0.13 μm emitter width 18.0 μm emitter length device

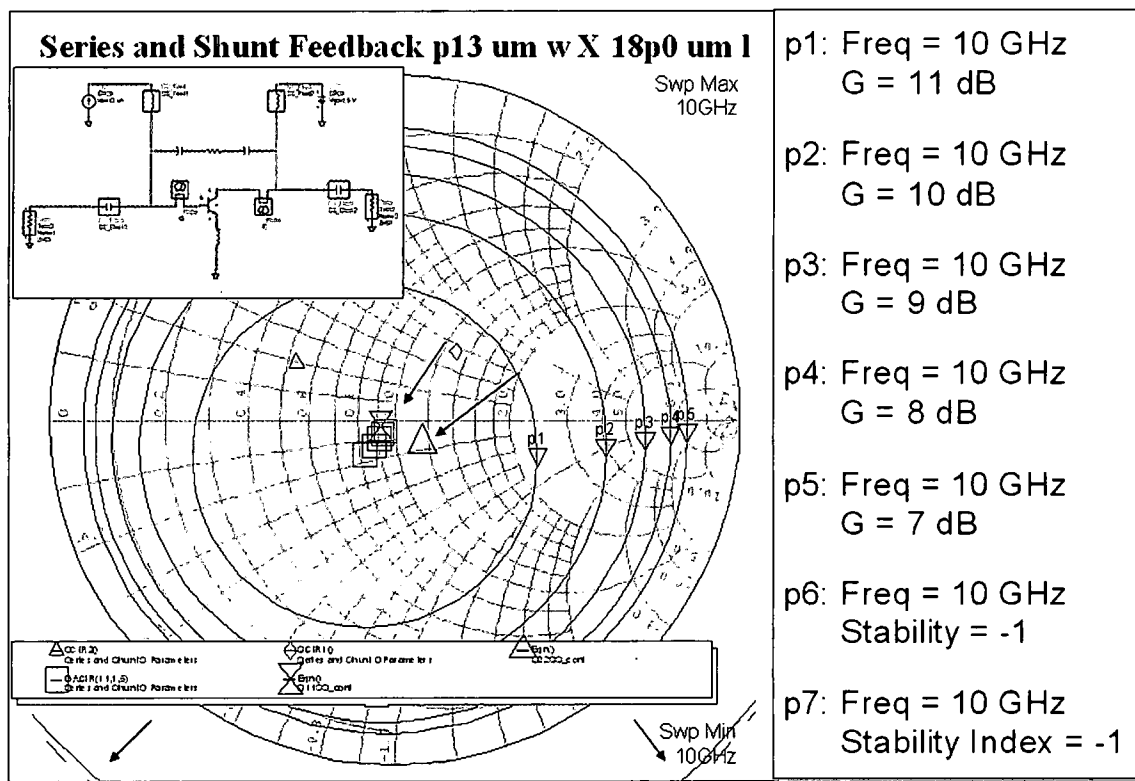


Figure 4.5: Smith chart of the series/shunt feedback for a 0.13 μm emitter width 18.0 μm emitter length device

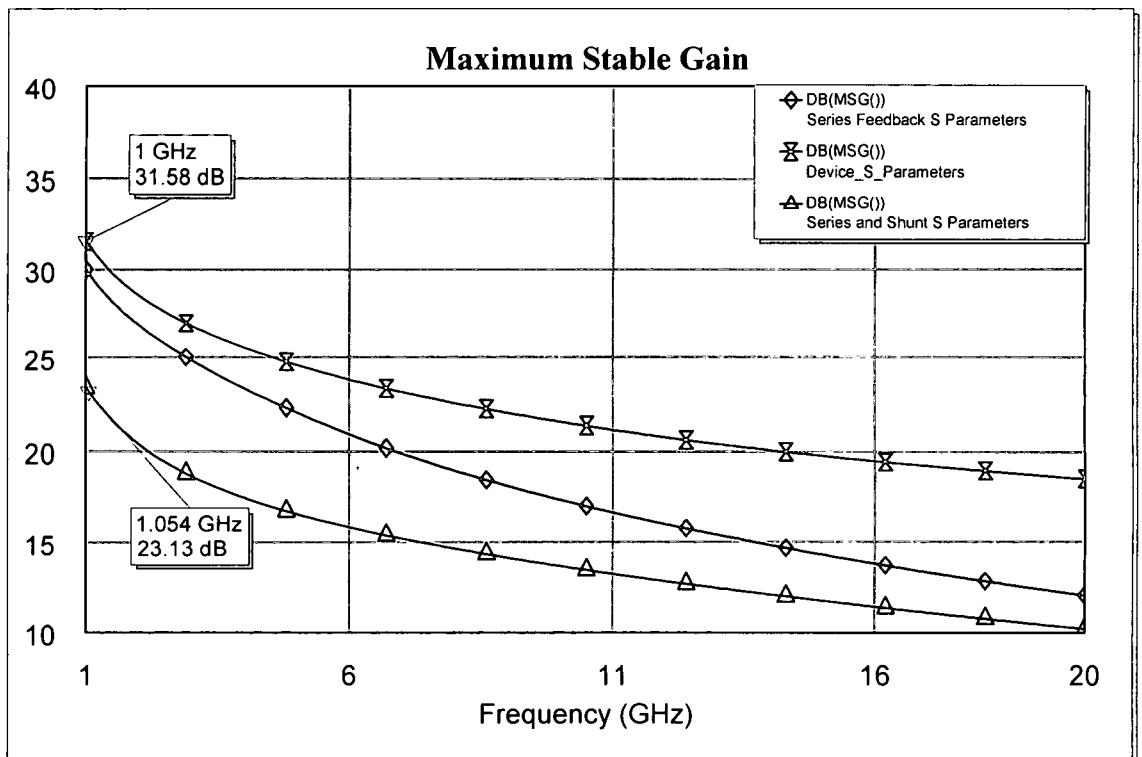


Figure 4.6 Maximum Stable Gain of the SiGe HBT

The input and output matching networks are designed with the intent to suppress out of band gain while matching the input and output terminals of the device to 50 Ohms. Additionally, from Fig. 4.6. the SiGe devices have gain of 32-23 dB at 1 GHz which is outside the band of interest. The chosen input matching network has a high pass characteristic shown in Fig. 4.7, which helps to suppress the excess gain at 1 GHz. The network consists of a Tee configuration consisting of series capacitors and a shunt inductor/capacitor as seen in Fig. 4.8. The simulated insertion loss of this network is 1.5 dB at 10 GHz and input and output matching is -14 dB and -15 dB respectively. The output matching network has a band pass response, as shown in Fig. 4.9. This network consists of two pi networks with shunt capacitors and series inductors and a

series capacitor placed between the two circuits for DC blocking, Fig. 4.10. Again, the output matching network helps to filter out both high and low frequencies from the band of interest. The band pass filter has -18 dB of rejection at 1 GHz, 2 dB insertion loss at 10 GHz, -14 dB input and -12 dB output matching at 10GHz.

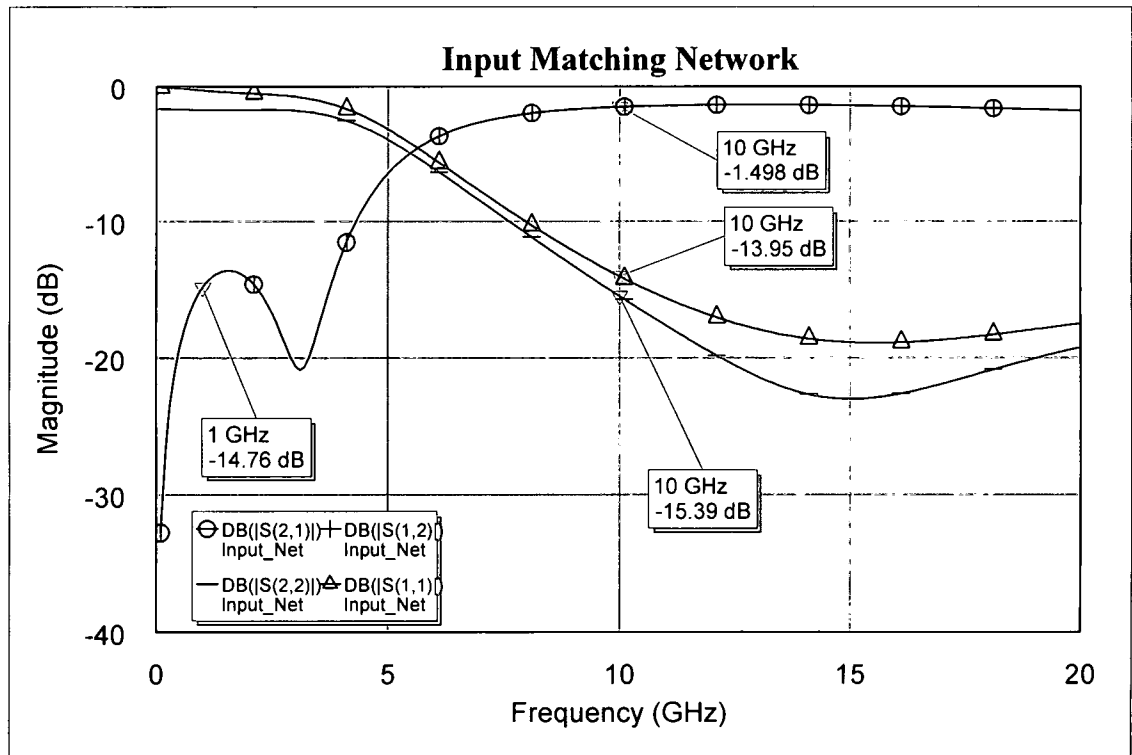


Figure 4.7: Simulated magnitude performance of the input matching network

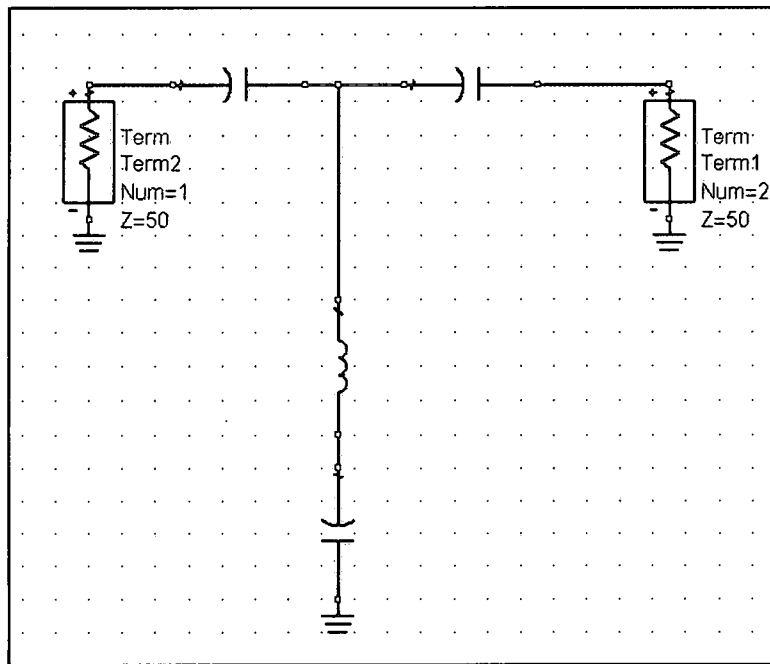


Figure 4.8: Ideal lumped element schematic of the input matching network

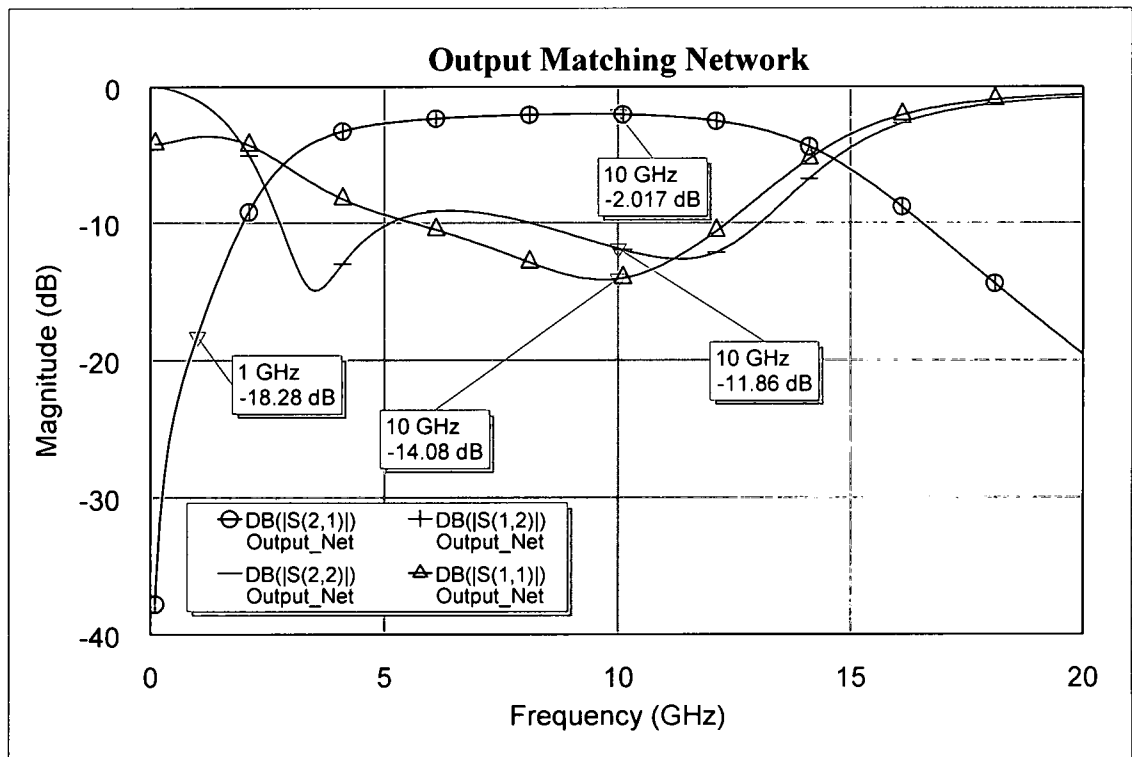


Figure 4.9: Simulated magnitude response of the output matching network

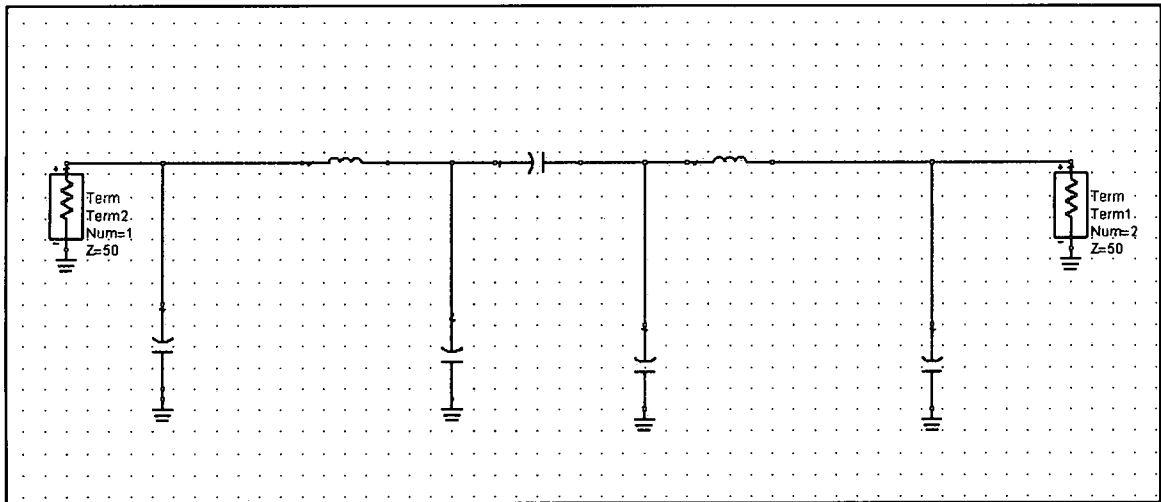


Figure 4.10: Ideal lumped element schematic of the output matching network

The tuning capability of the amplifier comes from two elements. The first is the shunt feedback using a resistor. This feedback resistor element can be substituted with an active FET device operating in the resistive region. Since the feedback network is already DC isolated by the surrounding capacitors, this makes it an ideal place for insertion. Fig. 4.11 shows an ideal implementation of this device. The additional large-valued resistors of 10K Ohm provides a high RF impedance while allowing easy biasing of the FET device with out impacting the RF performance. The ideal schematic also highlights the importance of defining the source and drain nodes of the FET. With one side of the FET connected to ground, the drain to source and gate to source voltages are clearly defined.

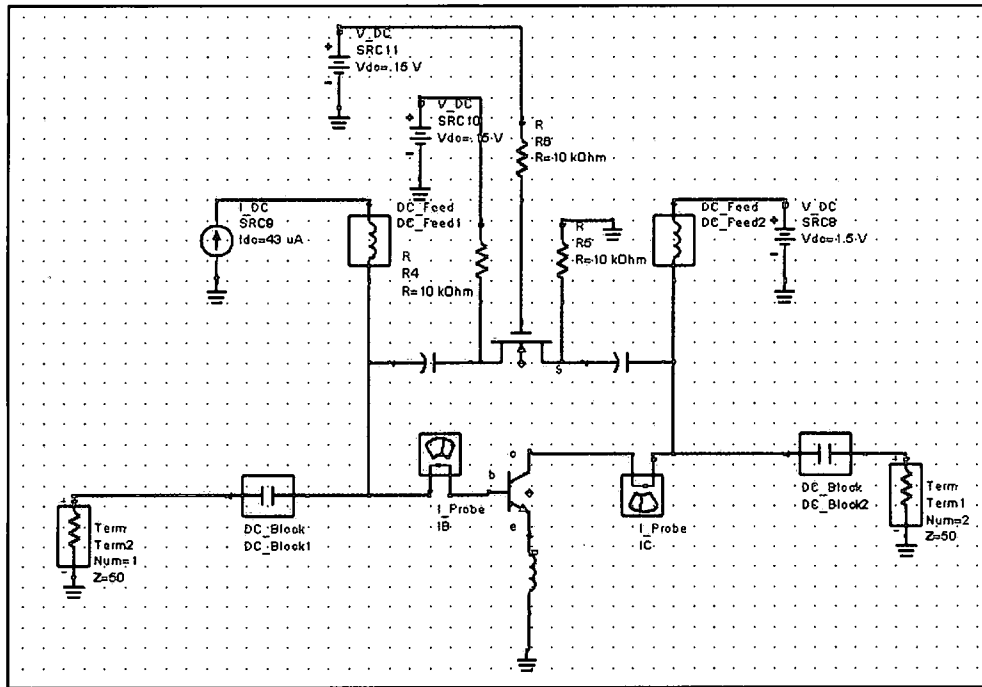


Figure 4.11: Ideal lumped element schematic of the FET resistive network

Since the FET replaced a known valued resistance of 300 Ohms, it was necessary to identify a device size to produce this value of resistance. Toward that end, the FET IV curves were modeled and the device size was optimized to a nominal resistance of 300 Ohms. This was achieved at the center of the tuning range shown in Fig. 4.12. The final selection for the FET device was a 4.5 μm , wide, by 0.24 μm , long, device with 3 fingers. The drain to source voltage was fixed at 0.15 V and the gate voltage was stepped from 0.40 V to 1.10 V. Using formula 4.1 one could calculate the given resistance of the FET at each gate voltage shown in Table 4.1

$$V = IR \Rightarrow R = \frac{V}{I} \quad (4.1)$$

where:

V : Voltage [Volts]

I : Current [Amps]

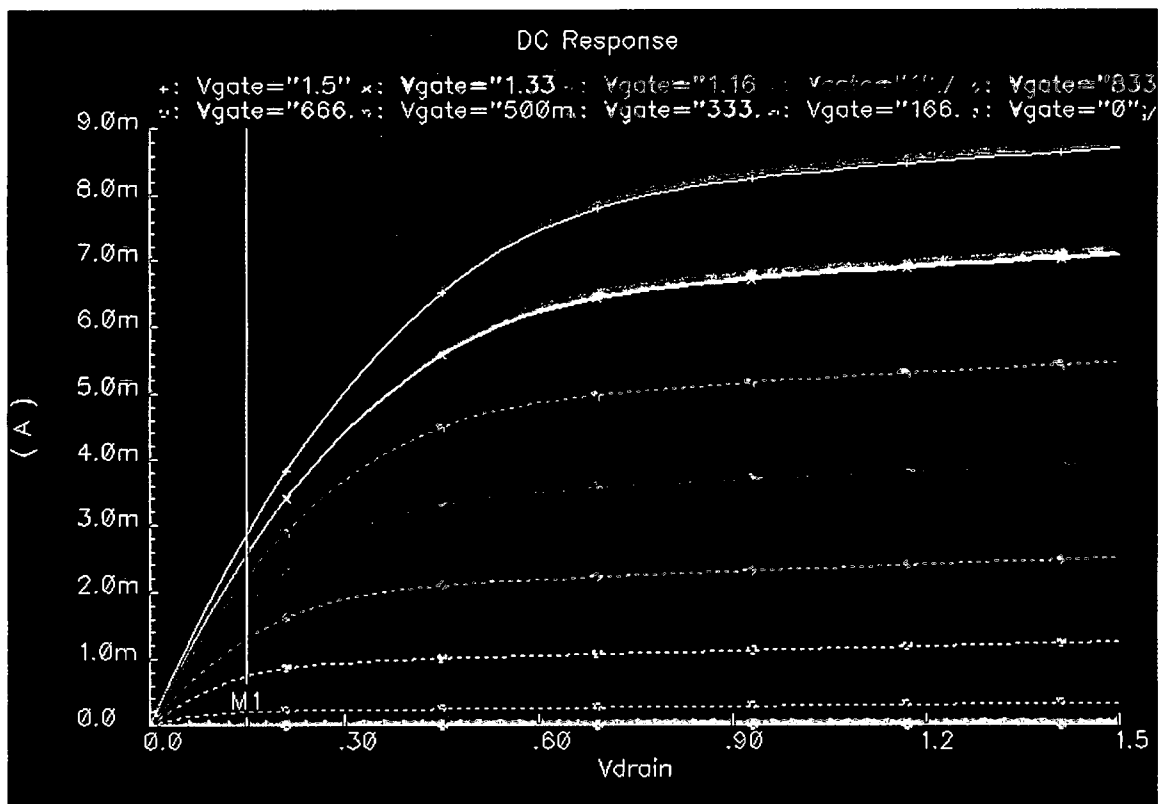


Figure 4.12: IV curves for feedback FET.

Table 4.1: Calculated Resistance of the FET

Gate-Source Voltage (V)	Drain-Source Voltage (V)	Resistance (Ω)
0.40	0.15	2675
0.48	0.15	1190
0.56	0.15	691
0.63	0.15	467
0.71	0.15	348
0.79	0.15	277
0.87	0.15	232
0.94	0.15	202
1.10	0.15	<200

Once appropriately sized a transient analysis was used to verify that the RF performance did not change the DC resistance value over time shown in Fig.

4.13. The incoming RF signal (pink) produces two sine waves which represent the output associated with going through the resistor (red) and FET (brown). The simulation shows that the output sine wave does not change when using a FET vs. a resistor in the feedback path.

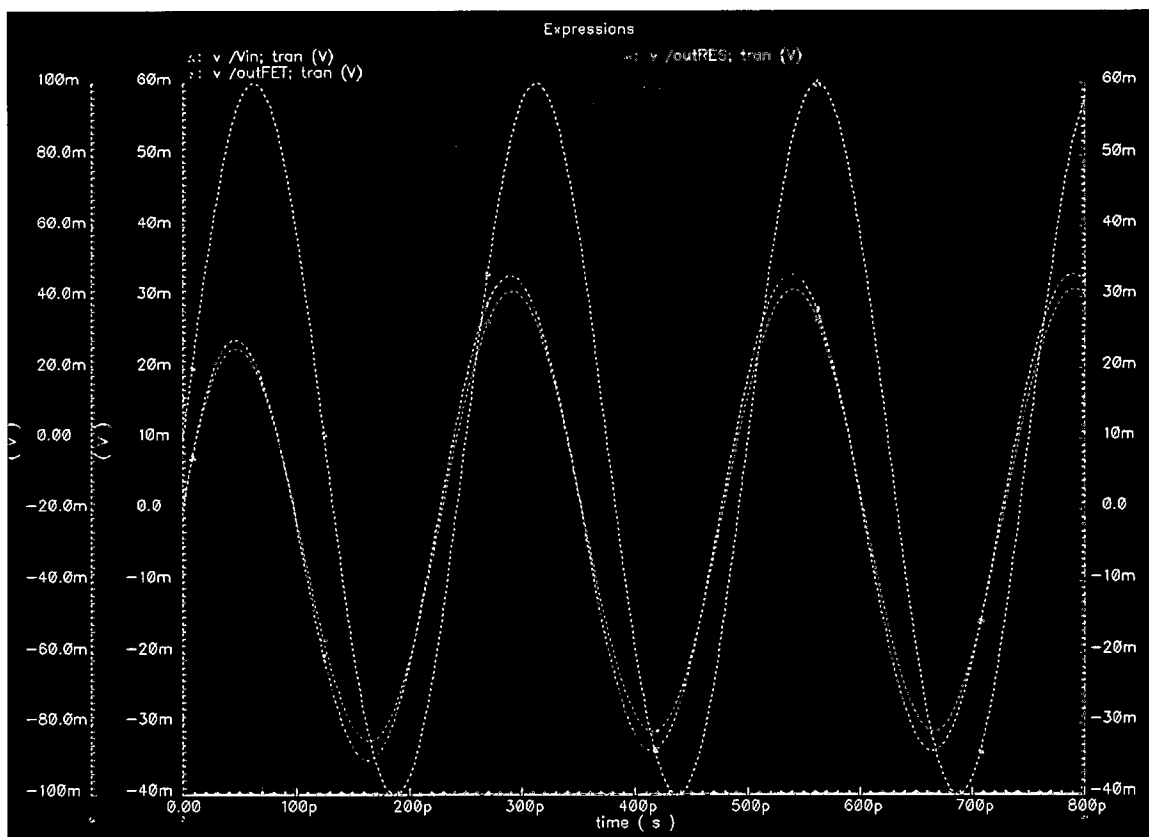


Figure 4.13: Transient analysis of FET vs. ideal resistor.

4.2 Current DAC

The second tuning capability appears at the base biasing terminal for the RF transistor. A current steering DAC is attached to this network and provides a secondary resistive path and therefore steers current away from the active device. This 3-bit current steering DAC is comprised primarily weighted resistors utilizing the HBT's as switches. Fig. 4.14 illustrates the simple 3-bit DAC utilized

in the amplifier design. The resistors were chosen in a binary weighted fashion, such that they are multiples of 750 Ohms, 1x, 2x and 3x. Additionally from Fig. 4.14, a current mirror was incorporated into the design to provide the correct base biasing to the amplifier and to isolate the current steering DAC from the RF amplifier.

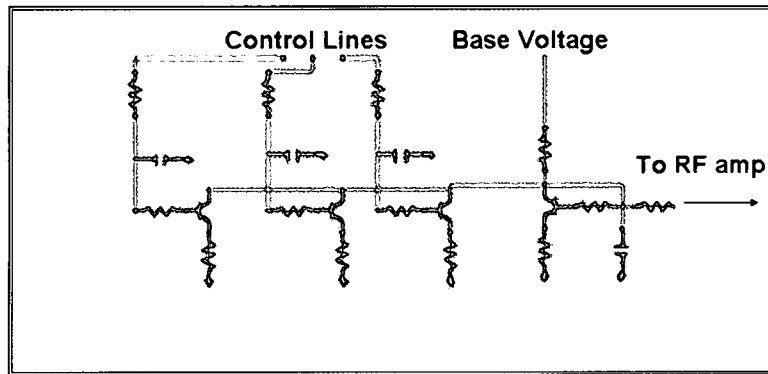


Figure 4.14: Ideal 3-Bit current steering DAC and current mirror

The X-band amplifier combines the input and output matching networks, active feedback network and current steering DAC. Once the ideal lumped element networks were designed to meet the specifications with margin, then they are converted to a realistic design that includes process design kit (PDK) elements and microstrip transmission lines. At these frequencies it is critical to account for all junctions, bends, and tees. The X-band amplifier schematic is shown in Fig. 4.15 identifying the critical networks. The corresponding circuit layout is shown in Fig. 4.16 highlighting the critical networks in the layout. Ground-signal-ground (GSG) pads are provided at the input of the amplifier for RF testing in a 50 Ohm system. For on-wafer characterization, multiple probe configurations were required. For example, it was necessary to use a GSGSG

probe at the output of the amplifier due to the additional drain voltage. The GSGSGSG pad configuration on the top side of the chip is required for the HBT base and collector biases and the gate voltage of the feedback FET. Finally, the gate voltage on the feedback device will be controlled by an external DAC through a bond wire. Due to the small feature sizes and the difficulty to place bond wires in close proximity to each other, the large bondpads and spacing are required for packaging the amplifier. Simulations of varying the base biasing via the current steering DAC and corresponding variation of the resistance value of the feedback FET are shown in Fig. 4.17 and Fig. 4.18, respectively.

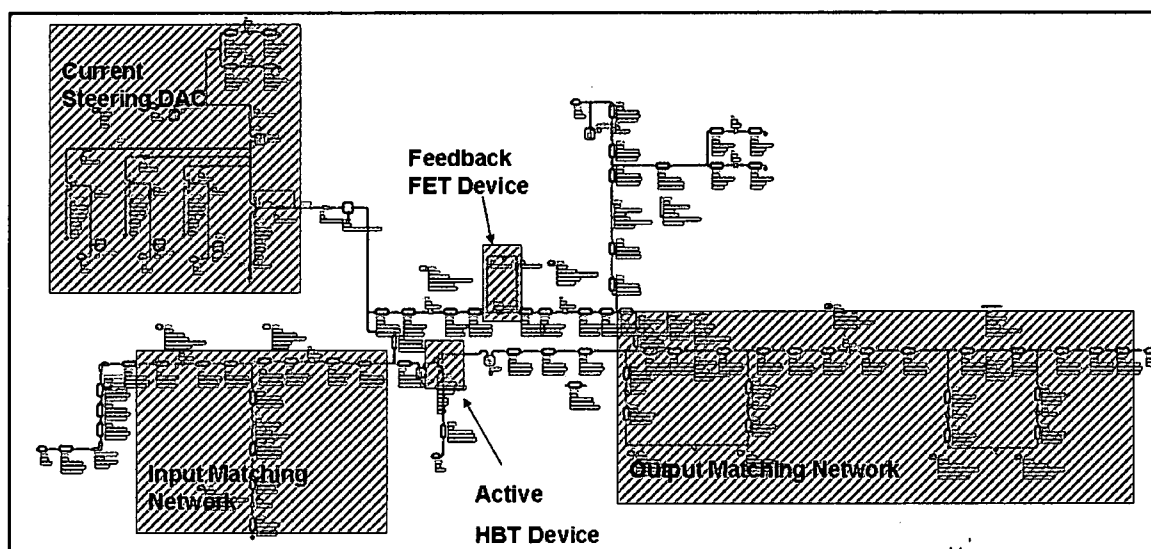


Figure 4.15: Final X-band amplifier schematic (see APPENDIX I A3 for larger picture)

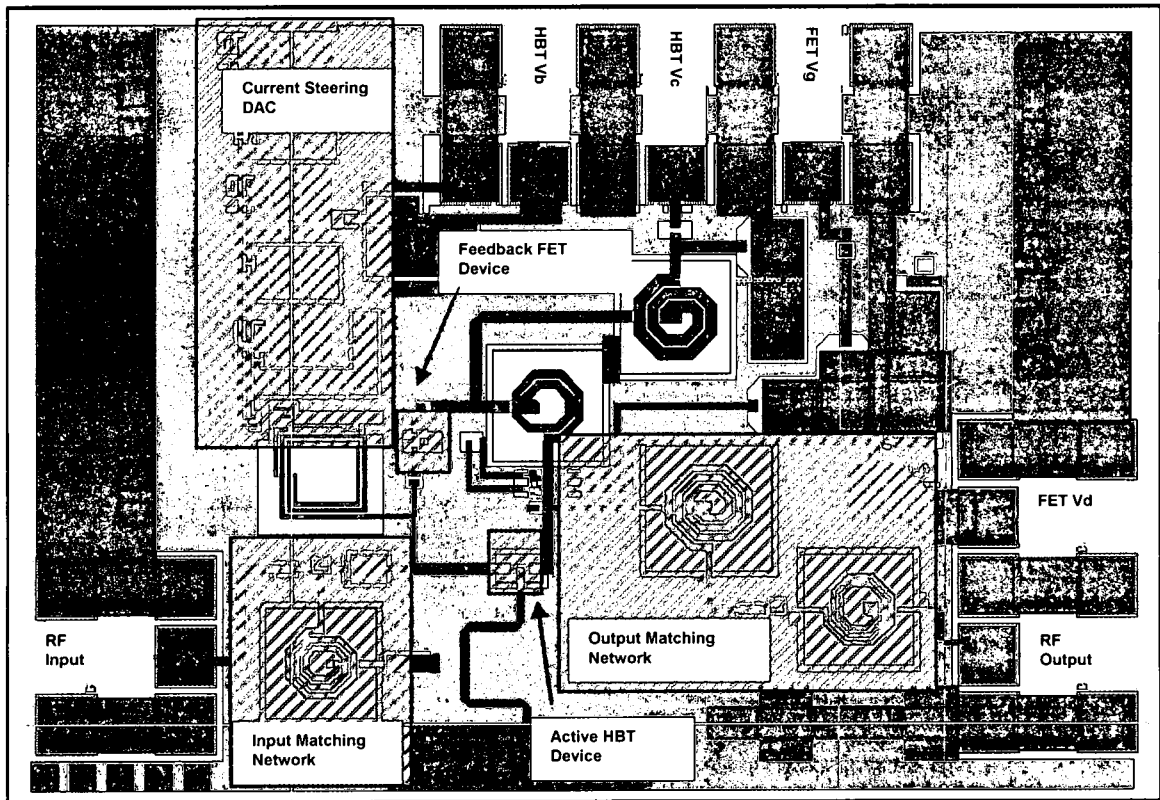


Figure 4.16: Final X-band amplifier layout (2 mm x 1.4 mm)

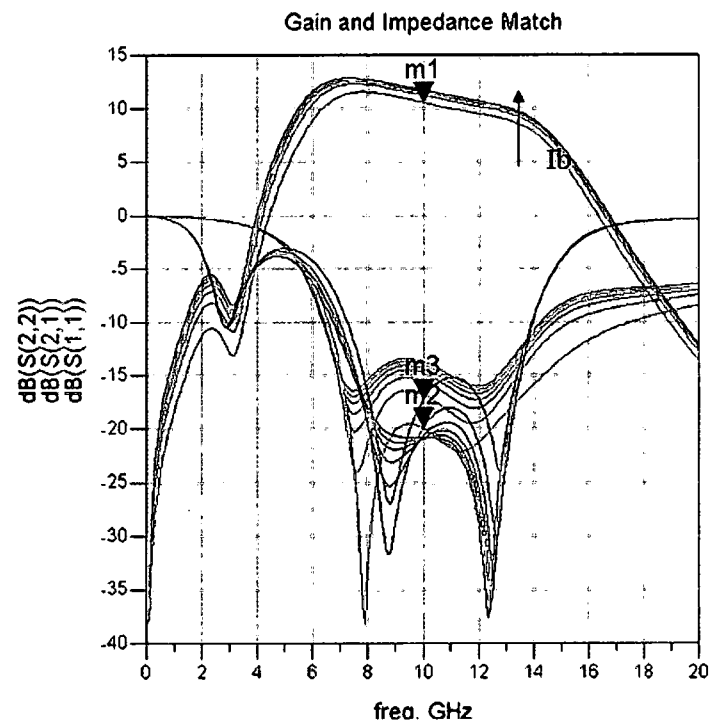


Figure 4.17: Simulated gain, input/output impedance vs. increasing base current

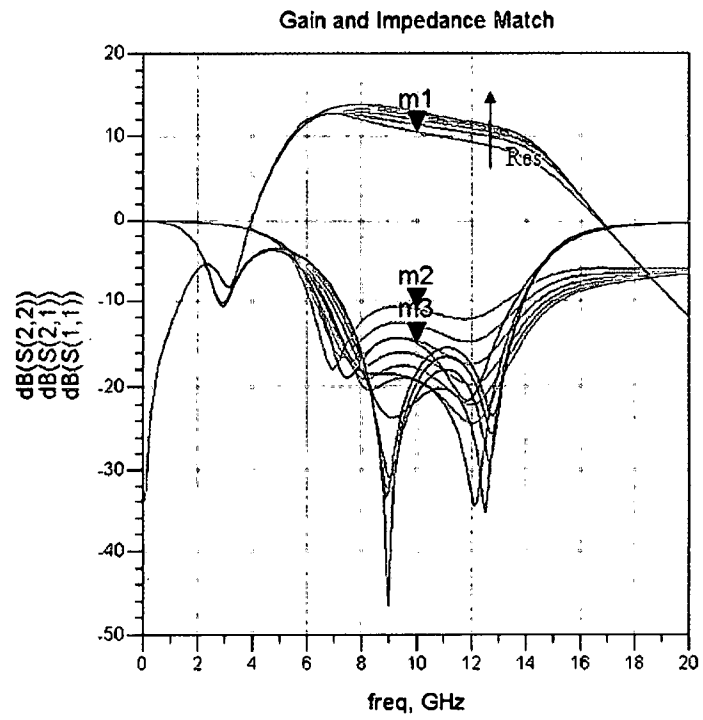


Figure 4.18: Simulated gain, input/output impedance vs. increasing feedback resistance

CHAPTER V

Results

Testing of the RF amplifier is broken into two subsections. The first step is to perform functional verification of the off-the-shelf packaged DAC. The second step is the characterization of the RF amplifier integrated with the DAC placed on an FR4 substrate.

The DAC used to control the feedback resistance is a parallel loaded eight bit R-2R DAC. This will provide 256 usable states. The DAC is able to resolve ~10 mV/bit of resolution based on a 2V reference source. Fig. 5.1 shows the DAC in its die form with B[0:7] as the incoming digital word, CLK1 is the externally applied clock signal, and 5V VDD source. The Vgain voltage output is the equivalent voltage represented by the incoming word. Unable to do on-wafer characterization of the DAC, due to its pad configuration and large number of I/O's, it was attached to an FR4 substrate using die epoxy then wire bonded to the control lines, Fig. 5.2. Once fixed to the board, wires were carefully soldered to the substrate providing easy access to the control lines for testing. A PiC18F series microcontroller having a 10 MIPS CMOS Flash-based architecture with 36 I/O's and a maximum clock speed of 40 MHz was used to test the DAC, Fig. 5.3. This illustration of the development board emphasizes the large amount of input and output I/O that are condensed onto a single board. This enables quick

testing of multiple DACs for functional verification. For this work, two DAC samples were tested using the PiC microcontroller to generate the binary input words and a Tektronix TDS224 digital oscilloscope to capture the voltage output, and critical input transitions. Fig. 5.4 shows the DAC under test with the PiC microcontroller board, power supply, and TDS224 scope. The results of the two samples tested are shown in table 5.5. An example of the DAC's output on the TDS224 is shown in Fig. 5.6 where a transition from the 0th state to the 128th state has occurred.

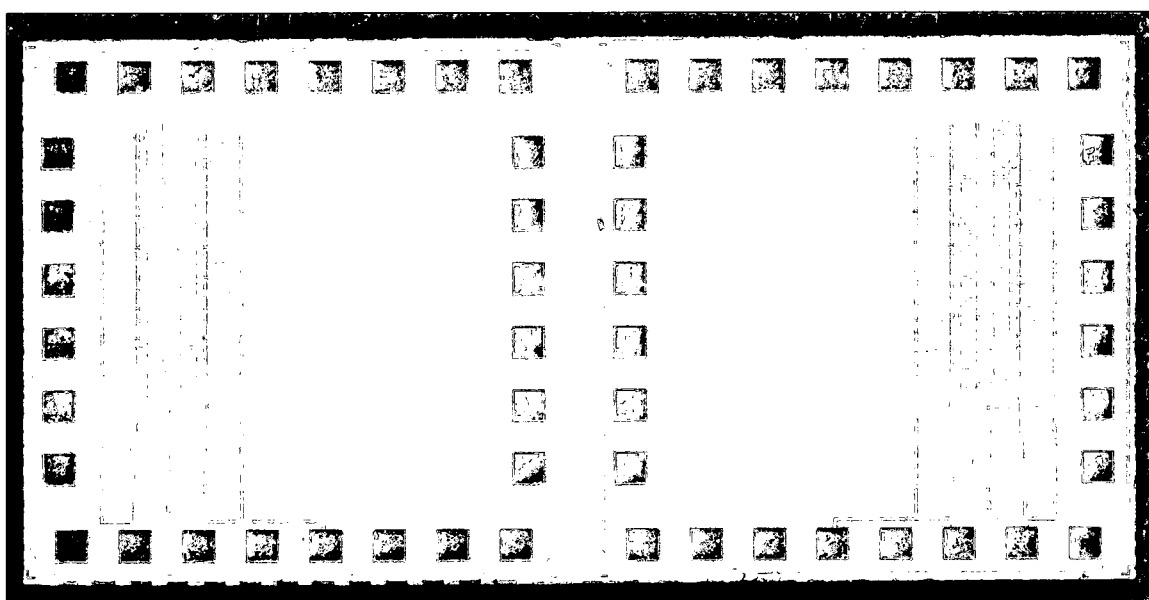


Figure 5.1: DAC used for feedback resistor control

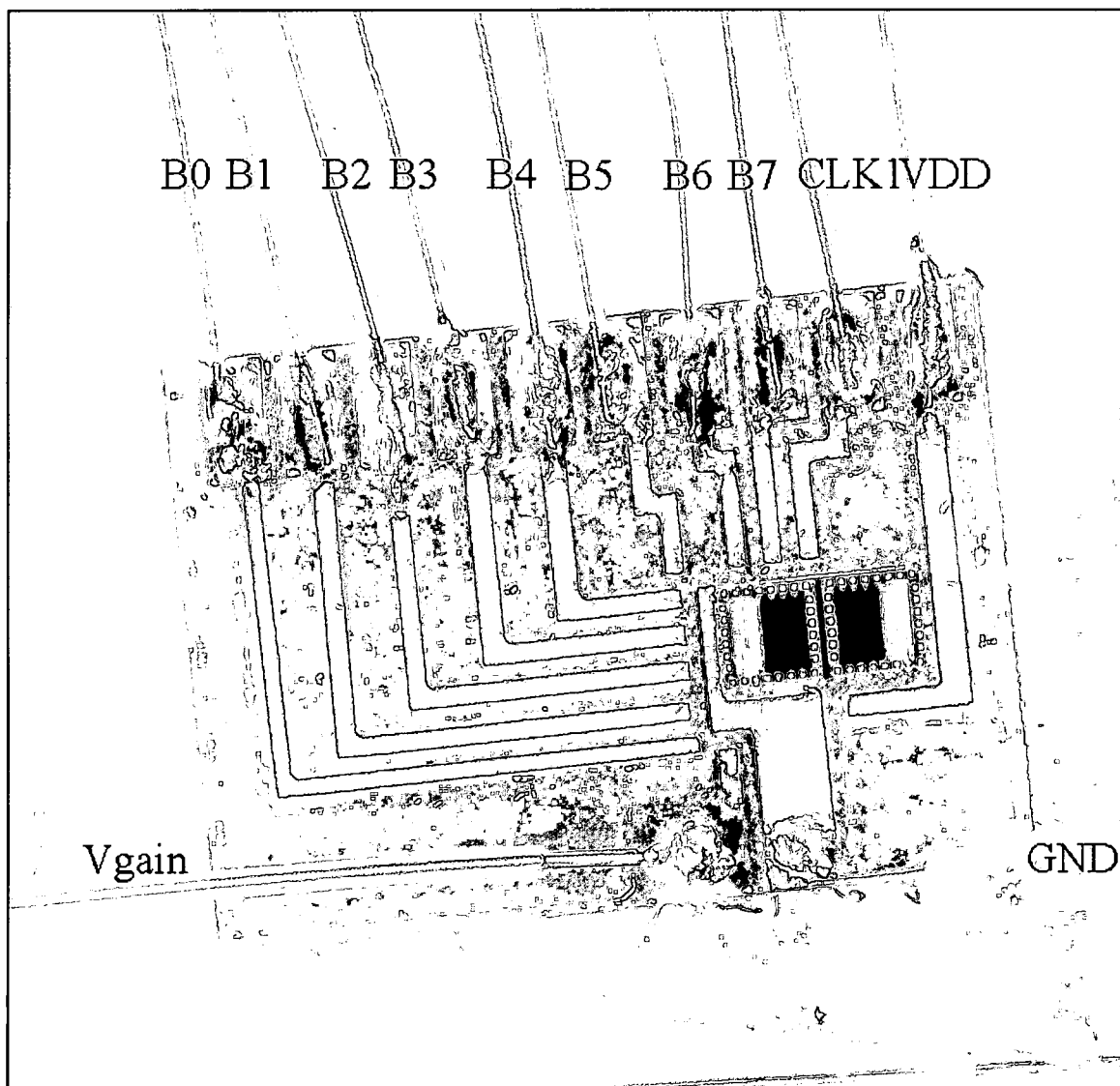


Figure 5.2: DAC attached to FR4 substrate (12.7 mm x 9.5 2mm)

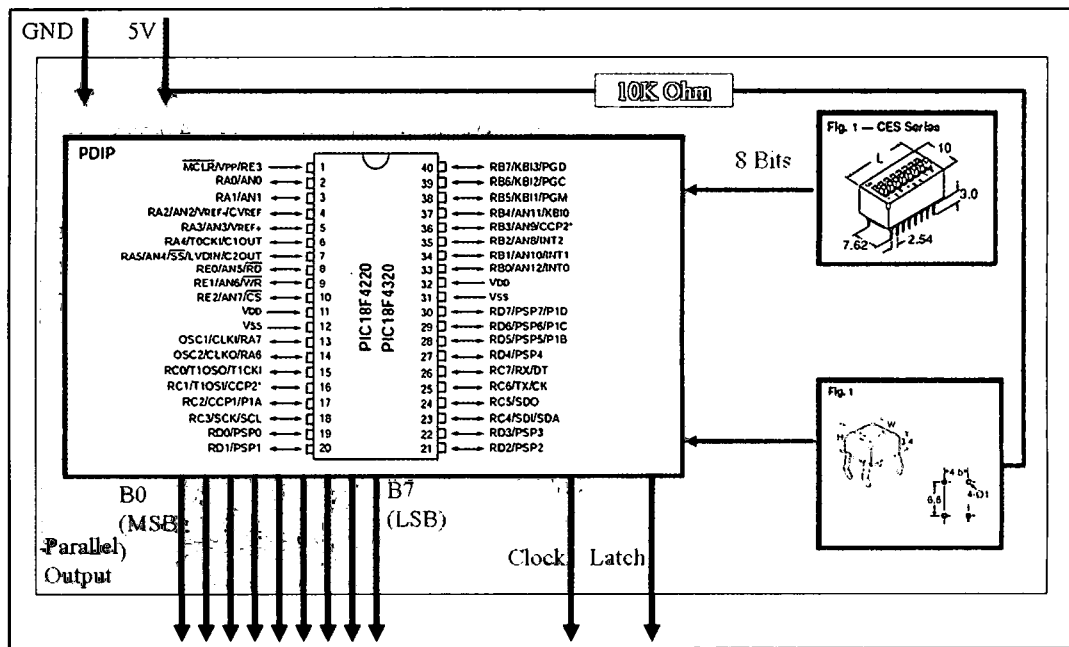


Figure 5.3: Developed PiC microcontroller board

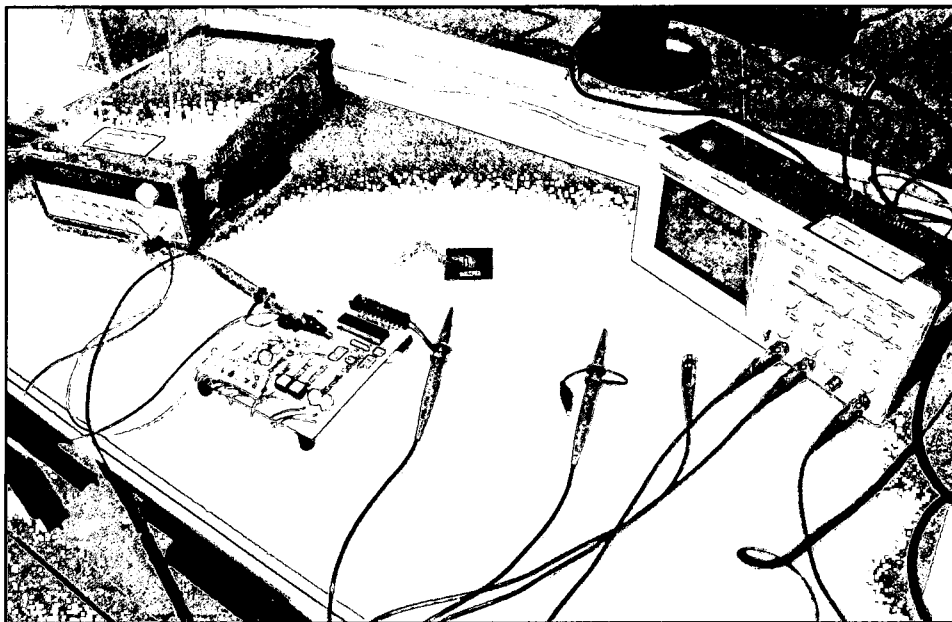


Figure 5.4: DAC with PiC microcontroller board, power supply and TDS224 oscilloscope

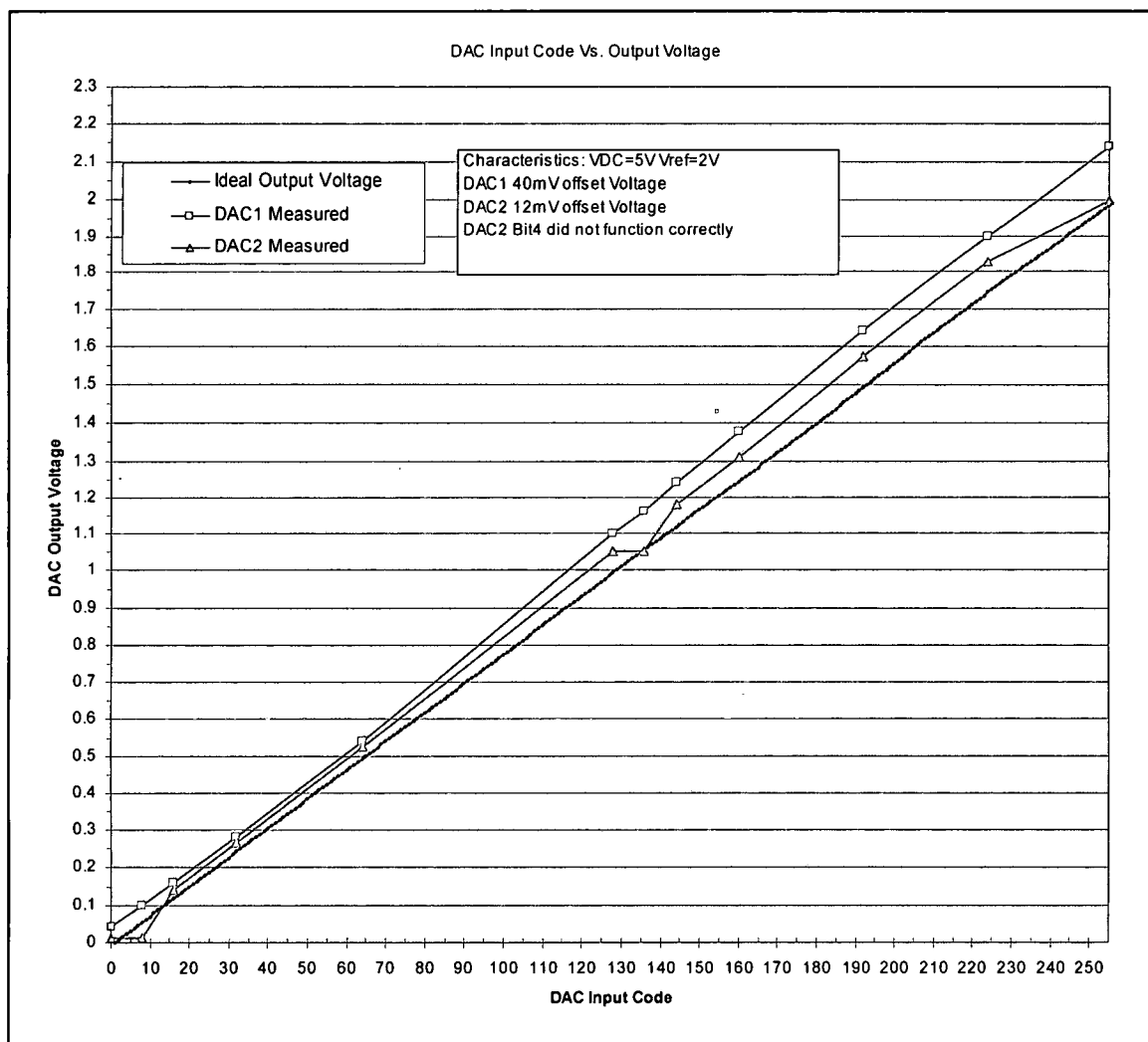


Figure 5.5: Measured DAC results compared to an ideal DAC

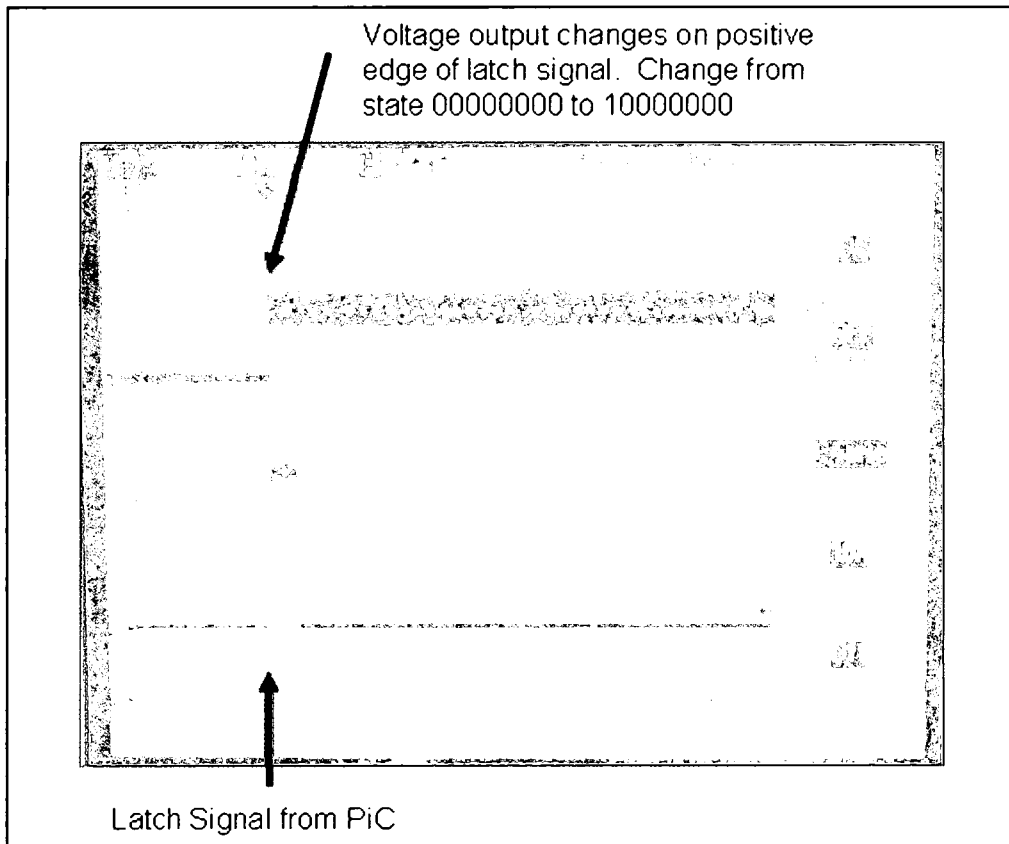


Figure 5.6: DAC transition from the 0th state to 127th state

Once the DAC was functionally verified it was integrated with the X-band RF amplifier. The X-band amplifier and DAC combination on the FR4 substrate is shown in Fig. 5.7. Here the digital words A[0:2] controls the current steering DAC, B[0:7] controls the DAC, CLK1 latches B[0:7] into the DAC, Vb and Vc are required voltages for the RF amplifier, and Vds sets the drain to source voltage of the feedback FET. The board dimensions are 12.70 x 19.05 mm. Using a similar procedure, a PiC microcontroller board was used for the DAC stimulus while RF stimulus was provided through an 8720 Network analyzer. Fig. 5.8 shows the photograph of the test setup used for characterization. Three additional voltage sources were needed to provide stimulus to the integrated

current steering DAC.

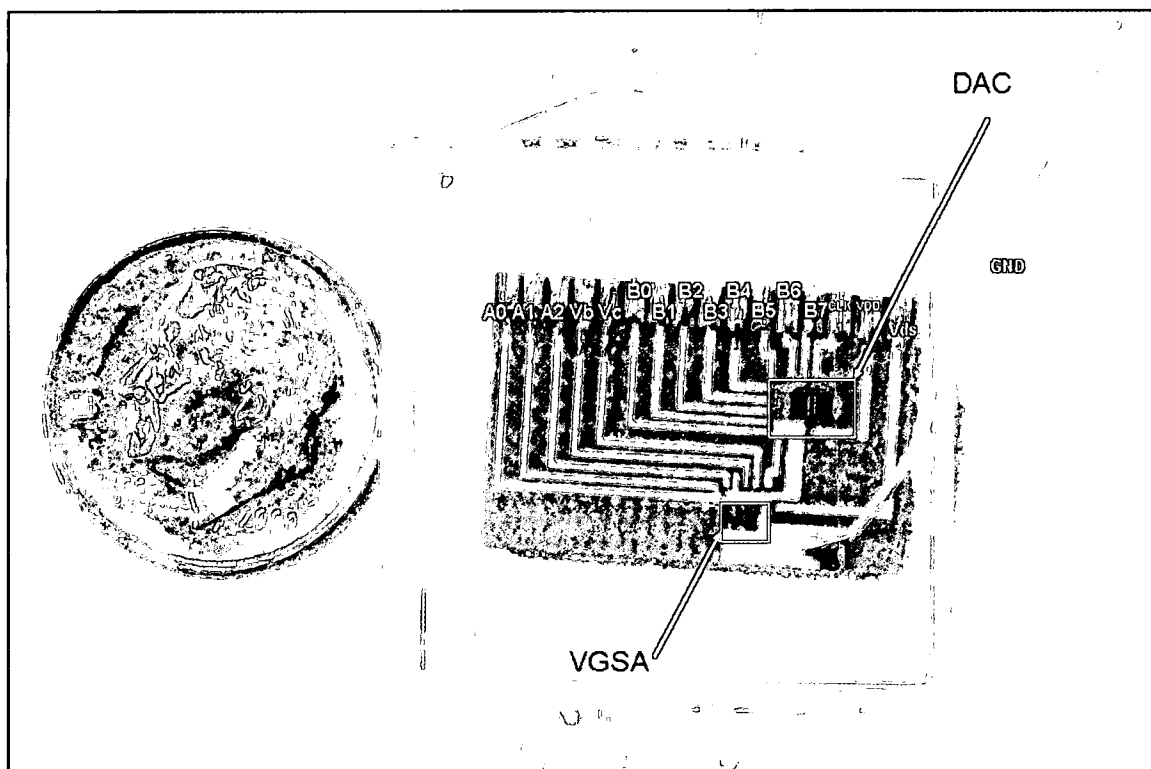


Figure 5.7: X-band amplifier and DAC combination (12.70 mm x 19.05 mm)

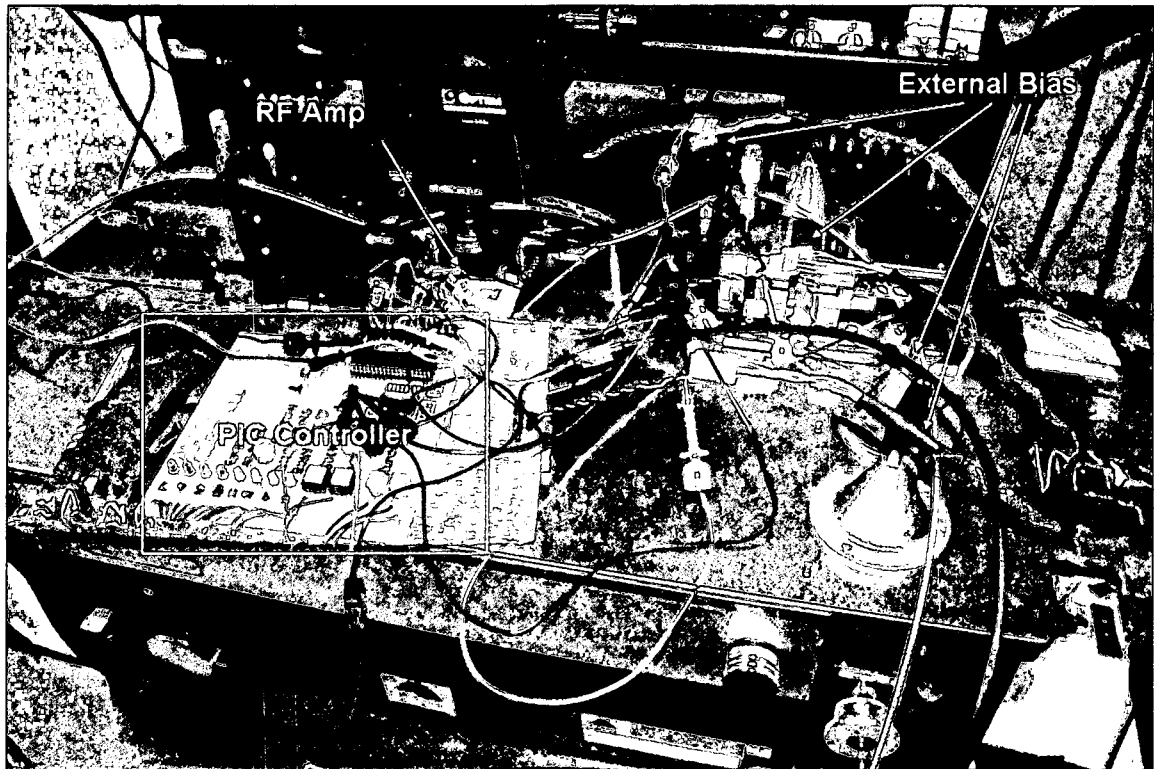


Figure 5.8: X-band amplifier and DAC combination under test

The VGSA measured results of the input and output impedances, S_{11} and S_{22} , are shown in Fig. 5.9 and Fig. 5.10 respectively. These plots show the multiple transitions of the VGSA with the input word to the DAC being altered for each transition. The current steering portion is held constant for these measurements. In the X-Band region of operation both the input and output exhibit better than -10 dB. The gain of the VGSA is shown in Fig. 5.11 and Fig. 5.12, where it ranges from 6.07 dB to 7.97 dB. Fig. 5.12 is the measured gain focused on the X-Band region of operation.

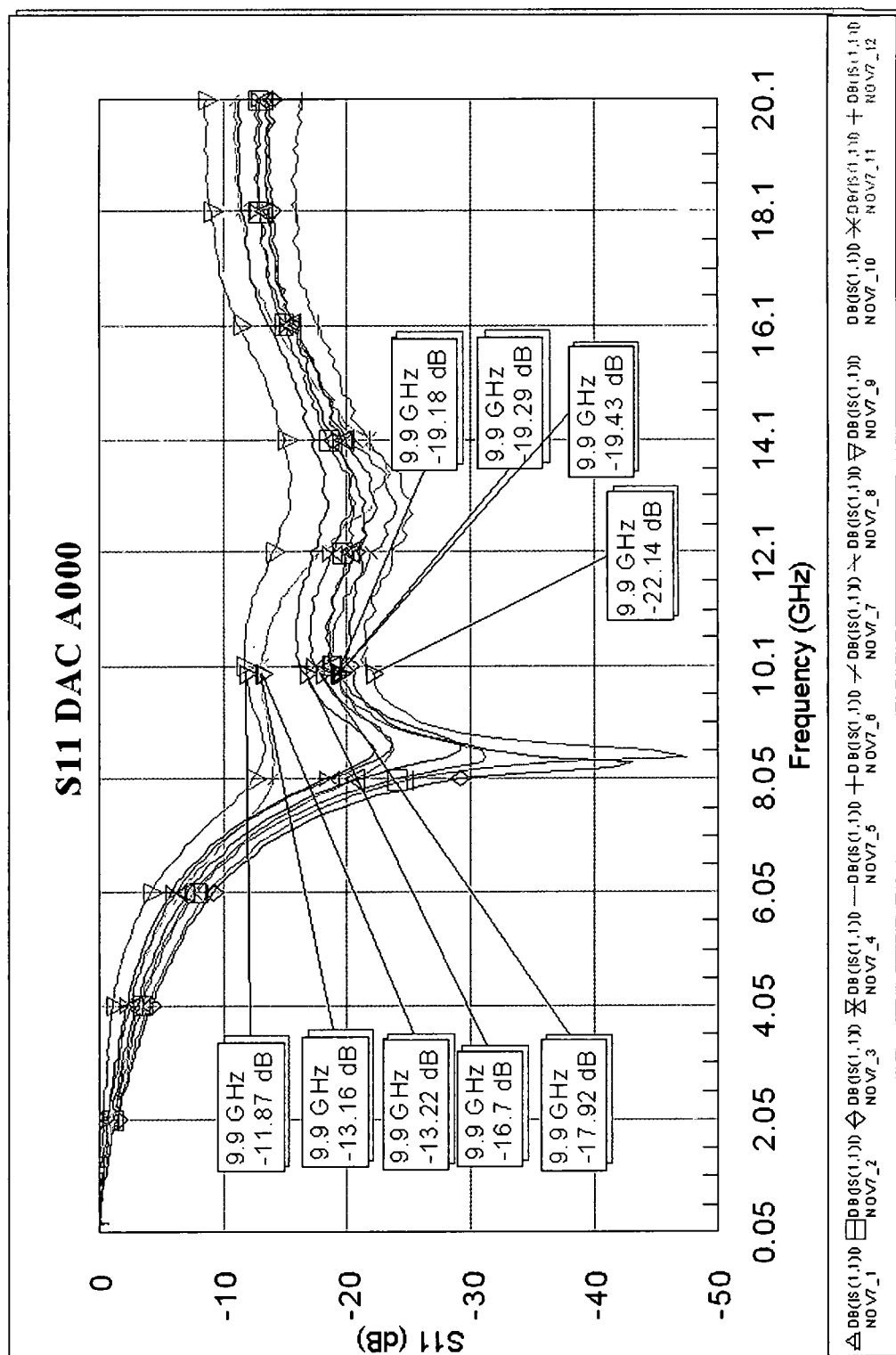


Figure 5.9: S11 Measured results through DAC transitions with Current DAC held constant

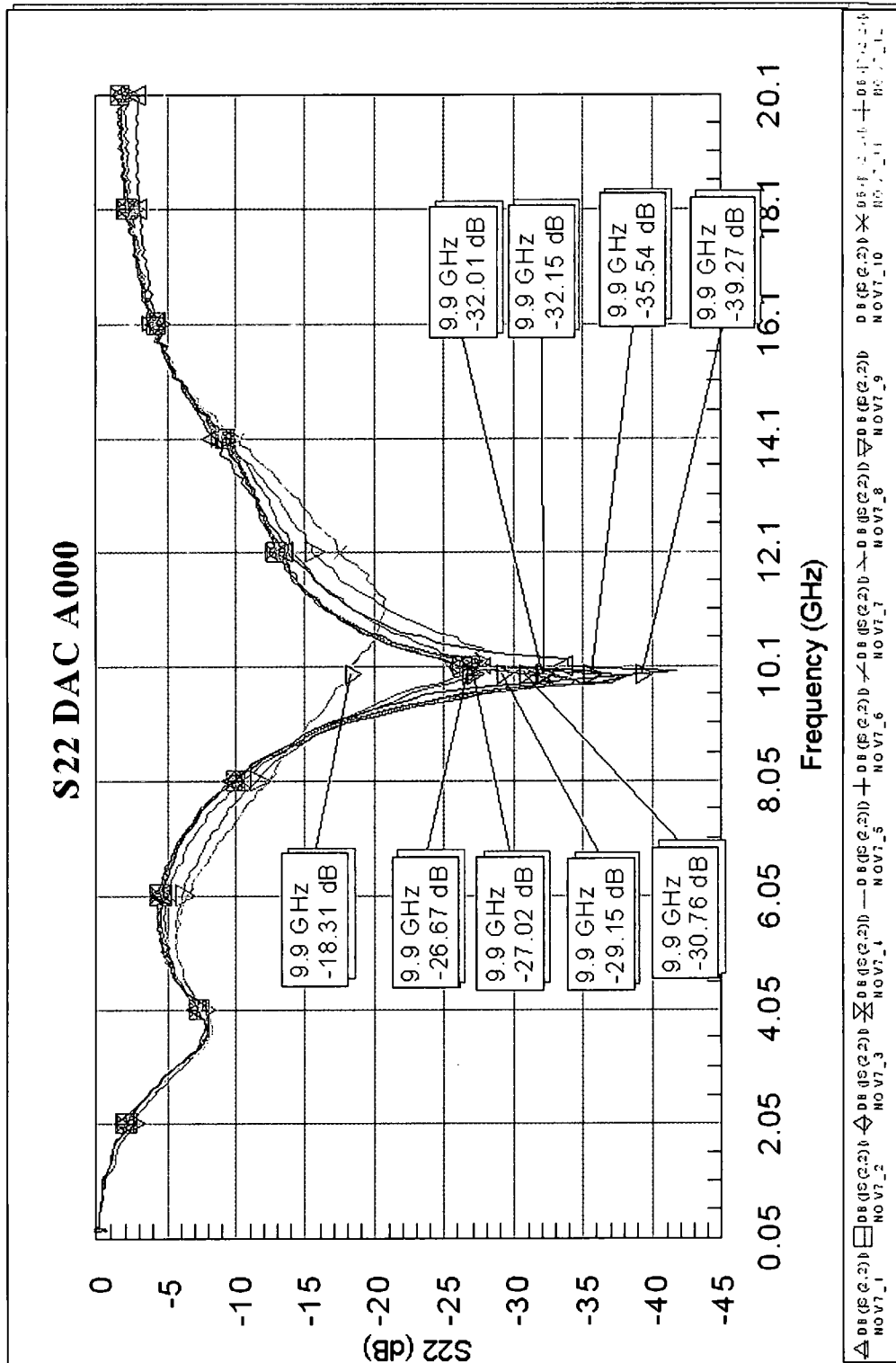


Figure 5.10: S22 Measured results through DAC transitions with Current DAC held constant

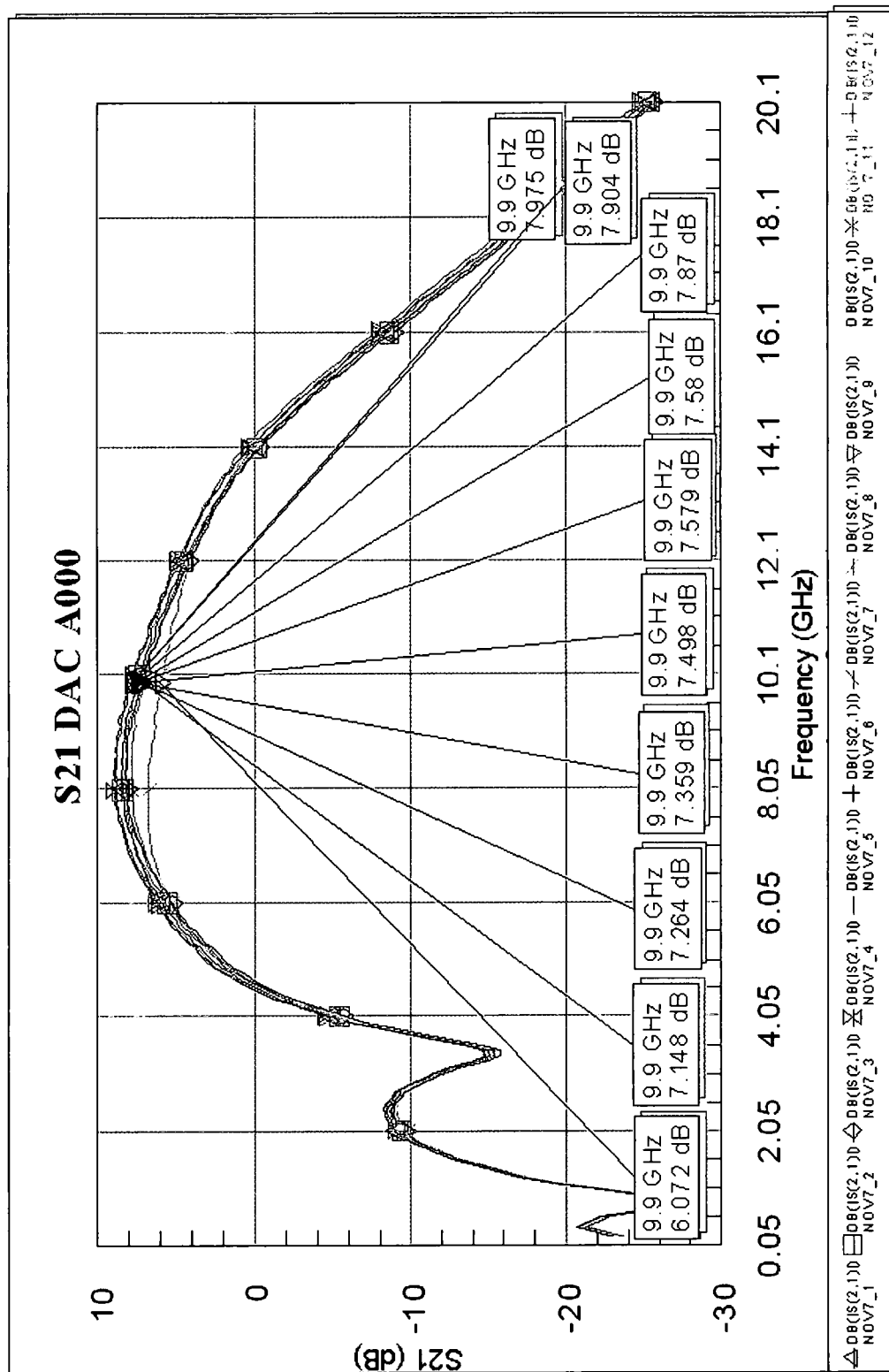


Figure 5.11: S21 Measured results through DAC transitions with Current DAC held constant

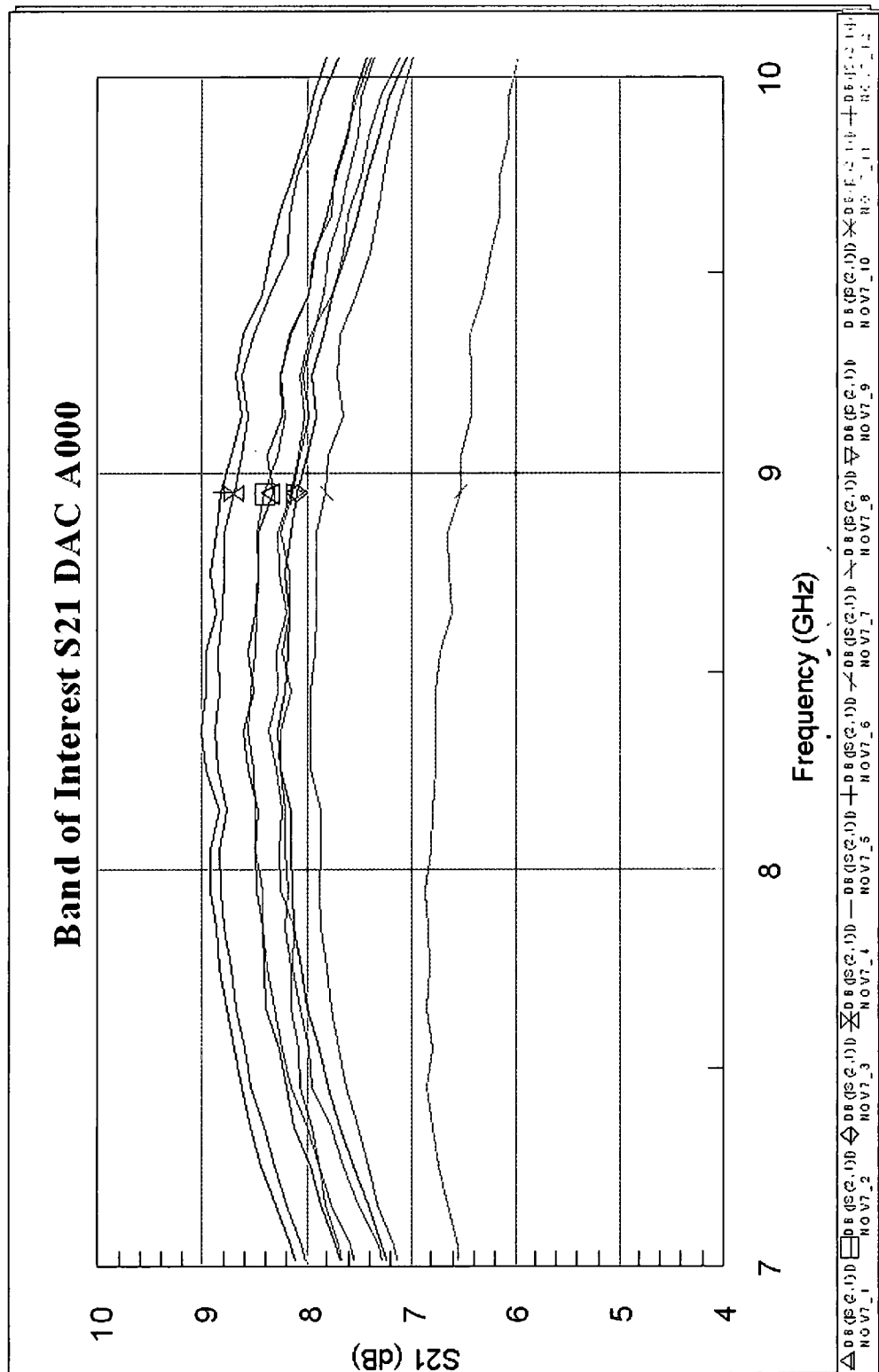


Figure 5.12: S21 Measured results through DAC transitions with Current DAC held constant across X-Band

Next, characterization of the current steering DAC portion was measured with the DAC being held constant. Fig. 5.13 and Fig. 5.14 show the input and output match are better than -10 dB over X-Band. The measured gain variation is from 5.95 dB to 8.38 dB, Fig. 5.15, using the current steering DAC.

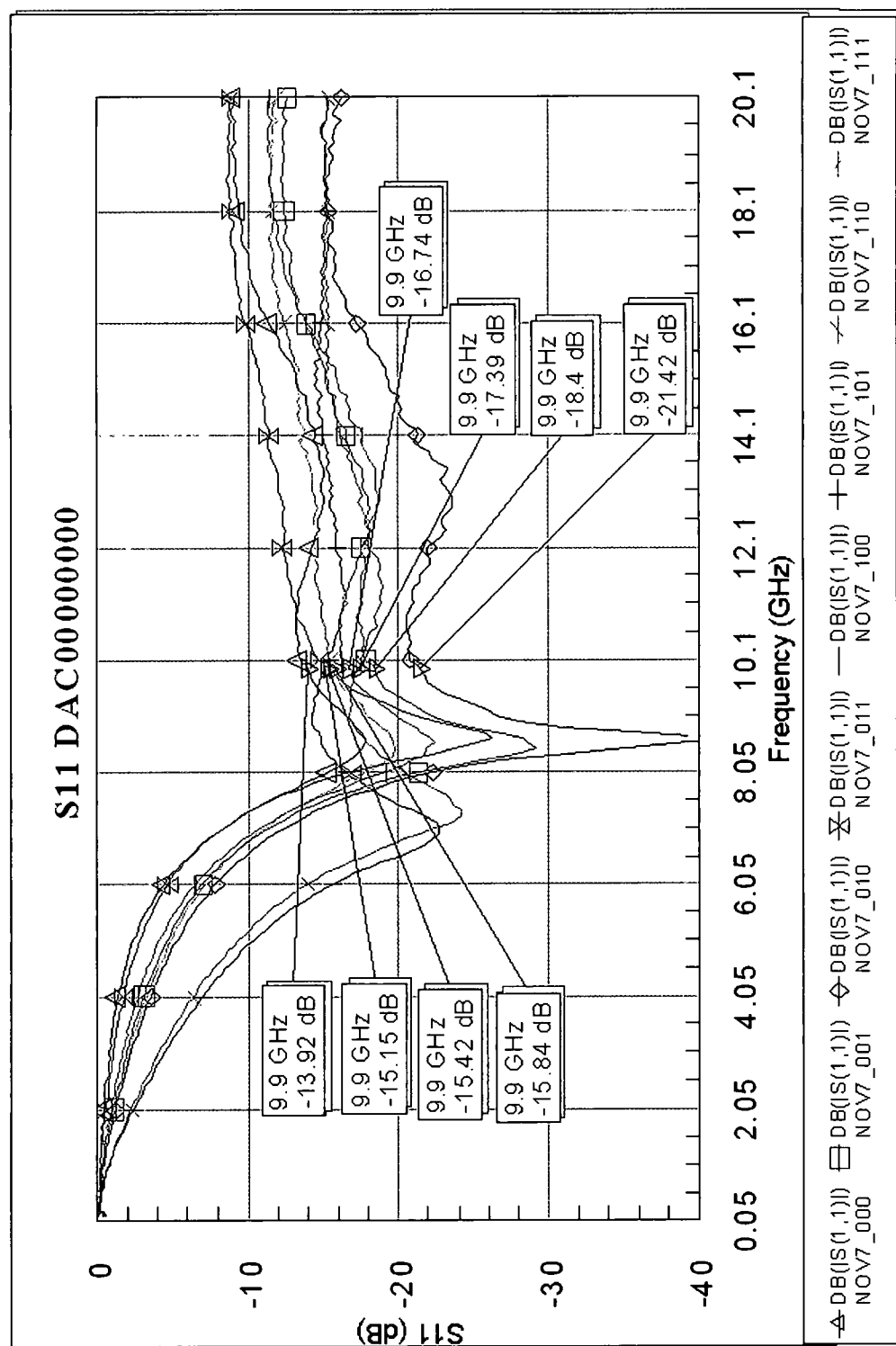


Figure 5.13: S11 Measured results through Current DAC transitions with DAC held constant

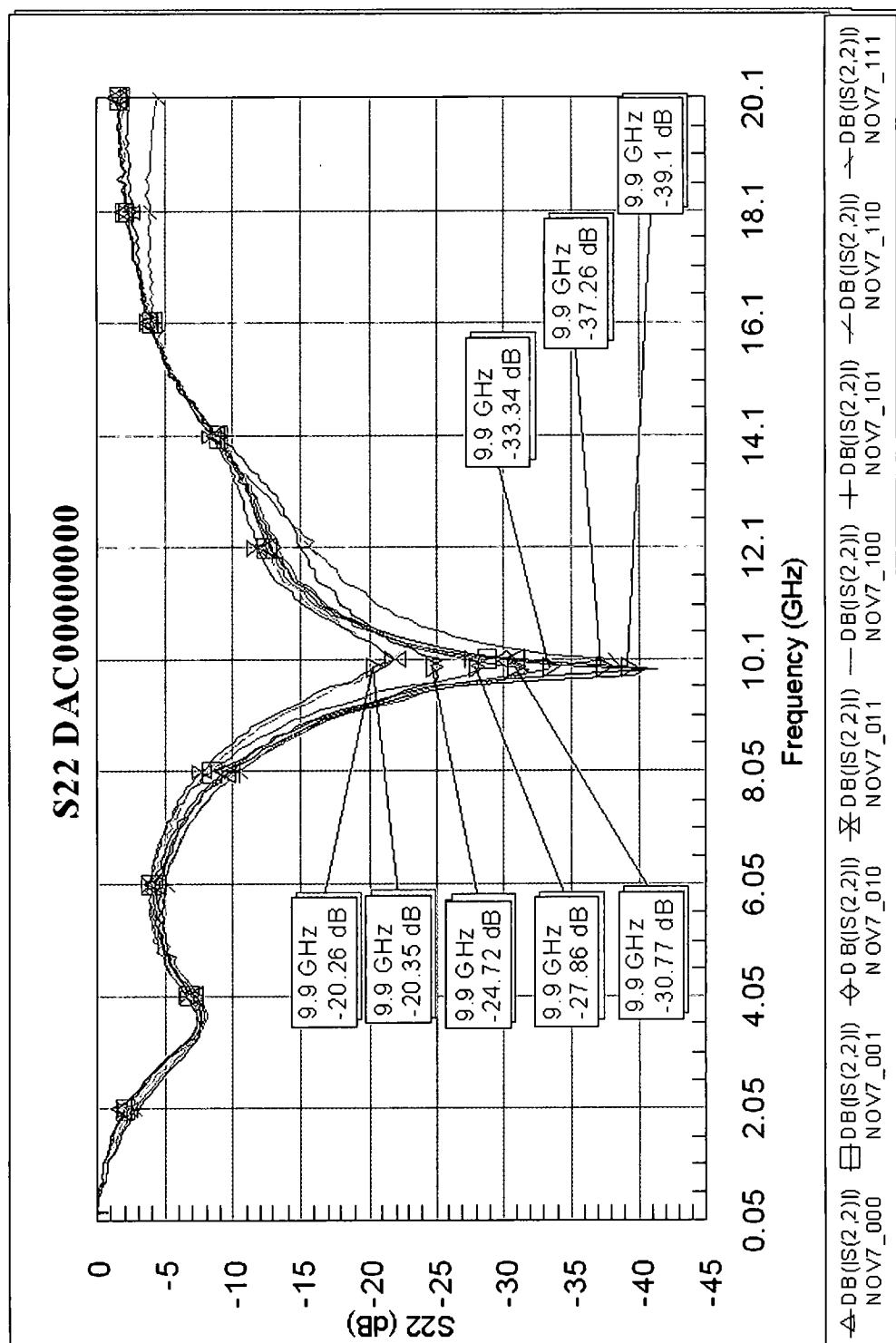


Figure 5.14: S22 Measured results through Current DAC transitions with DAC held constant

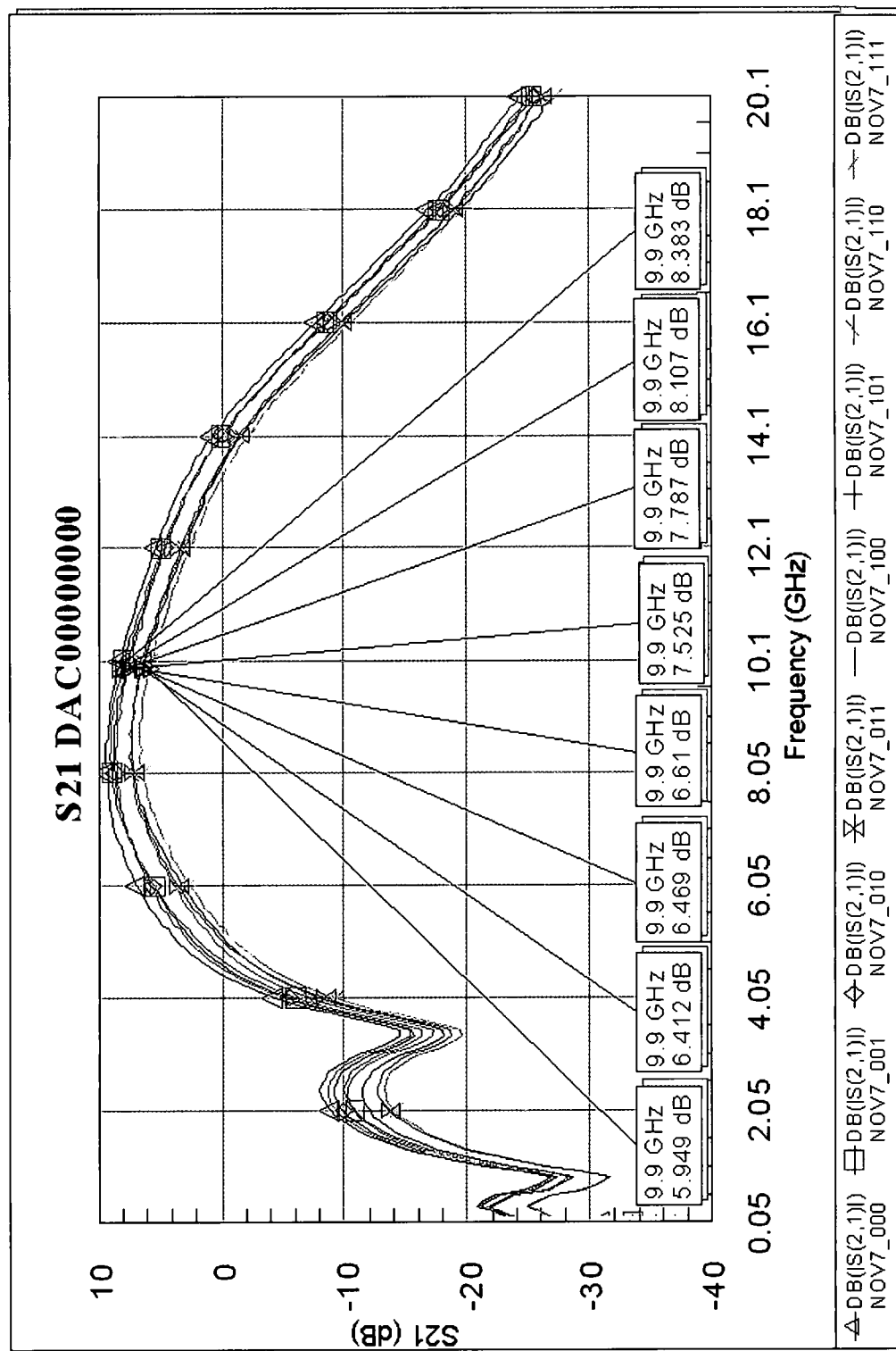


Figure 5.15: S21 Measured results through Current DAC transitions with DAC held constant

A comparison between simulated and measured data shows that the VGSA gain response was lower than expected. The simulated gain at 10 GHz was greater than 10.0 dB for all gain states. However, the maximum measured data gain response is 8.4 dB. This discrepancy can be attributed to the maturity of the SiGe process. The 0.13 μm SiGe process is still under development and the foundry is continuing to improve the active devices. Other potential sources of this discrepancy are unaccounted parasitics and inaccuracies in the foundry provided models.

CHAPTER VI

Summary and Conclusions

This research effort successfully demonstrated a VGSA at X-Band with integrated digital control logic. The measured gain variance is 2.3 dB across the frequency of operation, and the slope variance is from 0 to -0.125 dB/GHz. To date this is the only work that provides both gain and slope compensation. The input and output matching are better than 2:1 VSWR for a 50 Ohm system. Since the input and output matching conditions remain relatively close, with either gain or slope adjustment, this amplifier is ideal for integrating into larger systems. Additionally, the amount of gain and slope adjustment presented allows compensation for process variation, input power, and associated gain slopes of a RX/EX system.

The hybrid VGSA module would benefit from additional work in further integration of the feedback DAC with the RF amplifier. Also, the addition of large valued DC bypass capacitors in the hybrid would suppress any potential low frequency oscillation. Modifications to the PiC controller board would be required to move the PiC controller board off of the probe station during testing which eliminates any probe contact issues during testing. Another option would be to create an RF fixture that would allow the VGSA to have connectors for rapid testing of multiple bias DAC states.

This VGSA enables greater flexibility in future RF RX/EX systems. However, a greater understanding of the impact of the VGSA on system level

RX/EX performance metrics should be addressed and understood. This includes a detailed analysis on system noise figure, gain, and linearity. Additionally, a pairing of the VGSA with a control unit, either a FPGA or microprocessor, would be ideal for on-the-fly adjustment of the bias control for optimal performance.

APPENDIX I

Enlarged Graphs

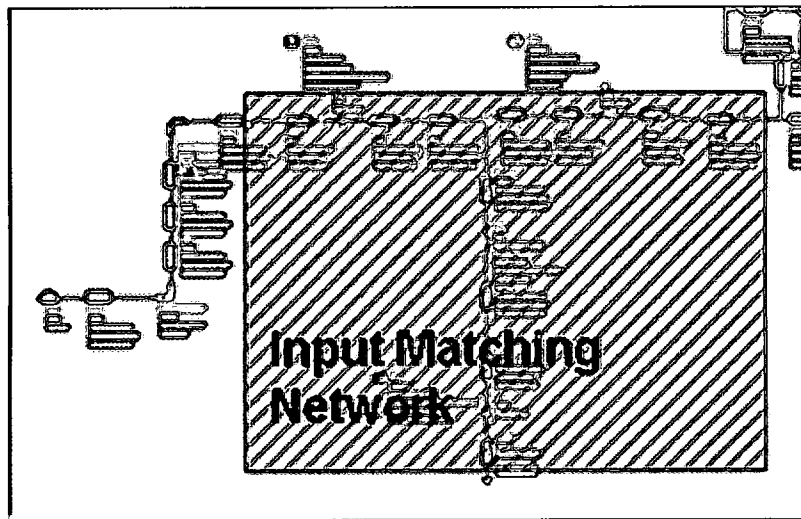


Figure A1: Input matching network schematic

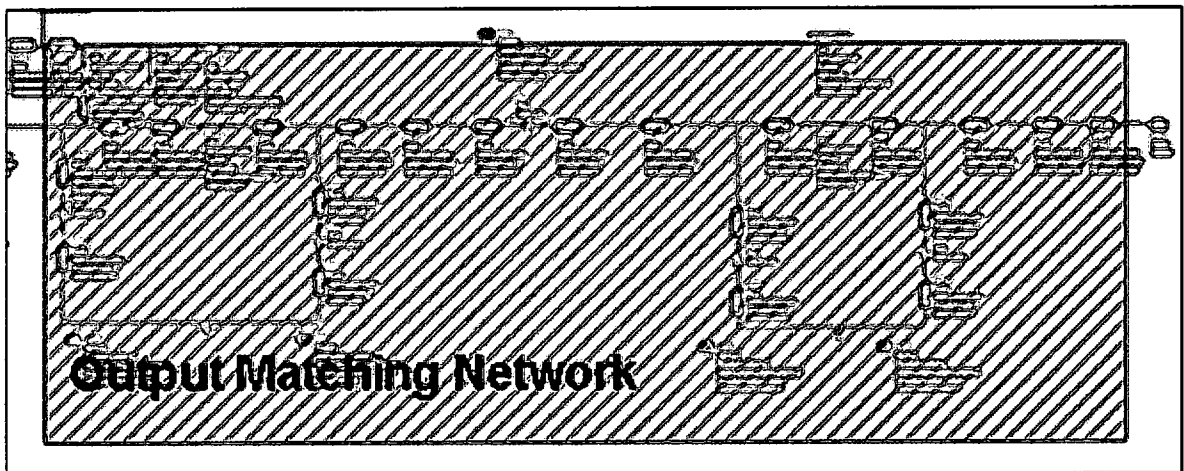


Figure A2: Output matching network schematic

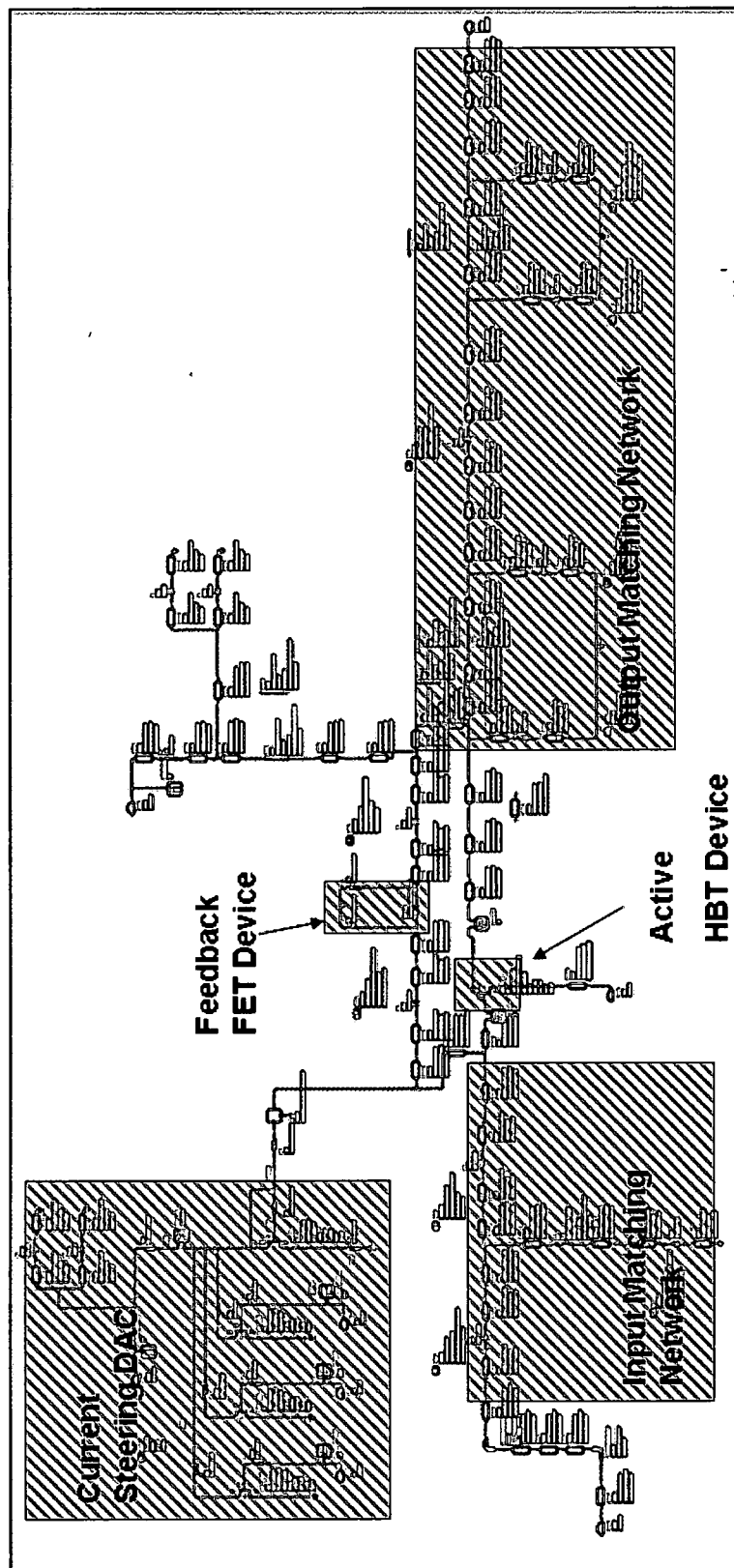


Figure A3: Enlarged Final X-band amplifier schematic

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